Editors' Suggestion

InAs-Al hybrid devices passing the topological gap protocol

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We present measurements and simulations of semiconductor-superconductor heterostructure devices that are consistent with the observation of topological superconductivity and Majorana zero modes. The devices are fabricated from high-mobility two-dimensional electron gases in which quasi-one-dimensional wires are defined by electrostatic gates. These devices enable measurements of local and nonlocal transport properties and have been optimized via extensive simulations to ensure robustness against nonuniformity and disorder. Our main result is that several devices, fabricated according to the design's engineering specifications, have passed the topological gap protocol defined in Pikulin *et al.* (arXiv:2103.12217). This protocol is a stringent test composed of a sequence of three-terminal local and nonlocal transport measurements performed while varying the magnetic field, semiconductor electron density, and junction transparencies. Passing the protocol indicates a high probability of detection of a topological phase hosting Majorana zero modes as determined by large-scale disorder simulations. Our experimental results are consistent with a quantum phase transition into a topological superconducting phase that extends over several hundred millitesla in magnetic field and several millivolts in gate voltage, corresponding to approximately one hundred microelectronvolts in Zeeman energy and chemical potential in the semiconducting wire. These regions feature a closing and reopening of the bulk gap, with simultaneous zero-bias conductance peaks at *both* ends of the devices that withstand changes in the junction transparencies. The extracted maximum topological gaps in our devices are 20–60 μeV. This demonstration is a prerequisite for experiments involving fusion and braiding of Majorana zero modes.

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I. INTRODUCTION

Topological quantum computation offers the promise of a high degree of intrinsic hardware-level fault tolerance [1–6], potentially enabling a single-module quantum computing system that is capable of solving critical problems sufficiently rapidly to have societal impact [7]. This approach hinges on (a) reliably producing a stable topological phase of matter that supports non-Abelian quasiparticles or defects and (b) processing quantum information through protected operations, such as braiding. The former is challenging due to the material parameter and disorder requirements for topological phases of matter. In this paper, we report on three-terminal semiconductor-superconductor nanowire devices that pass the stringent topological gap protocol [8] and therefore satisfy these requirements. We further extract the gap associated with the topological superconducting phase in our devices [9–12].

Topological phases are a form of matter in which the ground state has long-range quantum entanglement and there is a gap to excited states [13]. Unlike phases of matter that can be distinguished completely by local measurements, topological phases are identified by the transformations of their low-energy states that result from fusing and braiding their quasiparticles and defects. Directly measuring these properties in experiments is rather subtle [14], hindering efforts to fully determine the topological order of candidate materials. In the fractional quantum Hall regime, for example, a quantized Hall conductance reveals the presence of a nontrivial topological phase, but many different topological phases can have the same Hall conductance. Consequently, different measurements are necessary to determine which topological phase is present in a given device [15–22].

In the case of quasi-one-dimensional superconducting wires without any symmetries enforced, there are only two phases, one trivial and one topological. The latter supports Majorana zero modes (MZMs) localized at the ends of the nanowire [9,11,12]. While MZMs can be directly detected through fusion and braiding, one of their auxiliary signatures are zero-bias peaks (ZBPs) in the differential tunneling conductance at the nanowire's ends [23–28]. Indeed, most of the earlier experimental studies of candidate topological superconductors focused on ZBPs [29–42]. However, ZBPs can also be caused by disorder [43–45], smooth potential variations near the tunnel junction [46–51], unintentional quantum dots [52,53], or a supercurrent [54]. These trivial ZBPs can persist over a fairly large range of system parameters [55–57].

A ZBP associated with an MZM must have a partner at the other end of the wire and should be stable to variations in the electric and magnetic fields in the device. The stability of MZMs with respect to such variations is determined by the bulk gap. However, if a device has a sufficiently large number of control parameters, it is likely that it can be tuned into a configuration in which it has trivial ZBPs at both ends. Meanwhile, the predicted range of stability of a topological phase depends strongly on device geometry, the full stack of materials, and disorder, rendering it difficult to distinguish "stable" ZBPs from "accidental" ones purely empirically. Analyzing the detailed shapes of tunneling conductance spectra leads to some loose qualitative patterns, but there is no sharp binary distinction between the local tunneling conductance spectra associated with MZMs and trivial ZBPs at nonzero temperature. In short, neither more extensive data sets of ZBPs nor more beautiful ZBPs can distinguish the topological and trivial phases. Therefore, it is crucial to develop a practical, reliable protocol that enables the detection of the topological superconducting phase of a nanowire, and it is clear that additional measurements beyond the tunneling conductance are necessary for such a protocol.

This challenge is addressed by the topological gap protocol (TGP) [8], which is designed to reliably identify the topological phase through a series of stringent experimental tests. At the heart of this protocol is the fact that there is necessarily a quantum phase transition between the trivial and topological phases [58]. The protocol detects a bulk phase transition between low-magnetic-field and high-magnetic-field phases via a bulk gap closing. It establishes that the high-field phase is topological through the stability of its ZBPs, in a manner that we specify below. The TGP requires three-terminal device geometries, which overcome the limitations of many earlier two-terminal devices. They allow ZBPs to be simultaneously observed at both ends and also allow for a measurement of the bulk transport gap through the *nonlocal conductance*. The protocol is passed when (a) ZBPs are observed in the local conductances measured at tunnel junctions at both ends of a wire, and they are stable to changes in the junction transparency; (b) these stable ZBPs persist over a range of magnetic fields and electron densities in the wire; (c) a closing and reopening of the bulk transport gap is detected in the nonlocal conductances; (d) there is a region in the bulk phase diagram whose boundary is gapless and whose interior is gapped and has stable ZBPs; (e) the observed bulk transport gap throughout this region, the *topological gap*, exceeds the resolution of the measurement.

The hallmarks of most topological phases, including the one discussed here, are rather subtle: there is no signature as immediate as a quantized conductance or Meissner effect since there is no transport coefficient or thermodynamic observable that is a topological invariant of one-dimensional (1D) superconductors. Instead, the existence of a topological phase is imprinted on the measurable properties of the system in a manner that can only be identified through an elaborate measurement and analysis procedure such as the TGP or the even more elaborate procedures necessary for fusion and braiding. Thus, it is of paramount importance that the TGP has been validated by applying it to simulated transport data, especially since the tunneling spectroscopy and transport measurements comprising the TGP do not measure a topological invariant directly.

In simulated devices, we know whether there is a topological phase since we can compute a topological invariant. Hence, we tested the TGP on transport data from simulated

devices by comparing its output to this topological invariant. We emphasize that we have *not* attempted to establish qualitative similarities between simulated and measured conductance plots and this is not the purpose of these simulations. The goal is see if the TGP correctly distinguishes between regions with trivial and nontrivial topological invariant.

We simulated hundreds of devices with different disorder levels and concluded that if a device passes the TGP, then the probability that the candidate region in the phase diagram is not topological is $<8\%$ at the 95% confidence level. The TGP thereby distinguishes MZMs from trivial Andreev bound states and determines whether topological superconductivity is present in the parameter range scanned in a data set. Having thus confirmed the reliability of the TGP on simulated data, we formulate the central question of this paper: *Can we fabricate and measure devices that pass the TGP?*

We answer this question in the affirmative by presenting data from four devices, named A, B, C, and D, that have passed this protocol with respective maximum topological gaps ranging between 20–60 μeV. As we explain in more detail in Sec. II, our devices are based on heterostructures combining indium arsenide (InAs) and aluminum (Al). The superconducting component is an Al strip, epitaxially grown on the semiconductor so that it induces superconductivity via the proximity effect. The semiconducting portion is a shallow InAs quantum well hosting a two-dimensional electron gas (2DEG) that has been depleted by electrostatic gates, except for a narrow conducting wire that remains underneath the aluminum strip. Within this suite of components, we have used simulations to optimize the material stack and the device geometry with respect to the topological gap.

Disorder is the principal obstacle to realizing a topological phase supporting MZMs. We have used simulations to predict the (design-dependent) disorder level that the topological phase can tolerate. These simulations incorporate self-consistent electrostatics, the orbital effect of the magnetic field, and realistic semiconductor-superconductor coupling; see Refs. [41,59,60] for more details. Consequently, they show both qualitatively and quantitatively how device design can impact the effective disorder strength. Many of the resulting specifications are quite demanding, including (1) higher mobility ($>60\,000$ cm^2/V s) than previously achieved in shallow InAs quantum wells and (2) gate-defined wires that are sufficiently narrow (<120 nm) as to enable tuning into the single sub-band regime.

Our simulations indicate that mesoscopic fluctuations are important in our 3 μm long "topological gap devices" based on InAs-Al heterostructures (see Fig. 2). Thus, even devices with the same average disorder level can have different TGP outcomes: some disorder realizations will pass while others fail. The disorder strength determines an expected yield for passing the TGP which is between 0% and 100% over a range of disorder levels. As expected from these simulation results, we have also measured devices that were similar to devices A–D but did not pass the TGP, and we report on data from two of them, which have been named devices E and F.

In summary, each of devices A–D has a high probability of being in the topological phase. To the best of our knowledge, these devices are the first to have passed as stringent a set of requirements as those encompassed by the TGP, namely, (a) concurrent ZBPs that are stable both with respect to changes of the junction parameters and also with respect to changes of the bulk parameters that are larger (in appropriate units) than the bulk gap; and (b) a bulk gap closing and reopening in response to an increasing magnetic field that is visible in the nonlocal conductance, indicating a quantum phase transition into a phase with correlated ZBPs.

II. TOPOLOGICAL GAP DEVICE DESIGN AND REQUIREMENTS

A. Proximitized semiconductor nanowire model and its topological phase diagram

In this section we briefly review the proximitized nanowire model [11,12] which supports topological superconductivity over a range of densities and magnetic fields. The minimal model is comprised of a semiconductor nanowire with Rashba spin-orbit interaction coupled to a conventional (s-wave) superconductor. The effective Hamiltonian for such a system is

$$\begin{aligned} H &= H_{\rm SM} + \Delta_{\rm ind} O_{\rm SC},\\ H_{\rm SM} &= \int_0^L dx\, \psi^\dagger_\sigma(x)\left(-\frac{\partial_x^2}{2m^*} - \mu + i\alpha\hat{\sigma}_y\partial_x + V_x\hat{\sigma}_x\right)_{\sigma\sigma'}\psi_{\sigma'}(x),\\ O_{\rm SC} &= \int_0^L dx\,(\psi^\dagger_\uparrow(x)\psi^\dagger_\downarrow(x) + \text{H.c.}). \end{aligned} \tag{1}$$

Here, "SM" and "SC" are abbreviations for, respectively, semiconductor and superconductor, m^*, μ, and α are the effective mass, chemical potential, and Rashba spin-orbit coupling, respectively. V_x is the Zeeman splitting due to the applied magnetic field B along the nanowire: $V_x = g_{\rm SM}\mu_{\rm B}B/2$, where $g_{\rm SM}$ and $\mu_{\rm B}$ are, respectively, the Landé g-factor and Bohr magneton. The proximity to the s-wave superconductor is effectively described by the pairing operator $O_{\rm SC}$, while $\Delta_{\rm ind}$ is the induced pairing potential.

The zero-temperature phase diagram of the proximitized nanowire Hamiltonian of Eq. (1) consists of a trivial (s-wave-like) phase and a topological phase, as shown in Fig. 1. The latter supports MZMs at the opposite ends of the nanowire and is in the same phase as a spinless p-wave superconductor [9]. The trivial and topological phases are separated by a quantum phase transition at $V_x = \sqrt{\mu^2 + |\Delta_{\rm ind}|^2}$ which is necessarily accompanied by the closing of the bulk gap. The stability of a topological phase is characterized by its bulk transport gap or, equivalently, the gap to extended excited states, which we call the topological gap $\Delta_{\rm T}$. In the idealized case of Eq. (1), this is simply the bulk gap. This phase has been proposed to occur in quasi-one-dimensional systems composed of chains of magnetic atoms on the surface of a superconductor [61–65]; in nanowires that are completely encircled by a superconducting shell in which the order parameter winds around the wire due to the orbital effect of the magnetic field [41,66,67]; and in the vortex cores of three-dimensional superconductors [68,69]. The corresponding two-dimensional topological superconducting state can occur in $p + ip$ superconductors [58], at the surface of a topological insulator [70–72], in ferromagnetic insulator-semiconductor-superconductor heterostructures [10,24,38,73–76], and in s-wave superfluids of ultracold fermionic atoms [77,78].

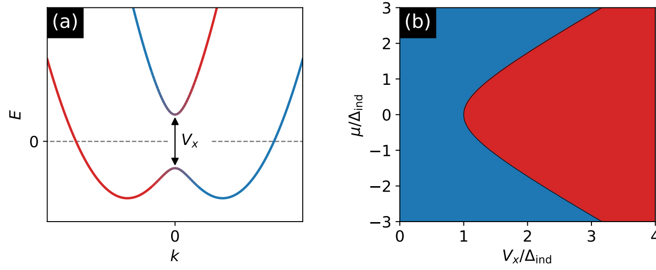

FIG. 1. (a) Energy spectrum as a function of momentum k along the nanowire. Rashba spin-orbit coupling splits the parabola at the bottom of the band into two parabolas displaced in k. The Zeeman energy V_x is proportional to the external magnetic field perpendicular to the direction of the Rashba spin-orbit coupling. A nonzero Zeeman energy V_x opens a gap at $k = 0$. When the chemical potential μ is within the gap, the nanowire Hamiltonian (1) has only one pair of Fermi points with spin and momentum locked. The color gradient represents the change of spin orientation with momentum. (b) The topological phase diagram as a function of Zeeman energy V_x and chemical potential μ. Δ_{ind} is the superconducting gap induced in the semiconductor nanowire. The low-field (blue) phase is a trivial superconductor while the high-field (red) phase is a topological superconductor that supports MZMs at the opposite ends of the nanowire.

The model discussed so far neglects many of the ingredients of actual devices, such as additional sub-bands and the orbital effect of the magnetic field. To address this, we have developed realistic three-dimensional (3D) simulations that take these effects into account. These simulations include self-consistent electrostatics, orbital magnetic field contributions, and renormalization effects due to coupling to the superconductor [59,60,79–82]. We have validated these simulations through comparison with ARPES [83], THz spectroscopy [84], the Hall bar measurements reported in Appendix B, and transport through multiple types of previous devices involving proximitized semiconductor nanowires [41,85–87]. We also take into account multiple disorder mechanisms such as charged disorder and variations of geometry and composition along the wire length, as discussed in Sec. II E. The superconductor's degrees of freedom are integrated out, yielding a formulation in which it is encapsulated by self-energy boundary conditions [41,86,87]. Using this advanced simulation model, we optimized the design for gate-defined devices based on high-quality 2DEG heterostructures in order to minimize the effects of disorder, additional su-bands, and the orbital effect of the magnetic field. This design is presented in the next subsection. We extract the parameters of a minimal model projected to the lowest sub-band (neglecting couplings to higher sub-bands which are suppressed by large sub-band level spacing) in Appendix A 1. Our minimal model is similar to Eq. (1). The parameters that define this effective single-sub-band model are listed in Table I. This projected model and the full 3D model show good agreement for bulk quantities in the field and density ranges of interest. In order to simulate transport properties, we add a realistic description of the junctions (junction design is described in the following section). We perform these simulations by projecting the full 3D model of our device to the low-energy subspace. The

TABLE I. Single-band effective model parameters obtained for various device designs. The δ' stack is not simulated. It has similar effective parameters to the δ stack, but differs in lever arm.

Design, stack	m^* [m_e]	α^* [meV nm]	g^*	Γ [meV]	$d\mu/dV_p$ [meV/V]
SLG-β	0.032	8.7	−11.8	0.13	85
DLG-δ	0.032	8.4	−11.5	0.21	79
DLG-ε	0.032	8.3	−11.4	0.32	78

corresponding results are presented in Sec. III. After we have discussed the device design, we describe the general effects of disorder in mesoscopic topological wires, then quantify the effective disorder potential in our devices.

B. Gate-defined proximitized nanowire

Our devices are defined by an Al strip separated from an InAs quantum well by a barrier layer. There are two designs which are conceptually similar but have some practical differences. One has a single-layer gate (SLG) design while the other has a dual-layer gate (DLG) design, shown in Figs. 2 and 3, respectively. We will refer to both designs as "topological gap devices." A cross-section of an SLG device is shown in Fig. 2(d), where the Al strip is light gray. The strip's dimensions have been optimized using the simulations described above: length 10 μm, width <120 nm, thickness <10 nm.

The length is in the direction perpendicular to the cross-section in Fig. 2(d). The Al strip is covered by a several nm thick top oxide formed by controlled oxidation [not shown in Fig. 2(d) or Fig. 3(c)]. The Al strip features larger Al pads at each end of its 10 μm length, which can be seen at the right and left edges of the scanning electron micrograph (SEM) images in Figs. 2(b) and 3(b). The pads are contacted with Ti/Au or Ti/Al Ohmic leads, by which the Al strip is grounded. (Both types of contacts are normal in the typical operating regime.) We will denote the direction perpendicular to the surface of the quantum well as the z direction, while the directions along and perpendicular to the Al strip are the x and y direction, respectively, as shown in Figs. 2(c) and 2(d).

There is a dielectric layer that separates the superconductor-semiconductor heterostructure from the electrostatic gates that are at the top of the cross-section in Figs. 2(d) and 3(c). The gates deplete the 2DEG except underneath the Al, which partially screens their electric fields, thereby creating a high-quality nanowire. The top view in Fig. 2(a) and the SEM image in Fig. 2(b) show that the split-gate structure of the SLG design is divided into three sections: three plunger gates and three cutter gates. The three plunger gates serve to deplete the 2DEG on their side of the Al strip while the three cutter gates deplete the 2DEG on the other side. Once the 2DEG has been depleted, operating the plunger gates at even more negative voltages tunes the density underneath the Al via the fringe electric fields that remain after screening by the Al. The densities in the left, middle, and right sections can be controlled independently by the three plunger gates. We operate in the low-density limit in which only the lowest z-direction sub-band is occupied so, here and henceforth, will use the term "sub-band" for

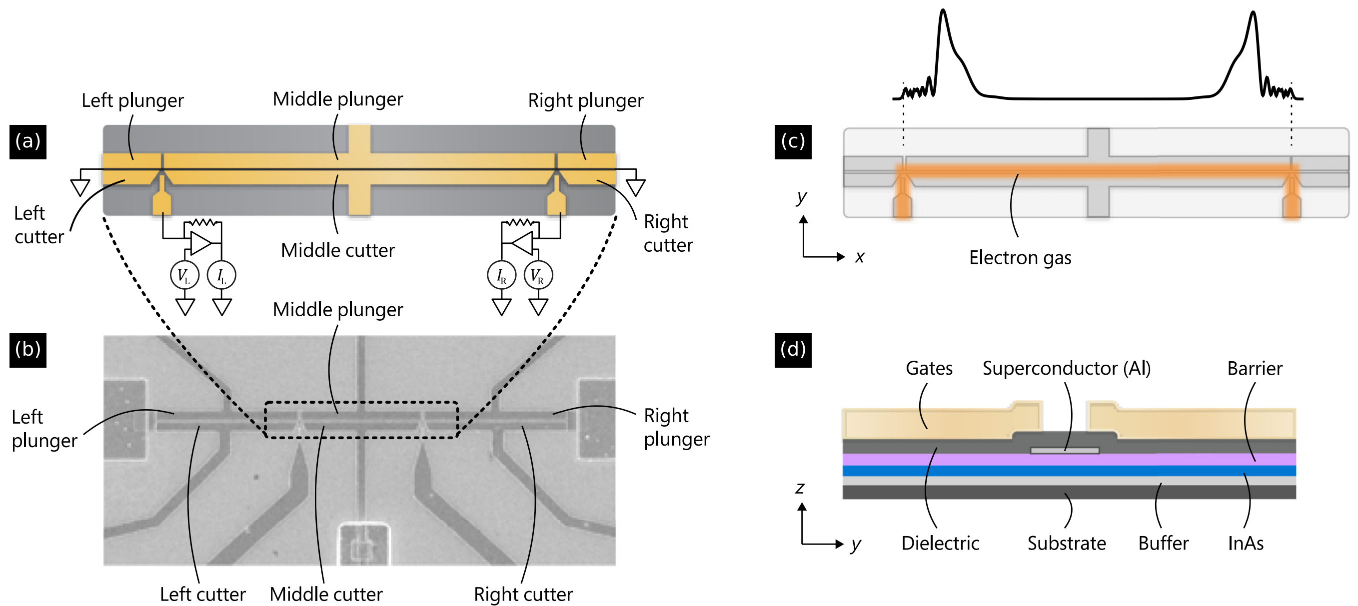

FIG. 2. (a) A schematic of the top view of the active area of a single-layer gate (SLG) topological gap device. All of the labeled gates serve to deplete the 2DEG in the InAs quantum well to define a high-quality one-dimensional conducting channel. The left, middle, and right plungers also tune the density in the corresponding sections of the device, while the left and right cutters also open and close the junctions. The two unlabeled gates are the "helper gates" which are used to control the electron density in the junctions and leads, the latter of which are connected to a measurement circuit as shown in this panel. (b) An SEM image of a topological gap device. The dashed line indicates the active region depicted in (a). (c) Region of nonzero electron density (orange) in the InAs quantum well when the device is tuned to the operating regime: the middle section (underneath the middle cutter/plunger) is tuned to the topological regime while the outer sections (underneath the left/right cutter/plunger gates) are tuned to the trivial phase using the plunger gates. The black curve shows the local density of states in the wire near zero energy, computed in the ideal disorder-free limit. (d) A schematic of the cross-section of an SLG topological gap device, in which the Al strip induces proximity superconductivity in the one-dimensional InAs nanowire that is defined by the gates shown in (a) and extends perpendicular to this cross-sectional view. The x, y, and z directions are indicated in (c) and (d).

y-direction sub-bands. The left and right plungers control the densities underneath the corresponding sections of the Al, which are normally set for full depletion (no occupied sub-bands) underneath the Al. The width of the Al strip was chosen to enable this for moderate gate voltages $V_{\rm dep} > -3$ V and also to minimize the orbital effects of a magnetic field in the x direction.

There are two side tunnel junctions at the boundaries between the middle cutter gate and the left/right cutter gates, enabling the three-terminal measurements [88–92] of the conductance matrix that are necessary for the TGP, as we discuss in Sec. III. In addition to depleting the 2DEG on the opposite side of the Al strip from the plungers, the left and right cutter gate voltages $V_{\rm lc}$ and $V_{\rm rc}$ are also used to vary, respectively, the transparency of the left and right tunnel junctions. The split-gate geometry with plunger-cutter pairs ensures independent tuning of density and junction transparency for each section of the gate-defined nanowire. The two junctions are typically tuned into the tunneling regime in which the above-gap low-temperature differential tunneling conductance $G_{\rm N}$ is $\lesssim e^2/h$, while the Al strip is grounded. The junctions are connected to Ohmic contacts via conducting paths in the 2DEG. There are two "helper" gates, which are the unlabeled gates at the bottom of Fig. 2(a); they extend from the junctions to the bottom edge of the SEM in Fig. 2(b). The helper gates define these conducting paths by accumulating carrier density in the 2DEG underneath them and keeping it conducting. The orange region in Fig. 2(c) shows where the electron density is nonzero in the 2DEG in the device's normal operating regime: underneath the middle section of the Al strip and underneath the helper gates.

In the DLG design, instead of a split-gate geometry, the plunger gates cover the Al strip completely, as illustrated schematically in Fig. 3(a) and in an SEM image shown in Fig. 3(b). This makes it considerably easier to align the gates with the Al strip. Moreover, the plunger gates have a single role, which is to control the electron density in the 2DEG, to fully deplete it underneath the regions adjacent to the Al strip and to either fully deplete it or to tune it to the lowest sub-band directly underneath the Al strip. The function of controlling the bulk density is separated from the function of opening and closing the junctions, which is accomplished by cutter gates that are in a second gate layer, separated from the first gate layer by a second dielectric layer. The cutter gates in the DLG design only cover the junctions, so they do not affect the bulk density in the wire. Although the above differences between the SLG and DLG designs are practically important, the basic principles and length scales are the same in both.

We will call the semiconductor underneath the middle section "the wire," and the superconducting gap that is induced in the wire at $B = 0$ via the proximity effect the "induced gap" $\Delta_{\rm ind}$. We denote the middle plunger gate voltage by $V_{\rm p}$, which tunes the density in the wire. At the optimal operation point, the wire is tuned to the single-sub-band regime that occurs just

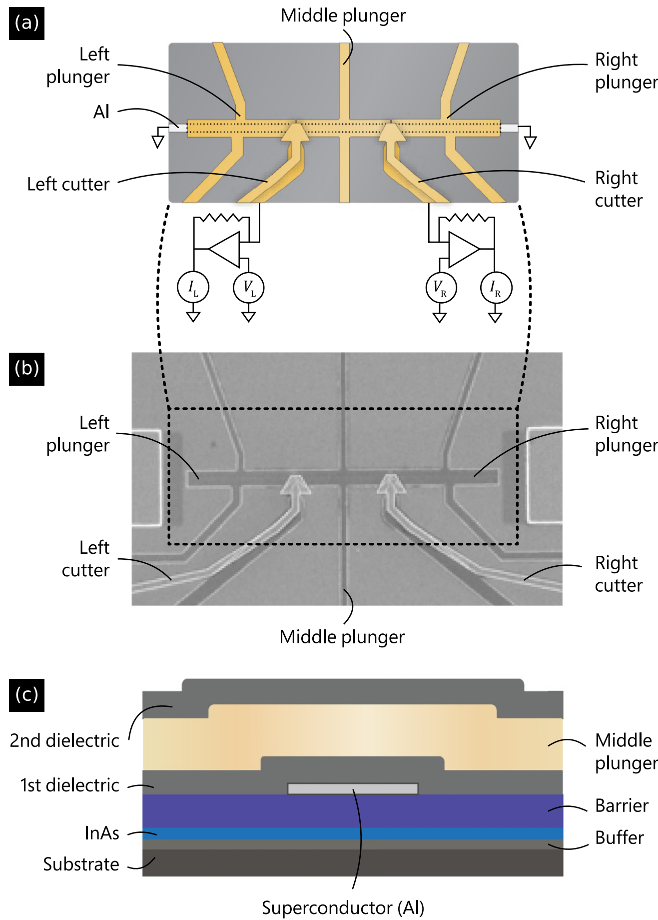

FIG. 3. (a) A schematic of the top view of the active area of a dual-layer gate (DLG) topological gap device. The plunger gates serve to deplete the 2DEG in the InAs quantum well to define a high-quality one-dimensional conducting channel and to tune the density in the corresponding sections of the device. The left and right cutters open and close the junctions. The two unlabeled gates are the "helper gates" which are used to increase the electron density in the junctions and leads, the latter of which are connected to a measurement circuit as shown in this panel. (b) An SEM image of a DLG topological gap device. The dashed line indicates the active region depicted in (a). (c) A schematic of the cross-section of the middle section of a DLG topological gap device, in which the Al strip induces proximity superconductivity in the one-dimensional InAs nanowire that is defined by the gates shown in (a) and extends perpendicular to this cross-sectional view. The bulk of the wire does not have a second gate layer, but the junctions have cutter gates in a second gate layer, and the second dielectric layer separates them from the plunger gates in the first gate layer.

before full depletion $V_{\mathrm{p}} \gtrsim V_{\mathrm{dep}}$. We will focus on the phase diagram of the wire as a function of the middle plunger gate voltage V_{p} and the magnetic field B.

We comment briefly on the length of the wire here and discuss it in greater detail in Appendix A 3. To operate the device in the optimal regime, the nanowire should be much longer than the coherence length in the topological superconducting state, so that MZMs are well localized at the opposite ends of the nanowire [the situation depicted in Fig. 2(c)]. In this case, MZMs would lead to ZBPs that are stable with respect to local perturbations. When the coherence length is comparable to or larger than the nanowire length, a ZBP at one end of the wire may arise from an Andreev state extending from the opposite end [93]. In this case, however, we do not expect ZBPs to be stable with respect to local perturbations. Our simulations suggest that, for these designs and material stacks, the coherence length in the topological state varies between 100–250 nm in the absence of disorder. The wire is designed to be much longer than this. Disorder in the bulk of the nanowire suppresses the topological gap and increases the coherence length which, as we discuss in Appendix A 3, leads to a nontrivial requirement for the wire length which depends on the stack geometry/composition and disorder level. On the other hand, the wire cannot be too long since the visibility of gap closings will be strongly suppressed if the length of the wire is more than several times the normal-state localization length [88].

Assuming weak to moderate disorder, the optimal wire length in our devices is 3 μm. This length choice also ensures that when a transport gap closing is observed, there is a nonzero density of states in the bulk at zero energy which has nonvanishing matrix elements to both leads so that nonlocal conductance is above the noise floor [90].

Finally, the outer sections (underneath the left/right cutter/plunger gates) must be significantly longer than the coherence length of the parent superconductor in order to prevent quasiparticle transport below the parent gap at full depletion.

C. Material stack

The material stack of the topological gap device is optimized to produce a large topological gap. To achieve a topological phase, the semiconductor stack needs to produce a large spin-orbit coupling and a large nominal g-factor in the confined 2DEG. In addition, the heterostructure should provide a low disorder environment, typically parametrized by high 2DEG mobility at low temperatures. Given the lack of suitable insulating and lattice-matched substrates, the active region is grown on an InP substrate employing a graded buffer layer to accommodate lattice mismatch.

The active region consists of the Al superconductor, an upper barrier, the InAs quantum well, and the buffer. The upper barrier layer plays a critical role in fine-tuning the coupling between the superconductor and the 2DEG residing in the quantum well. To drive the device into the topological phase, B needs to be increased until the Zeeman energy $\mu_{\mathrm{B}}|g^{\star}|B/2$ exceeds the induced gap Δ_{ind}. Here, $g^{\star}$ is the renormalized g-factor in the superconductor-semiconductor heterostructure, which is given by $g^{\star} = g_{\mathrm{SM}}\,\Delta/(\Gamma+\Delta)$ if we neglect the g-factor of aluminum; a more general form of the renormalization factor is discussed in Appendix A 1. For strong coupling Γ between the wire and the Al strip, Δ_{ind} would approach the gap in the Al strip Δ_{Al} and the electronic wave function of the single occupied sub-band of the wire would have large weight in the Al strip. In this case, $|g^{\star}|$ would be renormalized to small values. In such a case, $\mu_{\mathrm{B}}|g^{\star}|B/2$ would not approach Δ_{ind} until the magnetic field is very large (>2.5 T), close to the critical in-plane field of the Al strip [27,59,94–96]. Conversely, if the coupling between the superconductor and semiconductor were too weak, the maximum attainable

topological gap would be small since it is bounded above by $\Delta_{\rm ind}$. Hence, the material stack must satisfy $k_{\rm B}T \ll \Delta_{\rm ind} < \Delta_{\rm Al}$.

As we shall see in Sec. IV, the parent gap in the Al strip is $\Delta_{\rm Al} \approx 300$ μeV (this is strongly dependent on the Al thickness). For an optimized heterostructure, according to our simulations of the device of Fig. 2(a), we expect 100 μeV $< \Delta_{\rm ind} <$ 200 μeV, corresponding to an induced gap to parent gap ratio of $0.33 < \Delta_{\rm ind}/\Delta_{\rm Al} < 0.67$, and $4 < |g^\star| < 7$.

Another function of the upper barrier layer is to separate the quantum well states from disorder on the dielectric-covered surface of the stack, thus enhancing the electron mobility. The quantum well thickness is chosen to minimize orbital effects from the magnetic field applied in the x direction, to allow electrostatic tuning, and to retain the desirable properties of InAs, including optimally renormalized $g^\star$.

Rashba spin-orbit coupling in the wire, characterized by the parameter α, enables superconductivity to coexist with the magnetic field B. Although α does not determine the critical field for the transition into the topological phase, it does contribute to the size of the topological gap and the extent of the topological phase in parameter space. The spin-orbit coupling in a 2DEG heterostructure covered with the superconductor is difficult to measure directly. Using weak antilocalization measurements in shallow InAs 2DEGs (see, for example, Ref. [97]), and typical values of the electric field (obtained from simulations assuming band offset parameter measured in Ref. [83]), we estimate that the Rashba spin-orbit coupling is in the range of 5 to 15 meV nm.

In this paper, we present the results of measurements and simulations of devices based on four different material stacks satisfying the requirements given in this subsection. While they all feature an InAs quantum well, there are important differences in the quantum well width, barrier composition and thickness, and dielectric. In Table I, we give the effective parameters that encapsulate the effect of these materials changes, such as the the effective mass, g-factor, and spin-orbit coupling. We will call these different materials stacks β, δ, δ', and ε.

D. Phase diagram of ideal devices

For the SLG and DLG device designs described in Sec. II B and the material stacks described in Sec. II C, we have computed the phase diagrams in the ideal disorder-free limit as a function of the actual control parameters of the device, $V_{\rm p}$ and B. This is to be contrasted with Eq. (1) and Fig. 1, which contain the effective parameters μ and V_x. The bare spin-orbit coupling in the semiconductor is taken to be $\alpha_0 = 10$ meV nm in both the SLG-β and DLG-ε designs. The color scheme in Fig. 4 is determined by the Pfaffian invariant [9,99] (see Appendix A 4 for a brief description of this invariant). Darker red corresponds to larger topological gap and darker blue corresponds to larger trivial superconducting gap, as indicated by the color scale on the right-hand side of the figure.

The red parabola in Fig. 1 has now become a sequence of red slivers in the ideal phase diagrams of an SLG device built on the β stack in Fig. 4(a) and a DLG device built on the ε stack in Fig. 4(b). The red slivers are topological phases with different numbers of occupied 1D sub-bands in the wire [27,100]. When we zoom in on any one of these slivers,

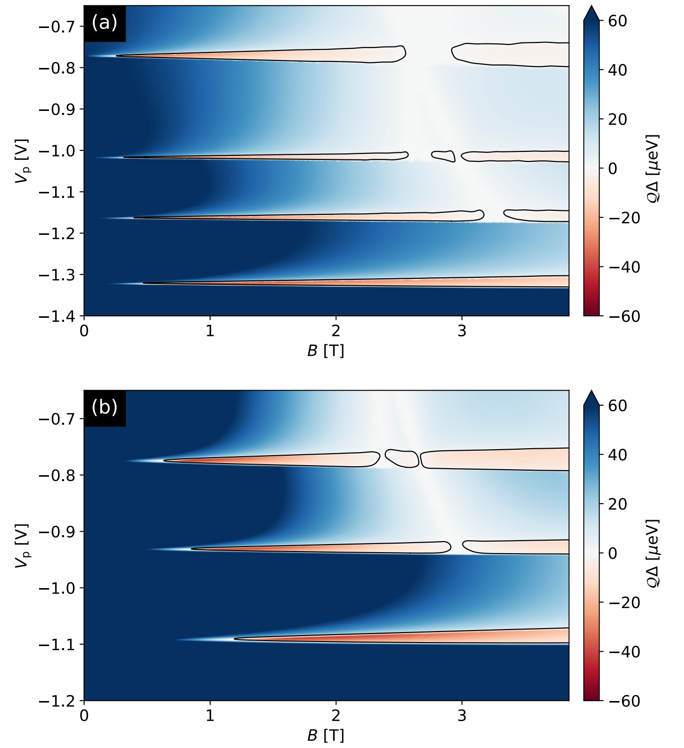

FIG. 4. (a) The simulated phase diagram of the SLG device design shown in Fig. 2(d) and the β material stack in the ideal disorder-free limit. (b) The simulated phase diagram of the DLG device design shown in Fig. 3(c) and the ε material stack in the ideal disorder-free limit. Here, the Pfaffian invariant $\mathcal{Q} = +1$ in the trivial phase and $\mathcal{Q} = -1$ in the topological phase. Hence, the color scale indicates the size of the gap in the trivial (blue) and topological (red) phases. The black curves indicate the phase transition where the topological invariant changes sign. The axes B and $V_{\rm p}$, the magnetic field and plunger gate voltage, respectively, are the actual control parameters of the device. Most of the phase diagrams in this paper will similarly be in the $(B, V_{\rm p})$ plane. This phase diagram is for a wire of infinite length. The maximum topological gap in the lowest sub-band is approximately 50 μeV. The data and scripts required to reproduce this and other simulated figures are available in Ref. [98].

we see that it has the parabolic lobelike shape $|g^\star|\mu_{\rm B}B/2 > \sqrt{\mu^2 + \Delta_{\rm ind}^2}$ that follows from Eq. (1). Here, the single-sub-band topological phase is at $V_{\rm p} \approx -1.35$ V, and it has a larger topological gap than when there are more occupied sub-bands. Recall that one of the design criteria was that the single-sub-band regime could be reached for moderate gate voltages; this figure confirms that it is satisfied by this design. As we increase $V_{\rm p}$, thereby increasing the number of occupied sub-bands, the effective cross-sectional area of the gate-defined nanowire increases and, at some point, the orbital effect of the applied magnetic field becomes very important. In the second sub-band, an orbital-field-induced gap closing is visible at $B \approx 3$ T and $V_{\rm p} \gtrsim -1.2$ V. It occurs at $B \approx 2.5$ T in the third sub-band and at lower fields in higher sub-bands. In contrast, in the lowest sub-band, an orbital-field-induced gap closing does not occur over the relevant field range. (At fields higher than 3.5 T, the Al parent gap can close, so an orbital-field-induced gap closing would be a subleading effect anyway.) Thus, in order to maximize both the accessible volume of the

topological phase and its maximum gap, it is necessary to tune the device into the single-sub-band regime.

There is very little difference between the SLG and DLG designs in the bulk of the wire; the principal difference is in the junctions, which have no effect on the ideal bulk phase diagram. However, the ε stack has larger Δ_{ind} and smaller g_{SM} so the topological phase occurs at higher B for this stack. Hence, the DLG-ε phase diagram in the clean limit has a lowest sub-band topological phase that is pushed to higher fields, as may be seen in Fig. 4.

Within the lowest sub-band, the effective mass m^*, effective Rashba spin-orbit coupling α^*, effective g-factor g^*, superconductor-semiconductor coupling Γ, and lever arm $d\mu/dV_{\text{p}}$ take the values given in Table I. As a result of the projection to the lowest sub-band, the bare Rashba spin-orbit coupling α_0 is replaced by the effective parameter α given in the table. The precise definition of the effective single-band model governed by these parameters is given in Appendix A 1.

E. Disorder and uniformity requirements

We now discuss the level of imperfection that our device designs can tolerate and still have a topological phase with coherence length $\xi(0)$ shorter than the wire length $L = 3$ μm. See Appendix A 3 for a discussion of the coherence length $\xi(0)$ and other important length scales.

In our devices, there are many different sources of disorder, including geometric and charged disorder [27,38,101]. Even small local variations in any of a number of device parameters can cause significant variations in the potential experienced by the electrons along the wire. As we discuss in Appendix A 1, we can extend the single-sub-band effective model (A1) parametrized by the couplings given in Table I to include disorder, leading to the Hamiltonian (A12). When the various disorder mechanisms are projected into this single-sub-band model, most of them can be characterized by the quenched Gaussian disorder model [102] in which disorder is represented by a random potential $V(x)$ whose probability distribution is approximately described by the second-order cumulant defined in Eq. (A14). Both the strength of disorder δV and its correlation length κ depend on each disorder source in a manner that is highly dependent on the specific design and must be calculated in a full three-dimensional model, as we describe below. The designs in Figs. 2 and 3 have been optimized to be as forgiving as possible by requiring that the design minimize the projected disorder for fixed microscopic disorder.

Even in such an optimized design, the topological phase is impossible if the disorder strength δV exceeds a critical value. For somewhat smaller disorder strengths, there will be a topological phase, but the coherence length $\xi(0)$ will be very long. We need still smaller δV in order to have a topological phase with $\xi(0) < L$. Hence, it is essential to understand and minimize the sources of disorder that contribute to δV.

In the regime of interest, the low-density regime with single-sub-band occupancy, charged disorder dominates [103]. From an analysis of the density dependence of the mobility of Hall bars, we conclude that charged disorder is located primarily at the interface between the semiconductor surface and the gate dielectric. Hall bar measurements allow us to extract the average density of charged imperfections at the semiconductor-dielectric interface, denoted by $n_{\text{2D,int}}$, and the lever arm $d\mu/dV_{\text{p}}$. This is illustrated in Appendix B. Each chip studied in this paper has both topological gap devices and Hall bars, as shown in Fig. 5, enabling us to extract the average density of charged imperfections for each chip and to assess the impact on topological gap devices of chip-to-chip changes in the disorder level. *Any impact that post-growth fabrication has on the semiconductor-dielectric interface in a topological gap device will be present in its partner Hall bar as well since they are processed together on the same chip.* If any fabrication processes increase the density of charged imperfections in a topological gap device, we will detect this in the corresponding Hall bar.

FIG. 5. There are Hall bars on the same chip as our topological gap devices, visible at the right and left sides, respectively, of this optical image. Both device types undergo the same processing steps, so the charged defect density at the semiconductor-dielectric interface $n_{\text{2D,int}}$ extracted from Hall mobility measurements is reflective of the semiconductor-dielectric interface in the neighboring topological gap device.

We have optimized the device geometry with respect to charged imperfections at the semiconductor-dielectric interface by choosing the Al width as wide as possible while still maintaining the ability to tune into the single-sub-band regime. This keeps the active region in the InAs quantum well as far as possible from charged disorder at the interface between the semiconductor and the dielectric [see Fig. 2(d)]. (As we discussed in Sec. II C, the barrier layer plays a similar role in separating charged disorder as much as possible from the active region.) We use self-consistent electrostatics calculations [59,60] to find the disorder potential underneath the Al. For realistic densities of charge defects $n_{\text{2D,int}}$, we find the variance of the projected disorder potential and correlation length to vary between $\delta V \approx 0.5$–1.5 meV and $\kappa \approx 75$–125 nm, respectively. In Fig. 23, we show how δV depends on $n_{\text{2D,int}}$ for the SLG and DLG designs of, respectively, Figs. 2 and 3 in the β, δ, or ε stacks.

From a transfer matrix calculation of $\xi(0)$ for the model in Eq. (A12), we can obtain the disorder strength δV at which the minimum value of the coherence length $\xi(0)$ begins to exceed our device length. Figure 23 enables us to translate that value into a target $n_{\text{2D,int}}$. In particular we obtain for SLG-β parameters that this occurs for $n_{\text{2D,int}} > 3\times10^{12}/\text{cm}^2$. The δ and ε stacks have slightly different requirements as a result of their stronger coupling to the superconductor Γ (which is still within the required range of $\Delta_{\text{ind}}/\Delta_{\text{Al}}$). Hence, an initial target for dielectric quality is $n_{\text{2D,int}} < 3\times\ 10^{12}/\text{cm}^2$. In this paper, we show data from devices that are below and above this

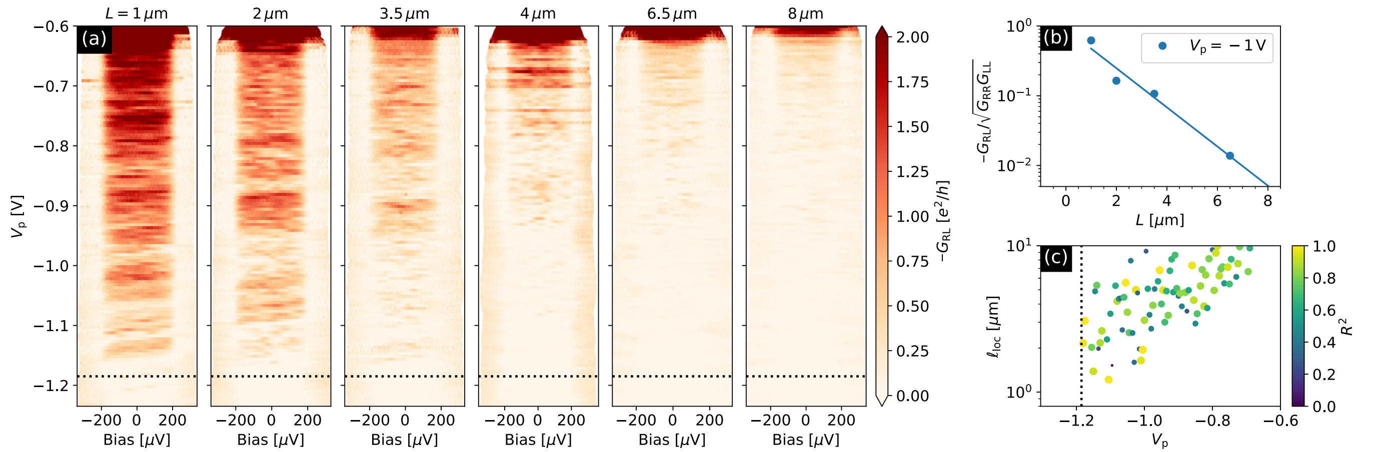

FIG. 6. The experimentally measured nonlocal conductance $-G_{RL}$ across sections of lengths $L = 1, 2, 3.5, 4, 6.5, 8\ \mu$m in the same wire (see Appendix C for a description of the device). (a) Shows the nonlocal conductance vs plunger and bias voltage for different length segments. Increasing the length directly leads to a significantly reduced conductance. Around $V_p = -1.185$ V the conductance of the 1 μm wire becomes larger than $0.05e^2/h$. The onset of conductance appearing around this gate voltage for multiple wire lengths suggests this signifies the onset of the first sub-band (indicated by black dotted lines). Around $V_p = -0.6$ V the conductance becomes very high in all segments because the entire 2DEG becomes conductive. In (b) an example of the localization length extraction is shown. The conductance is averaged over a small bias window of ±20 μeV to improve signal quality. The localization length is then extracted by fitting the data to the expected value of the typical conductance $-G_{RL}/\sqrt{G_{RR}G_{LL}} = A\ \exp(-2L/\ell_{loc})$ [104]. Fit parameters ℓ_{loc} and A are obtained by the linear fit of $\ln(-G_{RL})$ vs L with R^2 describing the quality of the fit. We normalize the nonlocal conductance $-G_{RL}$ by local conductances $\sqrt{G_{RR}G_{LL}}$ at zero bias to minimize the contributions of the local effects. (c) Shows the extracted localization length as a function of plunger. We note that it is above 1 μm throughout the measured range. We do not show points above 10 μm because the method cannot reliably determine ℓ_{loc} values greater than L.

target. The topological phase is present in the thermodynamic limit even for relatively high disorder [103], but with large $\xi(0)$, which renders it unusable in an $L = 3\ \mu$m wire. The condition that $\xi(0) < L$ is significantly more restrictive. As we shall see when we consider the case of a single disorder realization in Sec. II F, the condition that the gap not be too small is also more restrictive.

We estimate that the corresponding bound on the peak mobility (as a function of density) for Hall bar devices fabricated on the same material stack is $\mu_{2D} > 60\,000\ \text{cm}^2/\text{V s}$ at electron densities $n_e \sim 0.6$–$0.8\times10^{12}/\text{cm}^2$. The 2DEGs used in this paper have peak mobility in the range 60 000–100 000 $\text{cm}^2/\text{V s}$ in this density range. Additional details are in Appendix B.

In a similar fashion, we have optimized the design with respect to other disorder mechanisms including variations of the following parameters along the length of the wire: thickness and dielectric constant of the oxide, barrier thickness and composition, wire width, quantum well thickness, buffer composition and thickness. We have extracted these disorder parameters from measurements and used them in our simulations of topological gap devices. We have also taken into account disorder induced by imperfections in the substrate and as well as disorder resulting from inhomogeneous superconductor growth.

We now discuss how we have verified that these design, growth, and fabrication advances have led to superconductor-semiconductor nanowires with long localization length, as required for a topological phase. We have fabricated a variation on our topo gap device that has multiple junctions defining segments of different lengths, as we explain in more detail in Appendix C. This enables us to measure the nonlocal conductance for different segment lengths L and, thereby, extract the electron localization length ℓ_{loc} in the semiconductor. This device, shown in Fig. 27, was fabricated according to the same process as the DLG-δ topo gap device. We apply an in-plane magnetic field perpendicular to the wire $B \sim 1$ T to suppress the induced gap in all wire segments. Consequently, there is a signal in G_{RL} and G_{LR} at low bias. The junctions are operated in the open junction regime (see Fig. 6). The typical nonlocal conductance decays with length as $\sim\exp(-2L/\ell_{loc})$. For fitting our measured conductances to this form, we normalize it by the local conductances to reduce the effect of the junctions. From this fit we find that our gate-defined nanowires have localization length $\ell_{loc} \gtrsim 1\ \mu$m in the single-sub-band regime. Thus, the localization length ℓ_{loc} of electrons in the wire underneath the Al is much longer than the mean-free path of electrons in the Hall bar devices at a similar density due to screening of charged imperfections by Al in the former device type. This observation also confirms that the Al-2DEG interface is of high quality (i.e., the deposition of Al does not introduce new significant disorder mechanisms in our topo gap devices) and, thus, corroborates our disorder root-cause analysis discussed above.

Finally, we note, as a point of comparison to the previous works trying to realize topological superconductivity in quasi-one-dimensional nanowires [38], that "bottom-up" vapor-liquid-solid (VLS) nanowires have been measured with field-effect mobilities of 10^3–10^4 $\text{cm}^2/\text{V s}$ in InAs [105,106] and InSb [107] nanowires yielding localization lengths of 10–100 nm in the few sub-band regime. The origin of the dominant disorder mechanisms in VLS nanowires has not been established but is likely due to surface charged impurities. Thus, half-shell proximitized VLS nanowires are

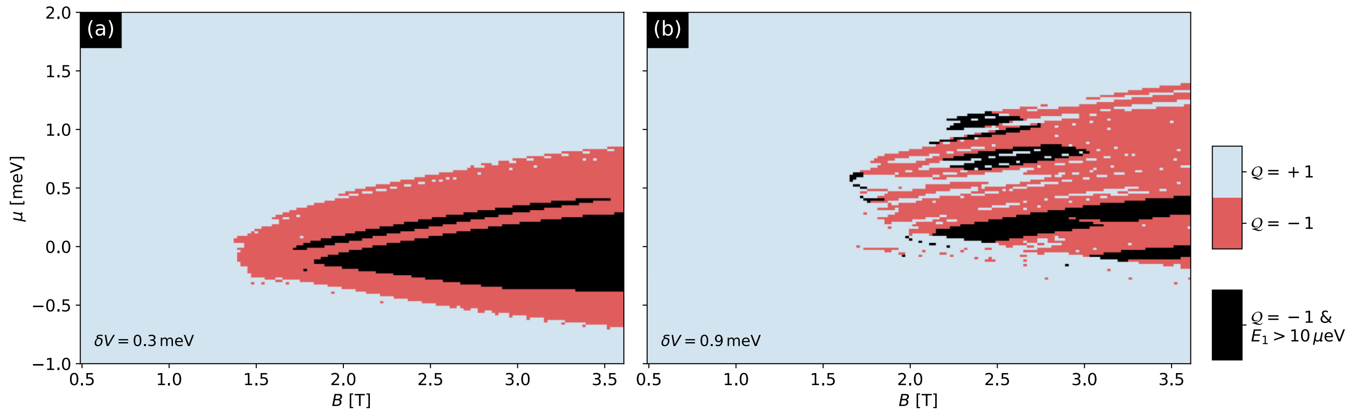

FIG. 7. Phase diagrams for a single disorder realization at $\delta V = 0.3$ and 0.9 meV, as a function of the magnetic field B and chemical potential μ for an $L = 3\,\mu$m wire with the ε stack single-band model parameters given in Table I. Blue represents the trivial phase and red is the topological phase, which is identified by the Pfaffian invariant $\mathcal{Q} = \pm 1$. Compared to the ideal topological phase in Fig. 1 and relatively weak disorder effect in (a), the lobe in (b) moves to higher values of μ and splinters as a result of increasing disorder, consistent with Fig. 24(b). A subset of the topological phase is highlighted in black, where the second lowest eigenvalue, representative of the gap, also has a high value. This more restrictive notion of topological region is even more "splintered" and prone to finite-size effects and mesoscopic fluctuations.

likely to have a much shorter localization length than the topo gap devices considered here. Field effect mobilities as high as 44 000 $cm^2/V\,s$ have been observed in stemless InSb nanowires [108]. It would be interesting to extract the corresponding localization length underneath a superconductor for such a nanowire by a measurement similar to that described above and in Appendix C. This can determine if topological superconductivity is possible.

F. Topological phase diagram for a single disorder realization

Even when a device satisfies the requirements explained in the previous subsection and has a topological phase, disorder can cause the shape of the phase diagram to be rather complicated. To gain a better understanding, it is helpful to examine the phase diagram for a few representative disorder realizations. In this section, we diagonalize the Hamiltonian in Eq. (A12) and calculate the Pfaffian topological invariant [9,99] for two independent disorder realizations. In any finite-sized system, the disorder-driven phase transition between the topological and trivial phases is rounded into a crossover. Consequently, a topological phase can be found in the phase diagram in some percentage of devices even for average disorder levels that exceed the critical value δV_c obtained in the thermodynamic limit. Conversely, some percentage of devices will not have a topological region of the phase diagram even for average disorder levels for which there would be a topological phase in the thermodynamic limit. Although disorder induces low-energy states (by creating domain walls between topological and nontopological regions, for instance) the density of such states may be low enough that an appreciable fraction of even reasonably long devices may not have any. Thus we can also characterize the phase diagram by the spectral gap in the $\mathcal{Q} = -1$ region, taken as the second-lowest eigenvalue E_1 of H (the lowest corresponds to the Majorana zero mode pair splitting).

In Fig. 7, we show the phase diagrams of two different simulated devices. Both have the DLG-ε design, but with two different disorder realizations, one with $\delta V = 0.3$ meV [Fig. 7(a)] and one with $\delta V = 0.9$ meV [Fig. 7(b)]. For weak disorder, the lobe structure of the topological phase is preserved, and the spectral gap remains high over a large region inside the lobe. For stronger disorder, mesoscopic fluctuations are important, as we discuss in Appendix A 3. The parabolic-shaped lobe of the topological phase of Fig. 1, as identified by the Pfaffian topological invariant $\mathcal{Q} = -1$, is splintered into several disconnected regions of narrow range in μ and larger extent in B. This effect is even more dramatic if we additionally condition on a large spectral gap (black regions in Fig. 7). We will call these long, narrow regions of topological phase *splinters* of the single-sub-band lobe.

There precise shape of these splinters varies from one disorder realization to the next. We expect such mesoscopic fluctuations in our devices. In Appendices A 2 and A 3, we will discuss disorder-averaged parameters, such as the localization length $\xi(E)$.

G. Statement on confidential information

In summary, the principles behind the design of our devices and material stacks are that they should enable three-terminal transport and (1) be based on a 2DEG residing in a low-defect quantum well; (2) have a charged defect density $n_{2D,int}$ at the semiconductor-dielectric interface that is less than $3\times10^{12}/cm^2$, as measured on a Hall bar on the same chip; (3) allow tuning to the lowest sub-band and full depletion of the wire; and (4) have an induced gap to parent gap ratio in the lowest sub-band that satisfies $0.33 < \Delta_{ind}/\Delta_{Al} < 0.67$. Hall bar measurements can be used to measure progress towards satisfying requirements (1) and (2); while zero-field transport measurements of topological gap devices (described in the next section) can be used to determine when (3) and (4) are satisfied. We present data from such measurements which directly verifies that the β, δ, δ', and ε material stacks in either SLG or DLG designs fulfill them.

The barrier thickness and composition, quantum well thickness, dielectric composition and deposition method, and Al strip width are critical factors that determine whether a

device meets these prerequisites. The details of these design parameters and fabrication methods are Microsoft intellectual property that we cannot disclose. However, we have explained the principles by which we determined these parameters and processes in this section (particularly Secs. II B, II C, and II E).

The following are some of the key ideas. We grow our superconductor-semiconductor heterostructure by molecular beam epitaxy on an insulating InP substrate. There is a graded buffer layer that modifies the lattice constant while preventing extended defects from reaching the active region [109]. In this regime, charged defects at the interface to the dielectric are the primary source of disorder. We have engineered the electron wave function in order to minimize the effective disorder level while maintaining a near-optimal induced gap in the semiconductor. In particular, we have varied the thickness of the InAs quantum well, t_{QW}, over the range 7 nm $< t_{QW} <$ 11 nm, and we have varied the thickness of an InAlAs barrier, t_B, over the range 4 nm $< t_B <$ 12 nm. These parameters have been optimized within these windows to maximize the distance from the active region to the dielectric while simultaneously targeting a gap ratio $\Delta_{ind}/\Delta_{Al} \approx 0.5$. We have chosen InAs for the quantum well because (a) its renormalized g-factor and spin-orbit coupling can reach the minimum required values of 4 and 4 meV nm, respectively; (b) there are known lattice-matched barriers; and (c) it has a larger temperature window for subsequent processing steps than alternative materials. We have chosen aluminum for the superconductor because it has demonstrated $2e$-periodic Coulomb blockade peaks, which is essential for the qubits that we discuss in Sec. VI, and it has a superconducting gap that is known to increase with decreasing thickness. The aluminum strip was chosen to be as wide as possible (in order to keep defects in the dielectric as far as possible from the active region in the quantum well) while still allowing full depletion of the wire at plunger gate voltages $V_p > -3$ V. Meanwhile, we have varied dielectric deposition conditions in order to find a process point at which $n_{2D,int} < 3\times10^{12}/\text{cm}^2$. Our devices can be reproduced through similar optimization steps, combining simulation and experimentation.

All of the key material and design parameters feed into the effective parameters given in Table I, together with δV and κ. They define the projected single-sub-band model in Eq. (A12) from which our simulations of bulk properties of our devices can be reproduced. Any device that replicates our design and material stack will have similar effective parameters.

III. TOPOLOGICAL GAP PROTOCOL

The goal of the TGP is to identify whether there are regions in the experimental parameter space that show signatures consistent with a topological phase. The full source code of the TGP and raw data sets are available in Ref. [98]. The device's outer sections are kept in the trivial superconducting phase by tuning their densities with the right and left plunger gates. In the topological phase of the wire, MZMs are localized at the boundaries between the topological and trivial sections [see Fig. 2(c)]. Provided that L is smaller than or, at least, not too much larger than the localization length $\xi(\Delta_T)$ (see Appendix A 3), there will also be an observed nonzero bulk transport gap. When this condition is satisfied,

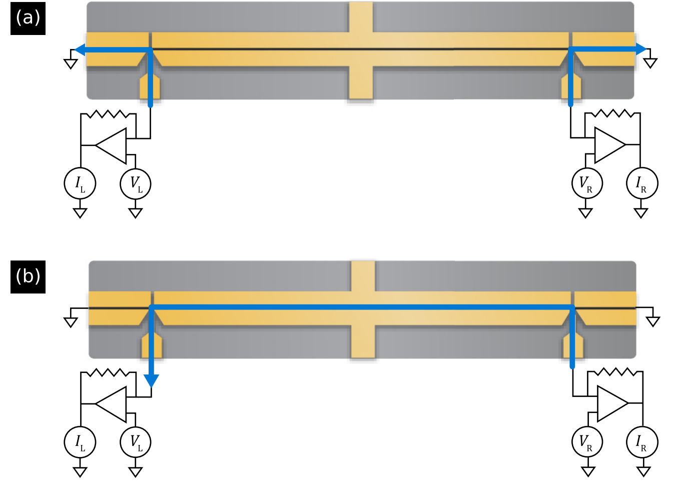

FIG. 8. Schematic illustrations of the current paths (blue arrows) that contribute to (a) G_{RR}, G_{LL} and (b) the nonlocal conductance G_{LR} discussed in Sec. III.

a nonzero above-gap nonlocal conductance is observable, enabling an identification of the gap, as we discuss further in Appendix A 3. In the TGP [8], the presence of MZMs and a bulk transport gap is detected by measuring the differential conductances

$$\begin{pmatrix} G_{LL} & G_{LR} \\ G_{RL} & G_{RR} \end{pmatrix} = \begin{pmatrix} dI_L/dV_L & dI_L/dV_R \\ dI_R/dV_L & dI_R/dV_R \end{pmatrix} \quad (2)$$

as a function of V_p and B as well as the voltages V_{rc}, V_{lc} controlling the tunnel junction transparencies, and the bias voltages $V_b = V_R, V_L$, which can be increased in order to tunnel current into states of higher energies. The currents and voltages I_R, I_L, V_R, V_L are illustrated in Fig. 8. We use the cutter gates to open and close the junctions; when V_{rc} is more negative, the junction is more closed, and similarly with V_{lc}. We discard all devices in which one of the junctions cannot be completely closed at a pinch-off voltage > -3 V. Even among devices that pass this basic health check, there is considerable device-to-device variation in the pinch-off voltages and, more generally, in the relation between V_{rc}, V_{lc} and the conductances through the junctions. This is, presumably, due to the different disorder configurations in the different junctions; these differences have a large effect because the junctions are depleted, leaving charged impurities unscreened, unlike in the bulk of the wire where the Al strip can suppress the effects of charged impurities via screening.

We want to vary the cutter gate voltages so that the local electrostatic environments at the two junctions change by enough to change the energy of bound states that are accidentally at zero energy for one cutter gate configuration. But since the cutter gate voltage change required to open or close a junction varies significantly from one junction to another as a result of disorder, we cannot simply choose the same sequence of V_{rc}, V_{lc} values for each device. Instead, we use the above-gap conductance G_N at $B = 0$ and a bias voltage of 500 μV as a measure of the junction transparencies. In each device, we find sequences of cutter gate voltages V_{rc}, V_{lc} for which G_N at both junctions take values between $\approx 0.1e^2/h$ and $\approx e^2/h$. They are slightly different in each device, but they

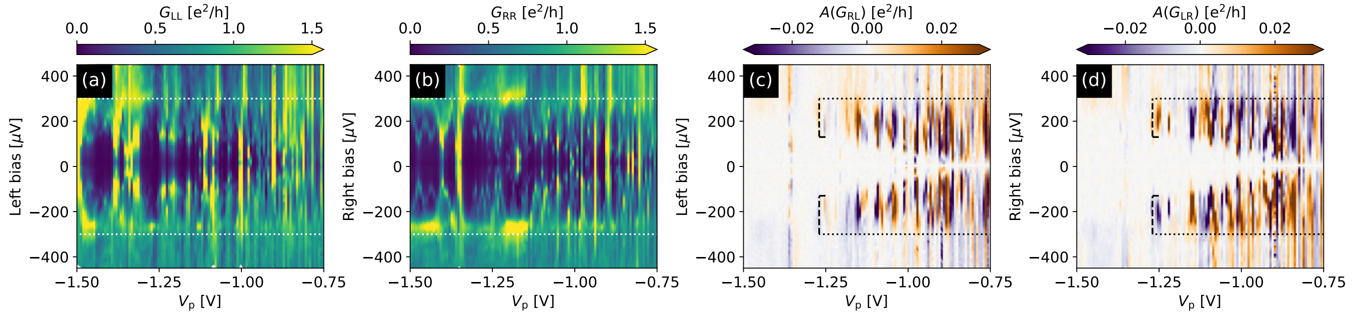

FIG. 9. The experimental local and antisymmetrized nonlocal conductances for device A at zero magnetic field as a function of plunger gate voltage V_p and bias voltage. The antisymmetrized nonlocal conductances in (c) and (d) are suppressed above the parent Al gap, which is indicated by horizontal dotted lines. They are nonvanishing down to small bias for V_p more positive than ≈ -0.9 V, which indicates that there is conduction through the region of the 2DEG that is not underneath the Al strip. This region of the 2DEG is depleted for V_p more negative than approximately -0.9 V. The antisymmetrized nonlocal conductances vanish for plunger gate voltages below $V_p \approx -1.27$ V, which we identify as the bottom of the lowest sub-band. For $-0.9 \text{ V} \lesssim V_p \lesssim -1.27$ V, the induced gap is indicated by a dashed curve which terminates in dashed vertical lines at the depletion voltage. The parent gap is visible in the local conductances in (a) and (b), but it is more challenging to identify the induced gap due to sub-gap states in the junctions.

always cover a substantial fraction of this range. When we say, as a shorthand, that we are varying the junction transparencies, we mean that we vary V_{rc}, V_{lc} in this manner.

In the tunneling regime (i.e., for $G_N < e^2/h$), the current paths contributing to G_{RR}, G_{LL} are illustrated in Fig. 8(a). In this regime, G_{RR} and G_{LL} directly measure the local density of states in the wire at the boundaries between the middle and, respectively, the right and left sections. ZBPs are determined by the condition that $-d^3I_R/dV_R^3$ exceeds the noise level and similarly for the left junction, i.e., the second derivative of the dI/dV curve is more negative than the noise level. ZBPs in G_{RR} and G_{LL} in the tunneling regime indicate the presence of zero-energy states in the wire with sufficient tunneling matrix elements to the leads, consistent with MZMs but also with trivial zero-energy Andreev bound states. A zero-energy state (either MZM or trivial ABS) at the right junction will be manifested as a ZBP in G_{RR} and similarly for a zero-energy state at the left junction and a ZBP in G_{LL}. Trivial ABS are not generically stable with respect to local perturbations whereas well-separated MZMs are. Therefore, the ZBP stability criterion, discussed below, allows one to better identify the region of interest.

The current path contributing to G_{LR} is illustrated in Fig. 8(b); G_{RL} is determined by the reverse path. For an intuitive understanding of G_{LR} and G_{RL}, we first note that in the thermodynamic limit of the wire, the clean limit, and the tunneling limit of both junctions, a current injected at bias voltage above the Al parent gap will flow through the Al strip to ground via the contacts at the ends of the device unless it relaxes to energies between the induced gap and the parent gap. Hence, at bias voltages above the Al parent gap, G_{RL} and G_{LR} are strongly suppressed and are nonzero only as a result of these weak relaxation processes [88,90,110]. At zero temperature, in the thermodynamic limit of the wire, the clean limit, and the tunneling limit of the junctions, current cannot be injected into the wire at bias voltages below the induced gap, except by Andreev processes, which inject supercurrent that also flows to the grounded contacts at the ends of the device. Now consider a finite-length disordered wire. At bias voltages at which the localization length $\xi(eV)$ is less than the length of the wire, G_{RL} and G_{LR} are strongly suppressed and are nonzero only as a result of nonzero temperature and finite ratio $L/\xi(eV)$. (In an infinite wire, G_{RL} and G_{LR} would vanish at all bias voltages because all states are localized, except precisely at the transition. For a further discussion, see Appendix A 3.) Consequently, the highest bias voltage below which G_{RL} and G_{LR} are nearly vanishing (in a sense that we make more precise below) can be interpreted as the transport gap Δ_{tr} that we define in Appendix A 3. As we discuss in Appendix D 1, we perform this gap extraction with the parts of the nonlocal conductances that are antisymmetric in bias voltage, $A(G_{RL})$, $A(G_{LR})$:

$$A[(G_{RL}(V_b)] \equiv [G_{RL}(V_b) - G_{RL}(-V_b)]/2 \tag{3}$$

and similarly for G_{LR}.

The high-dimensional nature of the parameter space that is explored by the TGP makes it prudent to narrow the measured parameter range. We explained above how the range of junction transparencies is limited. Meanwhile, the parameter range of V_p is chosen to be close to the bottom of the first sub-band. When the chemical potential is below the first sub-band, the wire is fully depleted. The depletion point is identified by scanning the nonlocal conductance as a function of bias and V_p. This can be done at $B = 0$ or at nonzero B, with B below the critical field of the superconductor, where the signal is generally larger. Recall that, as noted above, the nonlocal conductances are essentially zero outside the range of bias voltages between the induced and parent gaps, except for finite-size effects, thermal activation, and relaxation effects. Hence, full depletion of the wire causes the nonlocal conductance at bias voltages below the Al gap to drop below the noise floor. We use this depletion point to identify the single-sub-band regime.

In Fig. 9, we show the four elements of the experimentally measured conductance matrix as a function of bias voltage V_b and plunger gate voltage V_p at zero magnetic field in one of our devices, which we label device A, to illustrate how the depletion point is identified. As may be seen from Figs. 9(c) and 9(d), the antisymmetrized nonlocal conductances are small above the parent gap $\Delta_{Al} = 295 \pm 8$ μeV, which is indicated

by horizontal dotted lines in Figs. 9(c) and 9(d). The antisymmetrized nonlocal conductances are nonvanishing down to small bias for $V_\mathrm{p} \gtrsim -0.9$ V, which indicates that there is conduction through 2DEG regions not contacted by the Al for these plunger gate voltages. For V_p more negative than ≈ -0.9 V, these 2DEG regions are depleted, and the induced gap opens up. As discussed previously, the antisymmetrized nonlocal conductances are large between the induced and parent gaps, are suppressed above the parent Al gap, and are very strongly suppressed below the induced gap. As V_p is decreased further, the induced gap increases, eventually reaching its maximum measured value of $\Delta_\mathrm{ind} = 129 \pm 12$ μeV. At $V_\mathrm{p} \approx -1.25$ V, the antisymmetrized nonlocal signal drops sharply while local conductances remain large. For more negative V_p, the antisymmetrized nonlocal signal is very small, and there is no longer a visible bias range between the induced and parent gaps. This is interpreted as full depletion of the semiconductor below the Al strip. The single-sub-band regime occurs just before wire depletion.

In summary, the TGP makes the parameter space of our devices manageable by focusing on the most favorable region: V_p near the bottom of the lowest sub-band; B from zero up to 2.5 T; and a range of junction transparencies G_N between $\approx 0.1e^2/h$ and $\approx e^2/h$.

The steps of the TGP are divided into two stages. *Stage 1:* (1) From an analysis of G_RR and G_LL, identify ZBPs at each end of the wire that are stable to variations of the junction transparencies and variations in local junction potential (which are controlled by V_rc, V_lc in the manner discussed above). (2) Find clusters of points in the B-V_p plane where there are stable ZBPs at both ends of the wire. These clusters and their surrounding neighborhoods define the regions of interest ROI_1 that are the focus of Stage 2. If there are no such clusters, the device fails Stage 1.

Stage 2: (3) Focusing on smaller (B, V_p) ranges containing ROI_1s and restricting to cutter gate voltage pairs for which the junction transparency is approximately the same at both ends, confirm the existence of stable zero bias peaks in G_RR and G_LL and recover the clusters of points in the B-V_p plane where there are stable ZBPs at both ends of the wire. This step is important when there is a drift in V_p between Stages 1 and 2. The cutter voltages can either be set such that the junction transparencies are set on average to target conductance values, or compensated as a function of V_p such that the transparencies are stabilized to the target values. (4) Use $A(G_\mathrm{RL})$ and $A(G_\mathrm{LR})$ to determine the bulk energy gap as a function of (B, V_p) for each pair of cutter gate settings. (5) For each pair of cutter gate settings, find ZBP clusters identified in step 3 whose interiors are gapped and whose boundaries are gapless. We will denote them by $\mathcal{C}_i^A$ where i is a index for the pair of cutter gate settings and A is an index that distinguishes different gapped ZBP clusters with gapless boundaries that might occur for the same pair of cutter gate settings. (6) Find the sets of clusters T in the B-V_p plane consisting of $\mathcal{C}_i^A$ that overlap for different cutter gate settings. To be more precise, we define $T \equiv \{\mathcal{C}_i^A \,|\, \mathcal{C}_i^A \cap \mathcal{C}_j^B \neq \emptyset$ for some $j \neq i$ and $\bigcup \mathcal{C}_i^A$ connected$\}$. The device passes the TGP if there is a T such that there is a $\mathcal{C}_i^A \in T$ for a number of cutter gate settings i that exceeds some threshold, as we make more precise in Appendix D 2. In this case we define the region of interest $\mathrm{ROI}_2 = \bigcup_{\mathcal{C}_i^A \in T} \mathcal{C}_i^A$. Note that for a given device, there can be several T's and ROI_2s. We will call the clusters $\mathcal{C}_i^A \in T$ "subregions of interest SOI_2 belonging to a region of interest ROI_2."

Note that Stage 2 of the TGP typically uses 5 or fewer cutter gate values, chosen so that the above-gap conductance at each junction varies by $\sim e^2/h$ between the most closed and most open configuration. Stability of ZBPs to variation over a denser set of cutter gate values is neither necessary nor sufficient for passing the TGP. Further details are discussed in Appendix D.

There are a number of important measurement complexities that we discuss in Appendix D 1. The TGP is formulated with several thresholds which we explain in Appendix D 2: the minimum percentage of cutter gate settings for which a ZBP must be present in order to be considered stable, denoted by $(\mathrm{ZBP\%})_\mathrm{th}$; the minimum percentage of the boundary of a ZBP cluster that must be gapless in order for the whole boundary to be considered gapless, denoted by $(\mathrm{GB\%})_\mathrm{th}$; the conductance value below which we consider it to be effectively zero up to finite-size effects, denoted by G_th; and the minimum percentage of cutter gate settings for which an overlapping SOI_2 must be present in order to form an ROI_2, denoted by $(\mathcal{C}_i\%)_\mathrm{th}$.

The TGP captures the key physics of topological superconductivity because it requires a device to show stable ZBPs at both ends and also a bulk gap closing and reopening. However, we can make a much stronger quantitative statement about its reliability by testing it on simulated devices. We simulated 349 devices of different designs, material stacks, and disorder levels and applied the TGP to transport data from these devices. To test its reliability, we compared the ROI_2s located by the TGP with the "scattering invariant" [111], a topological index that is defined for open systems (see Appendix A 4 for a brief description of this invariant). When the topological index is -1 in some region of the phase diagram, the region is topological; when it is $+1$, the region is trivial. However, trivial regions of the phase diagram can exhibit relatively stable ZBPs in their transport data, and the TGP was designed to avoid misidentifying such regions as topological.

We classify ROI_2s as true positives (TP) if they contain any region with nontrivial topological index and as false positives (FP) otherwise. The false discovery rate (FDR) is the probability that an ROI_2 is trivial:

$$\begin{aligned} \mathrm{FDR} &\equiv P(\,\mathrm{ROI}_2 \text{ is trivial}) \\ &= \lim_{N\to\infty} \mathrm{FP}/(\mathrm{FP}+\mathrm{TP}), \end{aligned} \tag{4}$$

where N is the total number of devices. In essence, the FDR is the probability that if a device passes the TGP then the ROI_2 that it identifies has a completely trivial explanation, such as a trivial ABS. We estimate the FDR from the TP and FP numbers obtained from a large, but finite, number of simulated devices. As $N \to \infty$, the ratio $\mathrm{FP}/(\mathrm{FP}+\mathrm{TP})$ approaches the FDR. For finite N, the best that we can do is estimate upper and lower bounds on the FDR. We use the Clopper-Pearson confidence interval at the 95% confidence level to estimate these bounds.

Our results are shown in Table II. Since we found no false positives, the confidence interval for the FDR is between zero and the upper bound that we list in the rightmost column. We find that if a device passes the TGP, there is a $<8\%$ probability

TABLE II. Statistics of TGP results for simulated transport data from SLG-β and DLG-ε devices with 50 different disorder realizations for each of the average disorder strengths given in the first column. Devices with $n_{\mathrm{2D,int}} \leqslant 10^{12}/\mathrm{cm}^2$ typically have multiple distinct ROI$_2$s, so we have more total ROI$_2$s for low disorder. The listed range of FDR values is the confidence interval at the 95% confidence level.

Design, stack	$n_{\mathrm{2D,int}}$ [$10^{12}/\mathrm{cm}^2$]	TP	FP	FDR
SLG-β	1.0	244	0	<1.5
	2.7	46	0	<7.7
	4.0	45	0	<7.9
DLG-ε	0.1	125	0	<2.9
	1.0	97	0	<3.7
	2.7	67	0	<5.4
	4.0	66	0	<5.4

that the ROI$_2$ that it finds does not contain a topological phase, provided that the simulated data are drawn from the same probability distribution as the data produced by real devices. For the DLG-ε design, the probability is <6%. We simulated several different disorder levels to investigate whether the TGP is more likely to give false positives when disorder is higher. Our results indicate that the TGP is reliable over the entire range $n_{\mathrm{2D,int}} = 0.1\text{–}4\times10^{12}/\mathrm{cm}^2$, which is the range of charged disorder levels in the measured devices discussed in Sec. IV.[1] Similarly, the differences between the SLG-β and DLG-ε stacks and designs have no effect on the accuracy of the TGP. The small dependence of our FDR estimates on disorder level and design that may be seen in Table II are entirely a consequence of the different numbers of ROI$_2$s that were found at different disorder levels. Further details are given in Appendix E. As we discuss in Sec. V, the statistical properties of the ROI$_2$s that we find in our simulations agree with the corresponding experimental values, thereby further validating the simulation model used to estimate the FDR. This analysis addresses open questions regarding the reliability of the TGP [112].

IV. EXPERIMENTAL DATA

A. Measurements of device A

In the remainder of this paper, we focus on measurements of devices such as the one shown in Fig. 2. In this section, we focus on data from device A, which is a 3 μm long SLG device built on a β stack. We discuss three experimental measurements from this device. The raw data are available in Ref. [98]. Measurement A1 was taken in one dilution refrigerator while measurements A2 and A3 were taken in a different cooldown of device A in a different dilution refrigerator. The measured zero-field superconducting gap in the Al strip is $\Delta_{\mathrm{Al}} = 295 \pm 8$ μeV and the maximum induced gap at zero B field is $\Delta_{\mathrm{ind}} = 129 \pm 12$ μeV, which indicates that the induced gap to parent gap ratio $\Delta_{\mathrm{ind}}/\Delta_{\mathrm{Al}} = 0.44$ is well within the desired range.[2] The effective charged impurity density at the interface with the dielectric is $n_{\mathrm{2D,int}} = 2.7\times10^{12}/\mathrm{cm}^2$, as is discussed in Appendix B. This value satisfies the specification explained in Sec. II E, which is based on the assumption that the average charged impurity density at the dielectric-semiconductor interface in the Hall bar is the same as at the dielectric-semiconductor interface in a topological gap device [the boundary between light blue and gray on either side of the Al strip in Fig. 2(d)] on the same chip. The critical field, B_{c}, for the thin Al strip is >4.5 T for magnetic fields in the direction of the strip. The single-sub-band regime, as determined from the nonlocal conductance in the same manner as in Fig. 9, is reached at V_{p} between -1.2 and -1.4 V (depending on the cooldown). This is consistent with our simulations for device A (see Fig. 4). The base temperature in our measurements is ∼20 mK and, using NIS thermometry [113], we measured an electron temperature $T_{\mathrm{e}} < 40$ mK.

1. TGP Stage 1

We begin by finding the single-sub-band regime, following the method discussed in Appendix D 1. The nonlocal signal below the Al parent gap vanishes for $V_{\mathrm{p}} < -1.18$ V, which we interpret as the point at which the wire is fully depleted. We focus our Stage 1 scans on a V_{p} range of 30 mV above this value.

In Figs. 10(a) and 10(b), we show the cutter gate fraction for ZBPs at, respectively, the left and right junctions as a function of B and V_{p}. The black lines in Figs. 10(a) and 10(b) enclose the regions in which the cutter gate fraction for ZBPs at the left or right junction is greater than >70%. Finally, in Fig. 10(c), we show the fraction of junction transparencies at which there are ZBPs at both junctions, plotted as a function of B and V_{p}. The black line indicates the part of the phase diagram where the cutter gate fraction for ZBPs at both junctions is >70%.

Stage 1 data were taken for 21 different cutter gate voltages at each junction, chosen such that G_N at each junction is in the range 0.01 to $0.85e^2/h$. These 21 cutter voltages were found by the following procedure including a calibration measurement prior to the TGP Stage 1 (TGP1) measurement. 21 targets for G_N were chosen as equidistant points in the range 0.01 to $0.85e^2/h$. The change of local potential corresponding to this conductance change is estimated to be a few meVs. In the calibration measurement, the cutter voltage for each junction yielding each of the 21 targets (within $\pm\, 0.02e^2/h$) was recorded at 61 equidistant points along the plunger voltage range V_p to be used in TGP1. For each G_N target, the median cutter voltage along the plunger voltage axis is chosen as the cutter voltage for that G_N target. This procedure returned the 21 cutter voltages for each junction. Each of the 21 cutter voltage pairs used in TGP1 is a pair in which each of the voltages is drawn with no replacement from this list.

In Stage 1, we find (B, V_{p}) values at which there are ZBPs at both junctions for more than 15 out of 21 (V_{lc}, V_{rc}) pairs or,

[1]Note that the threshold G_{th} depends on the level of disorder in the system and is taken differently at $0.1\times10^{12}/\mathrm{cm}^2$ charged disorder compared to the other cases. See Appendices E 2 and E 3 for details.

[2]For the extraction of the zero-field induced gap, see Fig. 36.

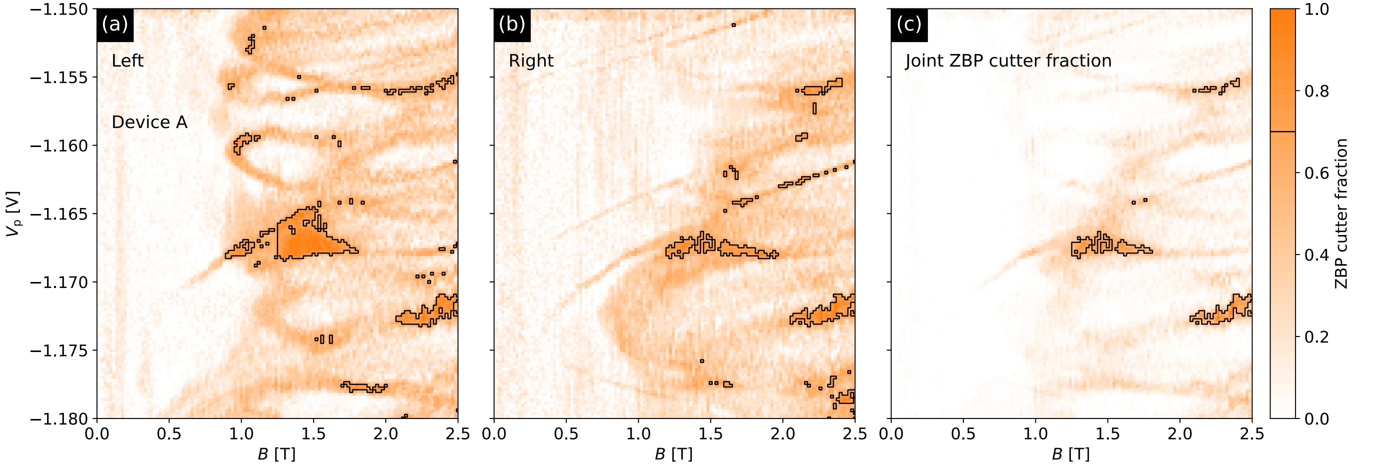

FIG. 10. Experimental ZBPs for device A, measurement A1, Stage 1 identifying ROI_1 for Fig. 11. (a) The cutter gate fraction for which there is a ZBP at the left junction as a function of B and V_p. (The color scale is at the far right.) (b) The cutter gate fraction for ZBPs at the right junction as a function of B and V_p. (c) The cutter gate fraction for ZBPs at both junctions. In all three panels, regions for which the cutter gate fraction for ZBPs is at least 70% are surrounded by black lines. The cutter gate fractions for ZBP are defined in the third paragraph of Sec. IV A 1. ZBPs that occur at only one junction or for a small cutter gate fraction are likely to be due to trivial Andreev bound states. The data and scripts needed to reproduce this and other experimental figures are available in Ref. [98].

in other words, for which the cutter gate fraction for ZBPs at both junctions is >70%. Clusters of such points are the candidate regions of topological phase yielded by Stage 1 of the TGP, dubbed ROI_1 in Ref. [8].

There are several key features in Fig. 10 worth emphasizing. First, we expect that the topological phase in proximitized nanowires should have a lobelike shape $|g^\star|\mu_B B/2 > \sqrt{\mu^2 + \Delta_{\mathrm{ind}}^2}$ in the absence of disorder. As a result of disorder, we expect the lobe to be splintered, as shown in the simulations in Fig. 7. In Stage 1 data from simulated device R1, this manifested as splintered regions in which there are stable ZBPs at both ends of the device, as may be seen in Fig. 30. The 30 mV field of view in Fig. 10 corresponds to a single lobe, which we identify as the lowest sub-band according to the method discussed in Appendix D 1. The structure that is visible in the phase space locations of stable ZBPs at the left and right junctions and, especially, in ROI_1 resembles the splintering of the lobe.

We have observed very similar ROI_1s in several devices (such as devices B, C, D, and E). In more disordered devices (such as device F, which is discussed in Sec. IV B), ZBPs are scattered throughout phase space, and there is no structure, which suggests a nontopological phase of matter.

The data are reproducible between successive measurement runs on the same device, as we show in Sec. IV A 3. The system is very stable, provided that V_p is varied by 30 mV or less. If the voltage is varied by more than 100 mV, features shift in V_p but we can recover the same ROI_1. If a device idles for approximately a week near an ROI_1, we find that voltages drift by at most a few mV, as we will see when we compare measurements A2 and A3.

We emphasize that the main goal of Stage 1 is to identify promising regions in parameter space for measurements of both the local and nonlocal conductances over a range of bias voltages, which are the focus of Stage 2.

2. TGP Stage 2: Measurement A1

In Stage 2, we focus on the regions of the B-V_p plane where there are clusters of points with stable ZBPs at both junctions. We map out the full conductance matrix Eq. (2) as a function of B, V_p, V_{lc}, V_{rc}, and, in addition, V_b. Since we are now exploring a higher-dimensional parameter space, we restrict the V_p sweep to the vicinity of ROI_1 identified in Stage 1, which is typically $\delta V_p \approx 5$–15 mV. We further restrict the parameter space by taking scans for 3–5 pairs of cutter gate settings (rather than the >20 pairs of Stage 1). For each pair of cutter settings, the cutters are compensated as a function of V_p to achieve the target G_N values at each side. In the measurement of device A displayed in Fig. 11, there were 3 cutter gate pairs $(V_{lc}(V_p), V_{rc}(V_p))$. These cutter gate settings correspond to G_N targets of 0.3, 0.5, and $0.7e^2/h$ at both junctions. In Fig. 11, we show data for the representative cutter gate settings for which $G_N = 0.3e^2/h$ for both junctions and the discussion below focuses on these data. Qualitatively similar observations hold for the other two settings.

Since, as was previously mentioned, there is typically a small voltage drift between Stages 1 and 2, we start the analysis of the Stage 2 data by determining the regions with stable zero-bias peaks anew. We call the ZBPs stable if they are present for at least 2 out of 3 cutter gate settings. In Figs. 11(c) and 11(d), we illustrate ZBPs for our representative cutter gate setting by showing G_{LL} and G_{RR} for $V_p = -1.171\,75$ V. In Fig. 11(b), we see that the corresponding horizontal line passes through a region with stable ZBPs, indicating that these ZBPs are present at least one other cutter gate setting as well. The G_{LL} and G_{RR} data shown in Figs. 11(c) and 11(d) are displayed as "waterfall" plots in Figs. 11(g) and 11(h), which is an alternate but equivalent method of representing the same data. We reemphasize that the conductances G_{RR}, G_{LL} are not topological invariants and are not expected to have quantized values at nonzero temperature and nonzero junction

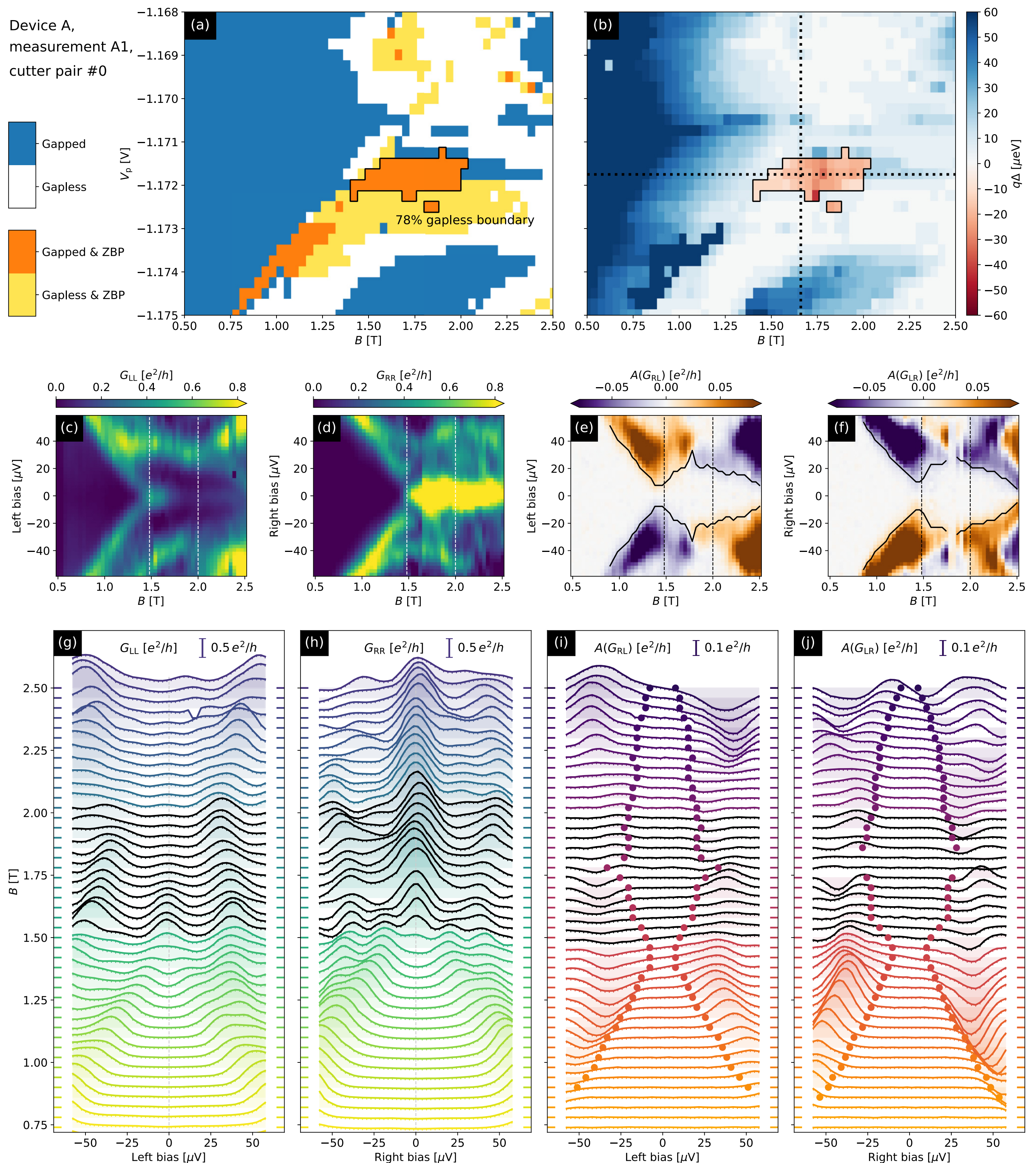

FIG. 11. (a) The experimental phase diagram of device A (measurement A1) in the color scheme shown at the left. The stability of ZBPs is determined by varying the cutter gates so that for both junctions G_N takes the values 0.3, 0.5, and $0.7e^2/h$ (cutter pairs #0, #1, and #2, correspondingly). The boundary of the SOI_2 is interpreted as a phase transition line, consistent with a visible gap closure along 78% of it. (b) The experimental phase diagram, showing trivial/topological phases, which the TGP identifies with the exterior/interior ($q = \pm 1$) of the SOI_2. The color scale shows the size of the trivial (positive sign) or topological (negative sign) gap. The protocol assigns a maximum topological gap $\Delta_{\rm topo}^{\rm max} = 23$ µeV. Measured local and antisymmetrized nonlocal conductances along the horizontal line in (b) at $V_p = -1.171\,75$ V: (c) G_{LL}, (d) G_{RR}, (e) $A(G_{RL})$, (f) $A(G_{LR})$. The SOI_2 lies between the vertical lines. Panels (g)–(j) are "waterfall" plots representing the same measured data. The data shown in (c)–(j) were obtained for $G_N \approx 0.3e^2/h$ for both sides (we call it cutter pair #0). The black curves in (e) and (f) and the dots in (i) and (j) are *not* guides to the eye; they indicate where the nonlocal signal drops below a threshold value, as described in the text. The analysis of cutter pairs #1 and #2 is shown in Figs. 33 and 34.

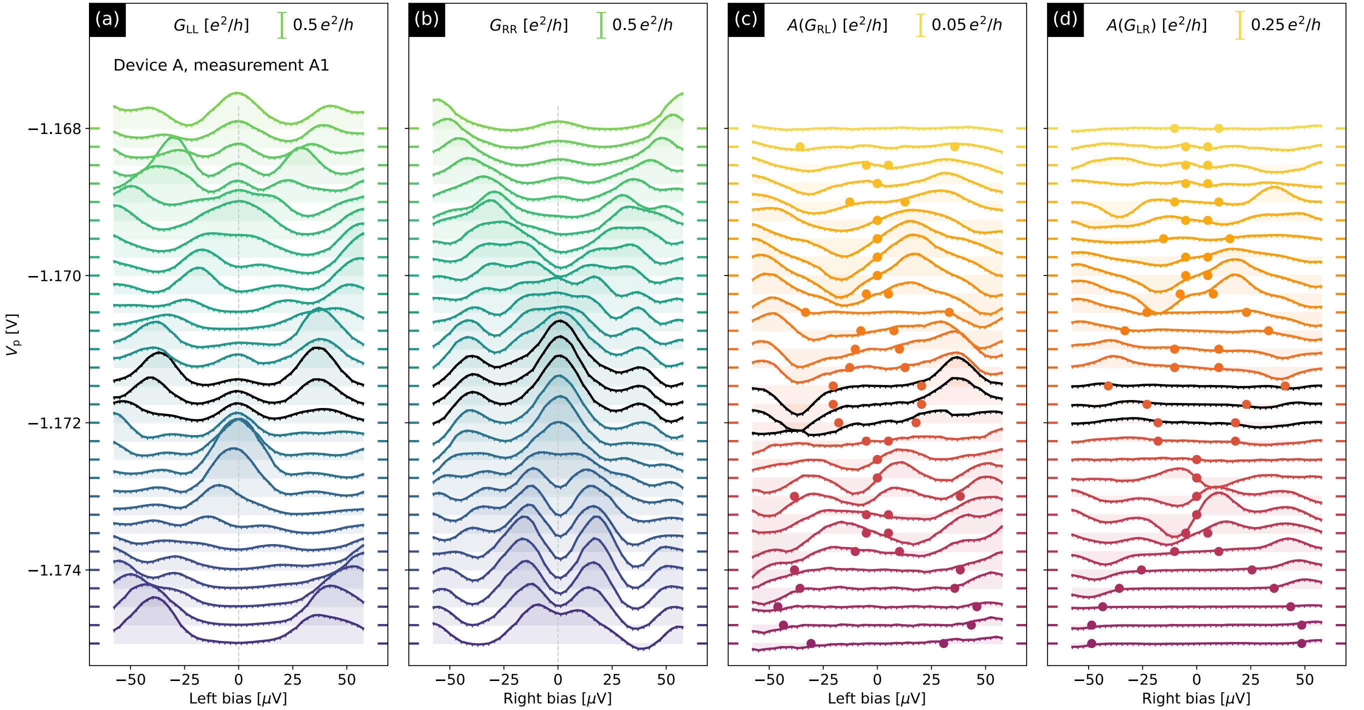

FIG. 12. "Waterfall" conductance plots of (a) G_{LL}, (b) G_{RR}, (c) $A(G_{RL})$, (d) $A(G_{LR})$ as a function of the corresponding bias and plunger gate voltage V_p for device A (measurement A1). The data are the $B = 1.66$ T vertical line in Fig. 11(b). ZBPs and extracted gap points corresponding to SOI_2 are shown in black.

transparency. So a ZBP, no matter how stable or well quantized, cannot prove that the system is in a topological phase. Conversely, the existence of a topological phase in a device is not disproven by a ZBP that has a small magnitude, such as the ZBPs at the left junction in Figs. 11(c) and 11(g). In the TGP, we classify ZBPs by their stability to parameter changes. In particular, ZBPs that are stable with respect to changes of the cutter gate voltages are a mandatory requirement of the TGP. We give an example from a Stage 2 measurement in Fig. 15.

Next, we use bias scans of the nonlocal conductances $A(G_{RL})$, $A(G_{LR})$ to determine the bulk transport gap at each point in the phase diagram. We illustrate this in Figs. 11(e) and 11(f), where we show $A(G_{RL})$ and $A(G_{LR})$ as a function of B at the $V_p = -1.171\,75$ V horizontal line in Fig. 11(b). The black curves in Figs. 11(e) and 11(f) show the transport gap extracted from, respectively, G_{RL} or G_{LR} as a function of B for this V_p value. The black curves are determined according to the procedure explained in Appendix D 1. The transport gap is obtained by taking the minimum of the values extracted from $A(G_{RL})$ and $A(G_{LR})$. There is a clear bulk transport gap closing and reopening visible in $A(G_{RL})$ at $B \approx 1.5$ T. The gap remains open from $B \approx 1.5$ T to $B \approx 2.5$ T.

We further illustrate the behavior of $A(G_{RL})$, $A(G_{LR})$ by taking a vertical cut through the B-V_p plane. In Fig. 12, we show waterfall plots of local and nonlocal conductances as a function of V_p at fixed $B = 1.66$ T. The black dots in Figs. 12(c) and 12(d) indicate the bulk transport gaps extracted from G_{RL} and G_{LR}. A gap closing and reopening is clearly visible in these plots. We emphasize that these cuts through the phase diagram are a very small sample of the data comprising Stage 2 of measurement A1.

While these illustrative cuts are highly enlightening, they are not the primary goal of Stage 2 of the TGP, which is to derive an experimental phase diagram from the measured conductance matrix as a function of B, V_p, V_{lc}, V_{rc}, and V_b. The TGP yields the experimental phase diagrams in Figs. 11(a) and 11(b) for our representative cutter gate setting. All three cutter gate settings yield similar phase diagrams. The color scheme in Figs. 11(a) and 11(b) is the same as in the simulated phase diagrams in Figs. 31(a) and 31(b). The most salient feature of Figs. 31(a) and 31(b) is the presence of an SOI_2. In this region, there are stable ZBPs at both ends of the device, and there is a nonzero bulk transport gap; 78% of the boundary of this region in the B-V_p plane is gapless. Device A passed the TGP.

The crucial point of the TGP is to not rely on a single feature to identify a topological phase, but instead to rely on the totality of the data to provide evidence for the observation of a topological phase. Indeed, each pixel in Fig. 11(b) is determined by conductance data in a neighborhood of points around that pixel and for a range of cutter gate settings.

From $A(G_{RL})$, $A(G_{LR})$, we infer a bulk gap closing and reopening, which is a signature of a second-order phase transition. It is important to distinguish such behavior in the nonlocal conductances $A(G_{RL})$, $A(G_{LR})$ from apparent gap closings/reopenings in the local conductances G_{RR}, G_{LL}, which could easily be the motion of a local state towards zero energy, rather than a bulk phenomenon.

This phase transition line separates the high-field gapped phase from the gapped trivial superconducting phase that is present at low fields. It does not quite surround the high-field gapped phase: 78% of the boundary shows a gap closing in

$A(G_{RL})$, $A(G_{LR})$. This surpasses $(\mathrm{GB}\%)_{\mathrm{th}}$; it is similar to the percentage of the boundary of the SOI_2 that is gapless in the simulated data of Fig. 31 and is typical for simulations of this device design and disorder level. Consequently, we believe that the second-order phase transition line that surrounds 78% of our putative topological phase is, in fact, part of an unbroken transition line surrounding the entire phase. As noted in our discussion of $(\mathrm{GB}\%)_{\mathrm{th}}$ in Appendix D 2, one possibility is that the gap closing is not visible along 22% of the boundary of the SOI_2 due to a suppression of the signal by disorder/nonuniformity while another is that the topological region is larger than the SOI_2. Indeed, for the cutter gate setting shown in Fig. 11, there are ZBPs at both junctions up to $B = 2.5$ T.[3] However, at the other cutter gate settings, there is no visible ZBP at the left junction.

The high-field gapped phase is characterized by stable ZBPs at both ends of the wire, which is consistent with the topological phase. For some V_p values, the ZBPs appear before the gap reopens, including at the $V_p = -1.171\,75$ V horizontal line in Fig. 11(b). This is consistent with a scenario in which quasi-MZMs [46–51] are precursors to the transition into the topological phase, which is frequently seen in simulations.

The maximum topological gap is $\Delta_{\mathrm{topo}}^{\mathrm{max}} = 23$ μeV for this cutter gate setting.[4] Over the SOI_2, which has an extent of $\delta B \approx 500$ mT, $\delta V_p \approx 1.5$ mV, the extracted topological gap increases from zero to $\Delta_{\mathrm{topo}}^{\mathrm{max}}$ in such a way that its median value over the region within the black line in Figs. 11(a) and 11(b) is 20 μeV. From the phase diagram in Figs. 11(a) and 11(b), we see that the lowest field at which the gap closes near the SOI_2 is ≈0.8 T, which implies an effective g-factor of at least $|g_{\mathrm{eff}}| \approx 5.6$. Here, we define $|g_{\mathrm{eff}}| \equiv 2\Delta_{\mathrm{ind}}/\mu_B B_{\mathrm{min}}$, where B_{min} is the lowest field at which the gap closes.[5] This value of $|g_{\mathrm{eff}}|$ is close to the optimal value for this device design and material stack.

The induced gap (and all structures associated with its closing/reopening) decreases rapidly when the magnetic field is rotated away from the direction of the wire, as expected. The transition to the topological phase should become more smeared as the temperature is increased, but it is difficult to study this systematically due to voltage drifts.

Comparing the experimental data in Fig. 11 to the simulated data in Fig. 31, we note both the qualitative and quantitative similarity between the phase diagrams. In both simulated and measured data, there are gap closings at similar V_p-dependent B-field values, and the extent of both the gapless regions and the SOI_2s are of similar size in the B-V_p plane. However, we emphasize again that the main role of simulated data such as that shown in Fig. 31 is to test the TGP on (simulated) devices for which we know the phase diagram and not to reproduce the experimental phase diagram.

3. Reproducibility of the data: Measurements A2 and A3

We now present experimental data from a different cooldown in which measurements A2 and A3 were performed one week apart. These measurements produced similar data sets, both passing the TGP, indicating the reproducibility of our data and the device's stability from one measurement run to another. Both of these data sets are consistent with measurement A1 shown in Sec. IV A.

In our simulations, we saw that devices can pass the TGP for some disorder configurations but not others. Each cooldown typically leads to a somewhat different disorder configuration, resulting, for example, in a shift of the gate voltages at which we see the depletion of the lowest sub-band. As mentioned previously, when the device idles for a week, the disorder configuration can also drift slightly. Hence, we expect that the same device will pass the TGP in some measurements but not in other measurements occurring a week or more apart or in different cooldowns. This was the case with device A. It regularly passed the TGP, but also failed sometimes. In this subsection, we focus on measurements A2 and A3, in which device A passed the TGP with a topological phase that shifted in parameter space. For measurement A2, device A was warmed up, removed from the dilution refrigerator in which A1 was performed, cooled down in a different dilution refrigerator, and remeasured. In accordance with the TGP, we performed Stage 1 measurements and identified an ROI_1 with stable ZBPs near $V_p = -1.4$ V. The results of the subsequent Stage 2 measurement are shown in Fig. 13.

The phase diagrams in Figs. 13(a) and 13(b) have the same basic features as those in Figs. 11(a) and 11(b). The primary differences are as follows. The lowest gap closing point in A2 is slightly lower in field than in A1, leading to an effective g-factor of $|g_{\mathrm{eff}}| \approx 6.4$. The topological phase starts at lower fields, close to 0.8 T, which is closer to the lowest fields at which the gap closes than in A1, and it extends over a larger range of plunger gate voltages, $\delta V_p = 2.5$ mV but a similar magnetic field range $\delta B \approx 500$ mT. The maximum topological gap in measurement A2 is $\Delta_{\mathrm{topo}}^{\mathrm{max}} = 29$ μeV [see Fig. 13(b)], which is the largest observed for device A, and the percentage of the boundary that is gapless is 80%. The local conductances are shown in Figs. 13(c) and 13(d). In addition to ZBPs, there is also a strong local resonance at the right junction which is evident in Fig. 13(d). However, this resonance moves away from zero bias as B is increased. Furthermore, this resonance disappears in the subsequent measurement shown in Fig. 14(d), indicating that this is an accidental feature due to an impurity that moved between measurements A2 and A3. This trivial resonance partially obscures the stable ZBP, which has a smaller amplitude.

In Fig. 14, we show measurement A3 which was performed in the same cooldown as measurement A2 but one week later. The electrostatic environment of the system drifted by 2–3

[3] At the left junction, this ZBP is small, but above the measurement resolution, as may be seen in Figs. 11(c) and 11(g).

[4] The extracted gap can depend on the cutter gate setting. Stability of the gap extraction with respect to cutter gate setting is not a requirement of the TGP.

[5] Here we define the effective g-factor as the average slope of the extracted induced gap vs B field. This is different from the conventional definition of the spin g-factor in terms of dE/dB at $k = 0$. The former depends on spin-orbit coupling and orbital physics whereas the latter does not. However, in the single-sub-band regime, where the lowest energy state has momentum close to $k = 0$, both the orbital effect of the B field and spin-orbit coupling effects are small. In this case, $|g_{\mathrm{eff}}|$ is a good proxy for $|g^\star|$.

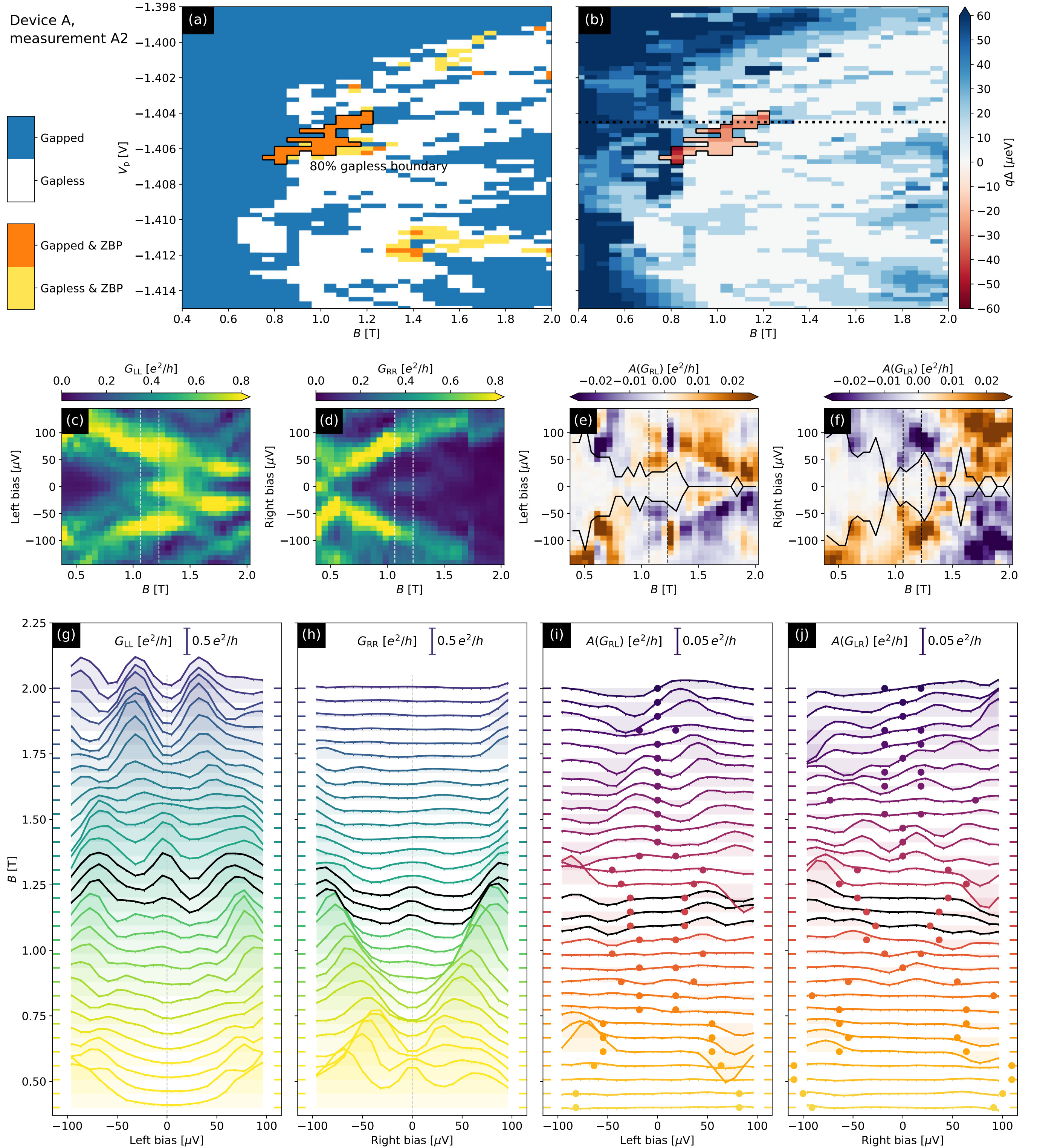

FIG. 13. (a) The experimental phase diagram of device A (measurement A2) that results from combining the clusters of stable ZBPs at both junctions with the map of the locus of zero/nonzero gap. The stability of ZBPs is determined by varying the cutter gate settings so that for both junctions G_N take the values 0.3, 0.5, 0.7, and $0.9e^2/h$. The boundary of the SOI_2 is interpreted as a phase transition line, consistent with a visible gap closure along 80% of it. (b) The experimental phase diagram, showing trivial/topological phases, which the TGP identifies with the exterior/interior ($q = \pm 1$) of the SOI_2. The color scale shows the size of the trivial (positive sign) or topological (negative sign) gap. The protocol assigns a maximum topological gap $\Delta_{topo}^{max} = 29$ μeV. Measured local and antisymmetrized nonlocal conductances along the horizontal line in (b) at $V_p = -1.4045$ V: (c) G_{LL}, (d) G_{RR}, (e) $A(G_{RL})$, (f) $A(G_{LR})$. The SOI_2 lies between the vertical lines. Panels (g)–(j) are "waterfall" plots representing the same measured data. The data shown in (c)–(j) were obtained for left (right) $G_N \approx 0.5e^2/h$ ($\approx 0.8e^2/h$). The black curves in (e) and (f) and the dots in (i) and (j) indicate where the nonlocal signal drops below a threshold value, as described in the text.

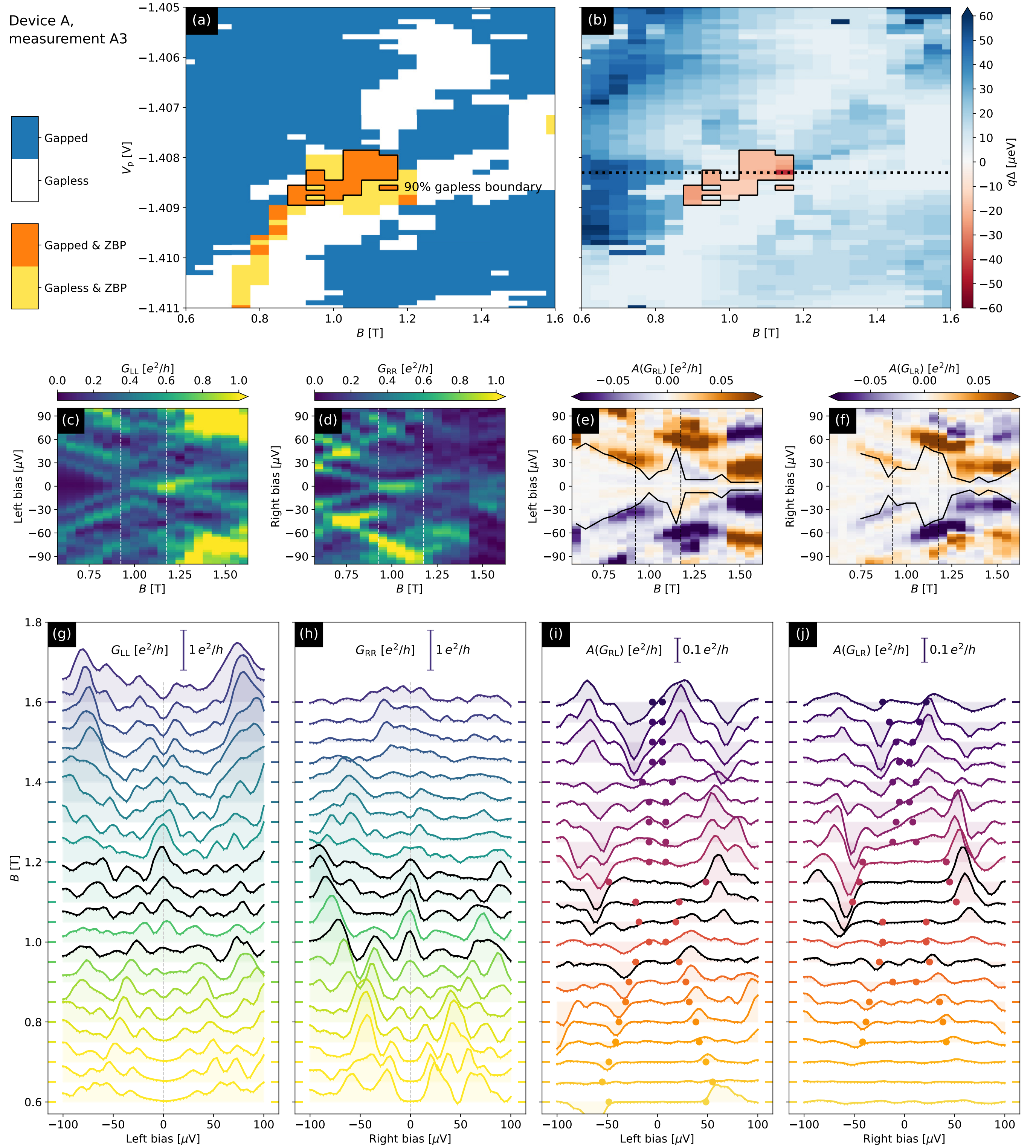

FIG. 14. (a) The experimental phase diagram of device A (measurement A3) that results from combining the clusters of stable ZBPs at both junctions with the map of the locus of zero/nonzero gap. The stability of ZBPs is determined by varying the cutter gate settings so that for both junctions G_N take four values between 0.3 and $0.8e^2/h$ at $B = 0$. The boundary of the SOI_2 is interpreted as a phase transition line, consistent with a visible gap closure along 90% of it. (b) The experimental phase diagram, showing trivial/topological phases, which the TGP identifies with the exterior/interior ($q = \pm 1$) of the SOI_2. The color scale shows the size of the trivial (positive sign) or topological (negative sign) gap. The protocol assigns a maximum topological gap of $\Delta_{\rm topo}^{\rm max} = 22$ μeV. Measured local and antisymmetrized nonlocal conductances along the horizontal line in (b) at $V_p = -1.4083$ V: (c) G_{LL}, (d) G_{RR}, (e) $A(G_{RL})$, (f) $A(G_{LR})$. The SOI_2 lies between the vertical lines. Panels (g)–(j) are "waterfall" plots representing the same measured data. The data shown in (c)–(j) were obtained for left (right) $G_N \approx 0.6e^2/h$ ($\approx 0.4e^2/h$). The black curves in (e) and (f) and the dots in (i) and (j) indicate where the nonlocal signal drops below a threshold value, as described in the text.

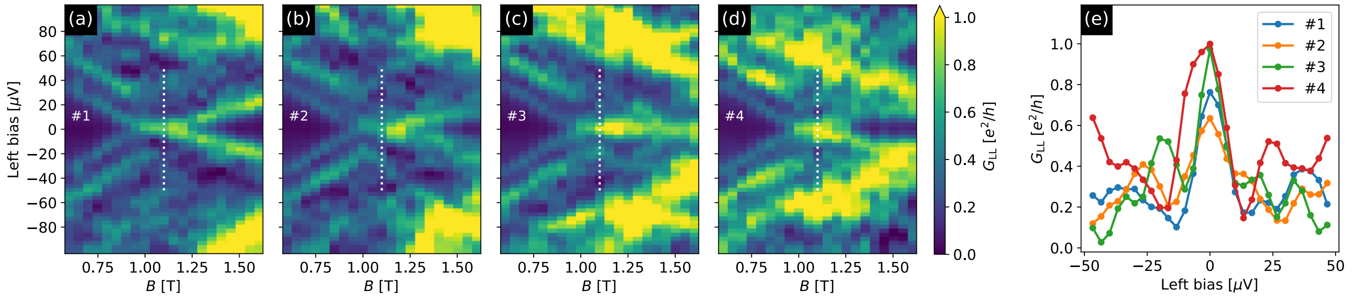

FIG. 15. (a)–(d) Bias-field cuts of measurement A3 at $V_p = -1.4083$ V. G_{LL} is shown for 4 different left cutter gate settings #1–#4 corresponding, respectively, to G_N of approximately 0.5, 0.6, 0.7, and $0.8e^2/h$. Panel (b) for cutter #2 shows the same data as Fig. 14(c). (e) Line-cut at $B = 1.1$ T for the above cutter gate settings. The chosen values of B and V_p lie within the SOI_2 shown in Fig. 14(b) for left and right cutters corresponding to G_N 0.6 and $0.4e^2/h$, respectively. Note that the ZBP height is of the order of e^2/h for all left cutter gate settings.

mV during the week between the two measurement runs, as is typically the case in our devices. However, the main qualitative features are reproduced from one run to the next: there is a topological phase with a comparable critical field and similar overall shape. The size of the maximum topological gap has decreased from its value in A2 to $\Delta_{\rm topo}^{\rm max} = 22$ μeV, which is close to value found in measurement A1.

Finally, we discuss the stability of ZBPs with respect to local perturbations. In Figs. 14(c) and 14(d) one can see stable ZBPs at both junctions over a magnetic field range $\delta B \approx 0.5$ T. They are similarly stable with respect to changes in V_p, as may be seen from the vertical extent of the orange region in Fig. 14(a). These peaks are also stable with respect to cutter changes modulating the transparency of the junctions, as we show in Fig. 15. There are ZBPs with height $O(e^2/h)$ that are present for 4 cutter gate settings. These changes in left cutter gate settings tune G_N on both sides to vary over the range 0.1 and $1.0e^2/h$. Thus, while these cutter changes significantly modify the junction transparencies, the ZBPs remain stable with respect to these perturbations. In SOI_2, there are ZBPs exhibiting this type of stability at both junctions.

To conclude this subsection, we believe that the totality of the data from device A, passing the TGP in multiple cooldowns and remeasurements, qualitative and quantitative consistency with simulations, and the stability of the SOI_2 with respect to various perturbations, provides strong evidence for the observation of a stable topological superconducting phase supporting MZMs in this device. We now turn to the reproducibility of these results in other devices.

B. Experimental data from other devices

Since disorder can destroy the topological phase, and different devices will have different disorder realizations, we can expect quantitative and qualitative differences between devices. Indeed, we have measured devices in which we were not able to find a topological phase. However, devices that have a narrow Al strip, zero-field induced gap to parent gap ratio in the required range, and weak disorder often pass the TGP while devices not meeting these requirements have never passed TGP, as expected from simulations. For example, no devices with dielectric charge density above $3\times10^{12}/\text{cm}^2$, as extracted from a Hall bar on the same chip, have passed TGP.

In this section, we show data from devices B, C, and D, summarized in Figs. 16, 18, and 19, which also pass the TGP, thereby demonstrating that we can reproducibly fabricate devices passing the TGP. These three devices are DLG devices. Device B is built on the ε stack and has $\Delta_{\rm Al} = 326 \pm 29$ μeV and $\Delta_{\rm ind} = 169 \pm 11$ μeV; hence, the ratio of the induced gap to the parent gap in device B is 0.52, which is slightly larger than in device A and very close to optimal. It has the largest topological gap reported in this paper: $\Delta_{\rm topo}^{\rm max} = 61$ μeV. Device C is built on the δ stack and has $\Delta_{\rm Al} = 292 \pm 8$ μeV and $\Delta_{\rm ind} = 104 \pm 6$ μeV; in device D, which is also built on the δ stack, the corresponding gaps are $\Delta_{\rm Al} = 293 \pm 9$ μeV and $\Delta_{\rm ind} = 117 \pm 20$ μeV. The ratio of the induced gap to the parent gap in devices C and D, 0.35, and 0.4, respectively, is somewhat smaller than the nearly optimal value of 0.52 that it takes in device B or even the value of 0.44 that it takes in device A. The effective charged impurity densities at the interface with the dielectric are $n_{\rm 2D,int} = 0.79\times10^{12}/\text{cm}^2$ in device B, $n_{\rm 2D,int} = 1.1\times10^{12}/\text{cm}^2$ in device C, and $n_{\rm 2D,int} = 1.0\times10^{12}/\text{cm}^2$ in device D, extracted by the procedure discussed in Appendix B.[6] These values are smaller than in device A and satisfy the specification given in Sec. II E.

In addition, we show data from devices E and F that do not pass the TGP. They are DLG devices built on the δ'-stack. As noted previously, we do not expect all devices to pass the TGP, even if they were to have the same gap ratio and disorder levels as device A. Hence, it is not surprising that some of our devices fail the TGP; indeed, it is required by consistency with our simulations. Moreover, devices E and F have lower induced gap to parent gap ratios, which suppresses their expected probabilities of passing the TGP. Device E has $\Delta_{\rm Al} = 415 \pm 13$ μeV and $\Delta_{\rm ind} = 90 \pm 6$ μeV (induced gap to parent gap ratio of 0.22); in device F, the corresponding gaps are $\Delta_{\rm Al} = 338 \pm 12$ μeV and $\Delta_{\rm ind} = 92 \pm 14$ μeV (induced gap to parent gap ratio of 0.27). The effective charged

[6]There is one subtlety here, which is that DLG devices have two different dielectric layers, one below the first gate layer and one between the gate layers. The first dielectric layer is likely to control bulk properties of the wire while both dielectrics contribute to junction properties. The quoted $n_{\rm 2D,int}$ numbers are for Hall bars with both dielectric layers, but the difference with $n_{\rm 2D,int}$ extracted from sibling chips is small.

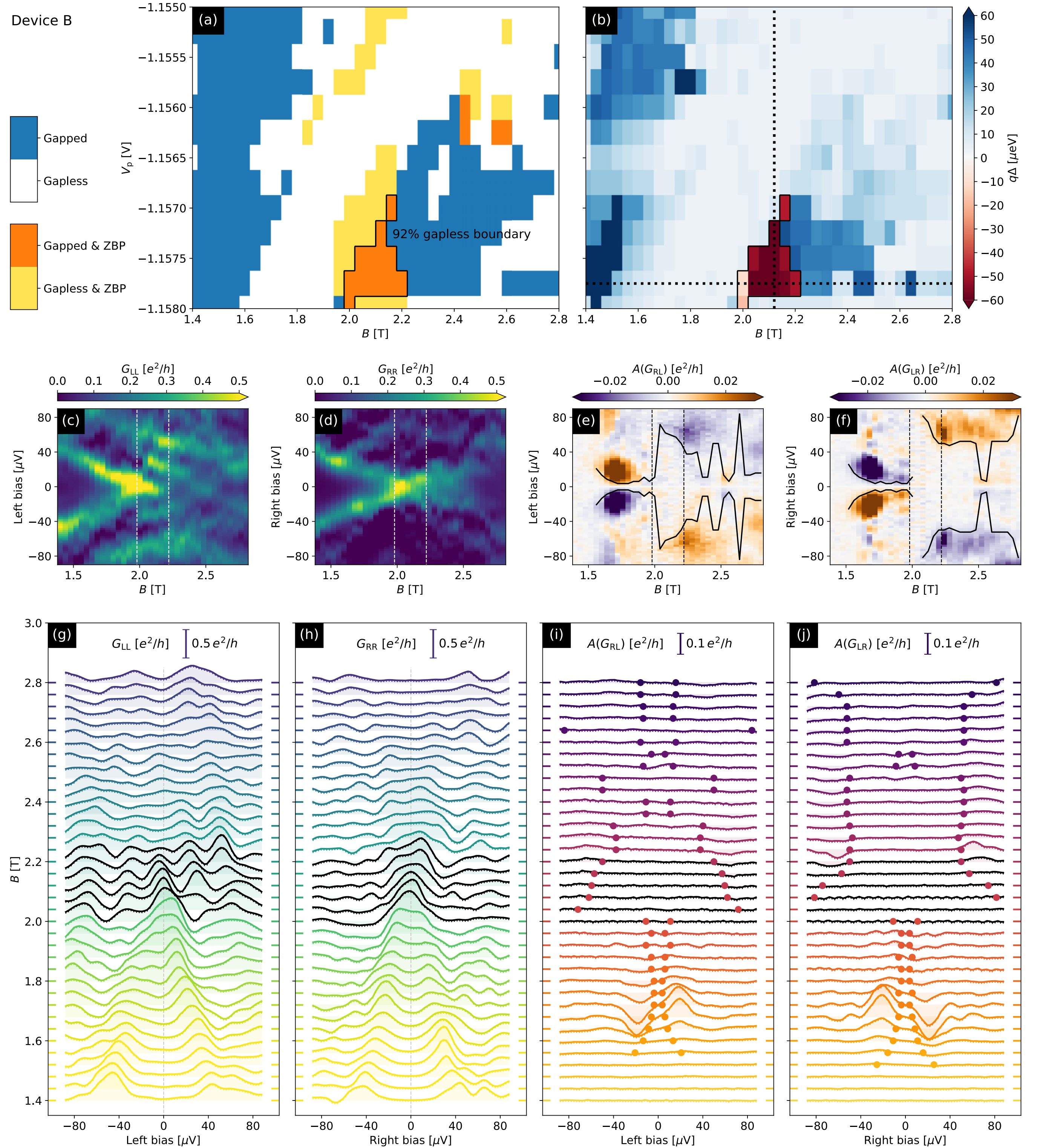

FIG. 16. (a) The experimental phase diagram of device B that results from combining the clusters of stable ZBPs at both junctions with the map of the locus of zero/nonzero gap. The stability of ZBPs is determined by varying the cutter gate settings so that for both junctions G_N take the values 0.5, 0.41, 0.33, 0.24, and $0.15e^2/h$ at $B = 1.4$ T. The boundary of the SOI_2 is interpreted as a phase transition line, consistent with a visible gap closure along 92% of it. (b) The experimental phase diagram, showing trivial/topological phases, which the TGP identifies with the exterior/interior ($q = \pm 1$) of the SOI_2. The color scale shows the size of the trivial (positive sign) or topological (negative sign) gap. The protocol assigns a maximum topological gap of $\Delta_{\rm topo}^{\rm max} = 61$ μeV. Measured local and antisymmetrized nonlocal conductances along the horizontal line in (b) at $V_p = -1.157\,75$ V: (c) G_{LL}, (d) G_{RR}, (e) $A(G_{RL})$, (f) $A(G_{LR})$. The SOI_2 lies between the vertical lines. Panels (g)–(j) are "waterfall" plots representing the same measured data. The data shown in (c)–(j) were obtained for $G_N \approx 0.41e^2/h$ on both sides. The black curves in (e) and (f) and the dots in (i) and (j) indicate where the nonlocal signal drops below a threshold value, as described in the text.

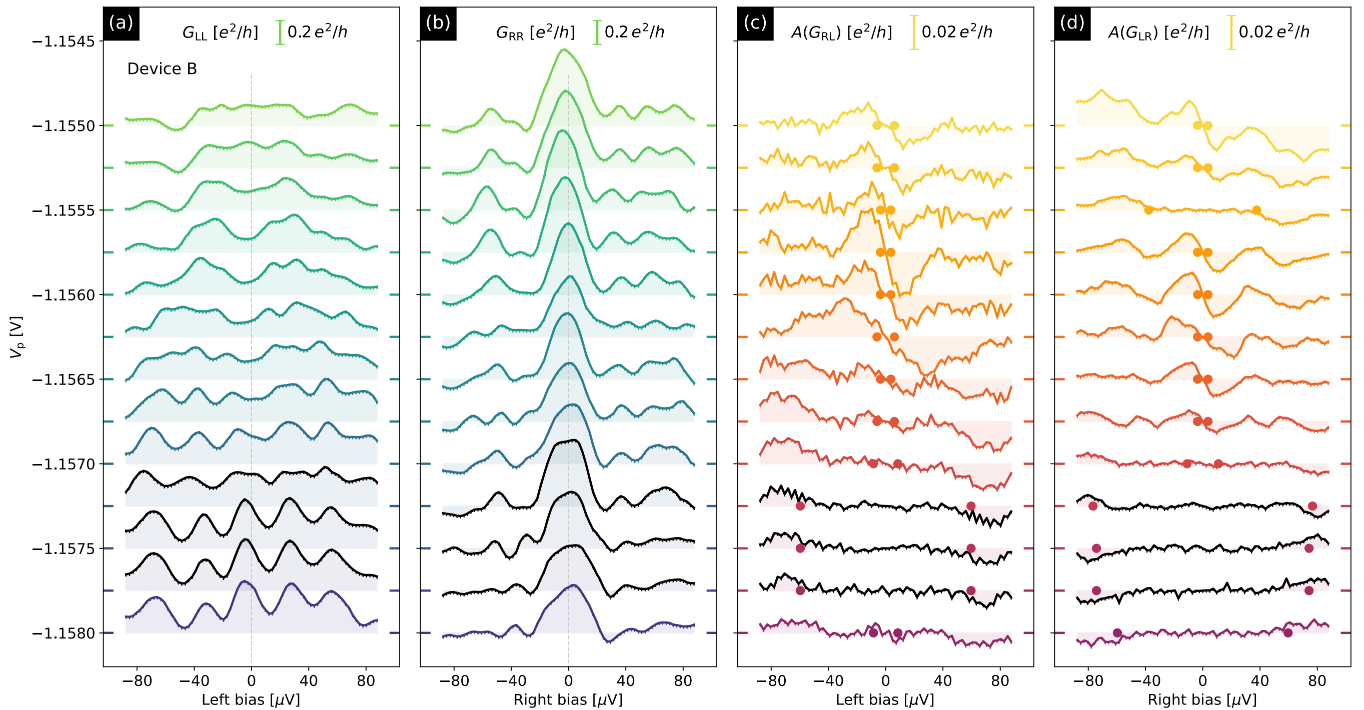

FIG. 17. “Waterfall” conductance plots of (a) G_{LL}, (b) G_{RR}, (c) $A(G_{RL})$, (d) $A(G_{LR})$ as a function of the corresponding bias and plunger gate voltage V_p for device B. The data are the $B = 2.12$ T vertical line in Fig. 16(b). ZBPs and extracted gap points corresponding to SOI_2 are shown in black.

impurity densities at the interface with the dielectric is $n_{2D,int} = 3.1\times10^{12}/cm^2$ in device E and $n_{2D,int} = 3.0\times10^{12}/cm^2$ in device F, extracted by the procedure discussed in Appendix B. These values are larger than in devices A–D, and, moreover, are large enough that they do not satisfy the specification given in Sec. II E.

Device E exhibits clusters of points in (B, V_p) space with stable ZBPs at both ends, thereby passing Stage 1 of the TGP. However, nonlocal conductance measurements in the region of interest yield zero gap. Device E is, thus, in a gapless phase and it fails Stage 2 of the TGP. Device F fails even Stage 1 because it does not have clusters of (B, V_p) points with stable ZBPs at both ends.

Overall, the measurement data from devices A–F demonstrate the different qualitative phenomena observed in our devices.

1. *Device B passing TGP*

Since device B has a considerably larger zero-field induced gap than device A, a topological phase would have to occur at higher magnetic fields. The TGP finds an experimental phase diagram that is consistent with this expectation. There is a topological phase transition at $B = 2$ T, as shown in Figs. 16(a) and 16(b). The TGP assigns this device a maximum topological gap $\Delta_{topo}^{max} = 61$ μeV. The median value of the topological gap across the orange region in Fig. 16(a) is 47 μeV. Device B has $|g_{eff}| \approx 3.7$, which is smaller than that of the other devices reported in this paper. This is consistent with device B’s large Δ_{ind}/Δ_{Al} ratio, which implies that electrons in the lowest occupied sub-band have a higher amplitude to be in the superconductor, thereby inheriting both a larger induced gap and a smaller $|g_{eff}|$.

The extent of the SOI_2 is $\delta B = 0.2$ T. The measured extent in V_p is $\delta V_p \approx 1$ mV, however, Stage 2 did not go to V_p lower than $V_p = -1.1580$ V, where the SOI_2 still appears to be quite robust, so it is possible that this underestimates the size of the SOI_2. It is also possible that the blue region centered around $B = 2.3$ T and $V_p = -1.573$ V, which the TGP identifies as a gapped trivial region due to the absence of stable ZBPs, is actually topological but has MZMs that are poorly coupled to the leads. There are some sign changes in the nonlocal conductance, such as the one that occurs at $B \approx 2$ T in Figs. 16(e) and 16(f). Since G_{LR} and G_{RL} are suppressed at these sign changes, they lead to large values of the extracted gap, which can bias Δ_{topo}^{max} towards larger values. However, even the median gap is 47 μeV, and there is a clearly identifiable gap edge at ≈50 μeV in G_{RL} at $B = 2.1$ T. “Waterfall” plots for local and nonlocal conductances at fixed plunger $V_p = -1.157\,75$ V are shown in Figs. 16(g) and 16(j). Additionally, in Fig. 17 we show “waterfall” plots of conductances for fixed magnetic field $B = 2.12$ T corresponding to the vertical line in Fig. 16(b).

As noted above, device B has the largest Δ_{ind} value and the smallest $n_{2D,int}$ value reported in this paper and, perhaps not surprisingly, the largest topological gap Δ_{topo}^{max} as well. The topological gap is actually equal, within error bars, to the largest topological gap that we would expect for a *perfectly clean*, infinitely long DLG-ε device. This is not a contradiction. Finite-size effects can increase the gap. We measure a transport gap, which is the gap to extended states (for $L = 3$ μm), and it can be larger than the gap in the spectrum if states at the gap edge have short localization lengths.

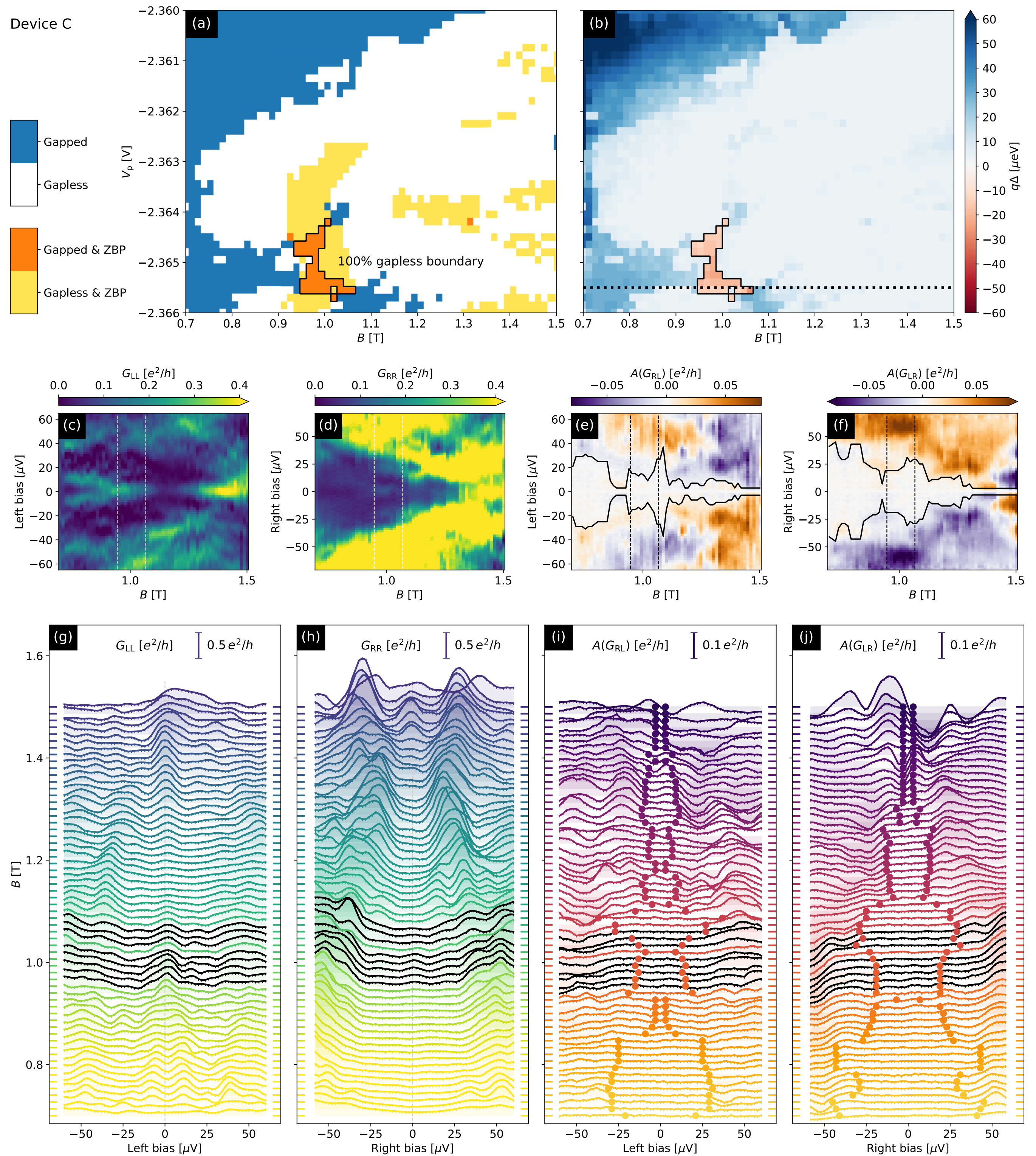

FIG. 18. (a) The experimental phase diagram of device C that results from combining the clusters of stable ZBPs at both junctions with the map of the locus of zero/nonzero gap. The stability of ZBPs is determined by varying the cutter gate settings so that G_N range from 0.6 and $1.0e^2/h$ on the left and from 0.2 and $0.4e^2/h$ on the right. The boundary of the SOI_2 is interpreted as a phase transition line, consistent with a visible gap closure along 100% of it. (b) The experimental phase diagram, showing the trivial/topological phases, which the TGP identifies with the exterior/interior ($q = \pm 1$) of the SOI_2. The color scale shows the size of the trivial (blue) or topological (red) gap. The protocol assigns maximum topological gap of 19 μeV. Measured local and antisymmetrized nonlocal conductances along the horizontal line in (b) at $V_p = -2.3655$ V: (c) G_{LL}, (d) G_{RR}, (e) $A(G_{RL})$, (f) $A(G_{LR})$. The SOI_2 lies between the vertical lines. Panels (g)–(j) are "waterfall" plots representing the same measured data. The data shown in (c)–(j) were obtained for left (right) G_N of approximately $0.6e^2/h$ ($0.2e^2/h$). The black curves in (e) and (f) and the dots in (i) and (j) indicate where the nonlocal signal drops below a threshold value, as described in the text.

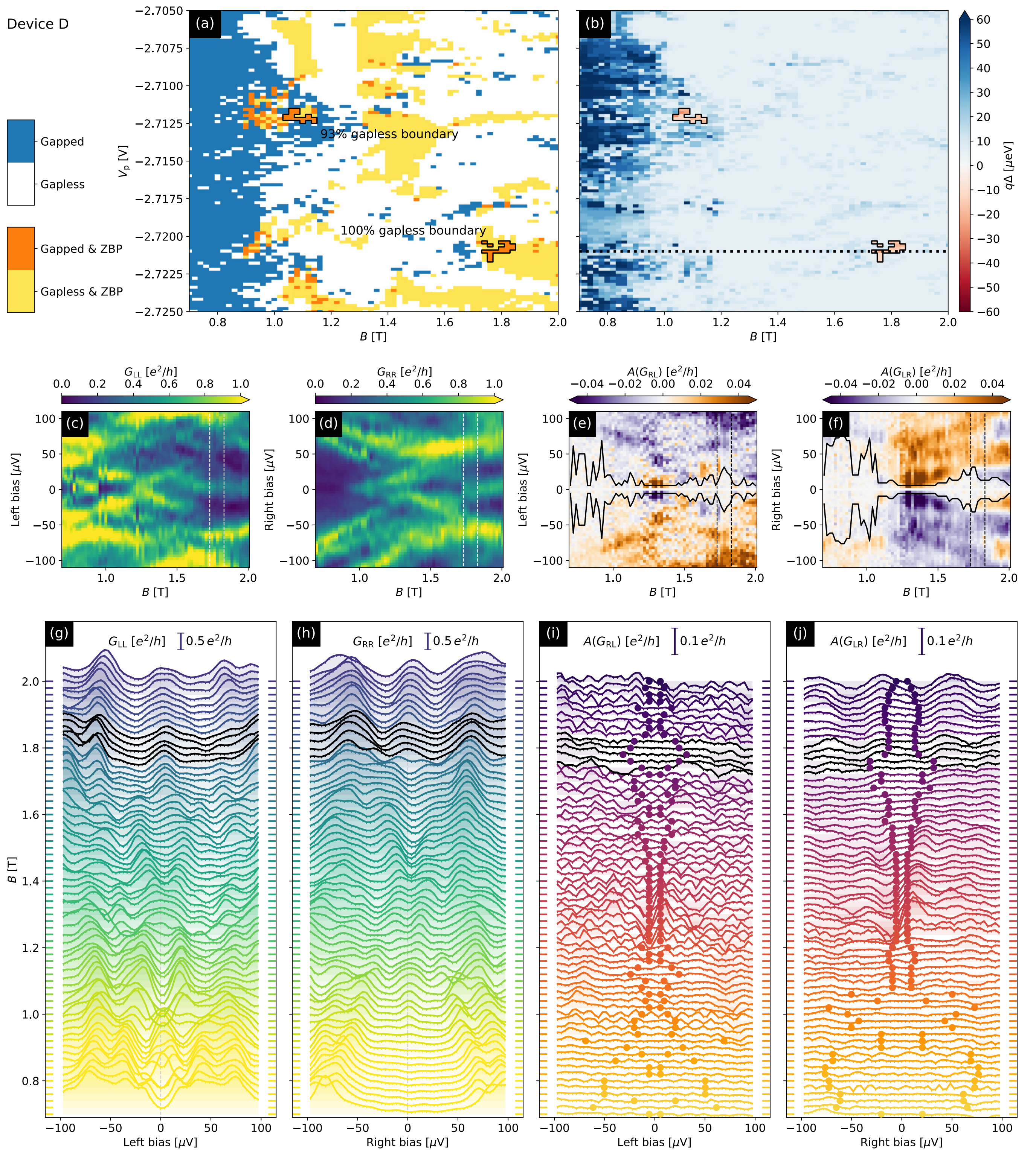

FIG. 19. Stage 2 data for device D. There are two SOI_2s in the phase diagram. (a) The experimental phase diagram of device D that results from combining the clusters of stable ZBPs at both junctions with the map of the locus of zero/nonzero gap. The boundary of the SOI_2s is interpreted as phase transition lines, consistent with visible gap closures along, respectively, 100% and 93% of them. (b) The experimental phase diagram, showing the trivial/topological phases, which the TGP identifies with the exterior/interior ($q = \pm 1$) of the SOI_2. The color scale shows the size of the trivial (blue) or topological (red) gap. The protocol assigns maximum topological gaps of 17 and 21 μeV for the top and bottom clusters, respectively. Measured local and antisymmetrized nonlocal conductances along the horizontal line in (b) at $V_p = -2.721$ V: (c) G_{LL}, (d) G_{RR}, (e) $A(G_{RL})$, (f) $A(G_{LR})$. The SOI_2 lies between the vertical lines. Panels (g)–(j) are "waterfall" plots representing the same measured data. All data shown in this figure were obtained for left/right G_N of approximately $0.8e^2/h$. The black curves in (e) and (f) and the dots in (i) and (j) indicate where the nonlocal signal drops below a threshold value, as described in the text.

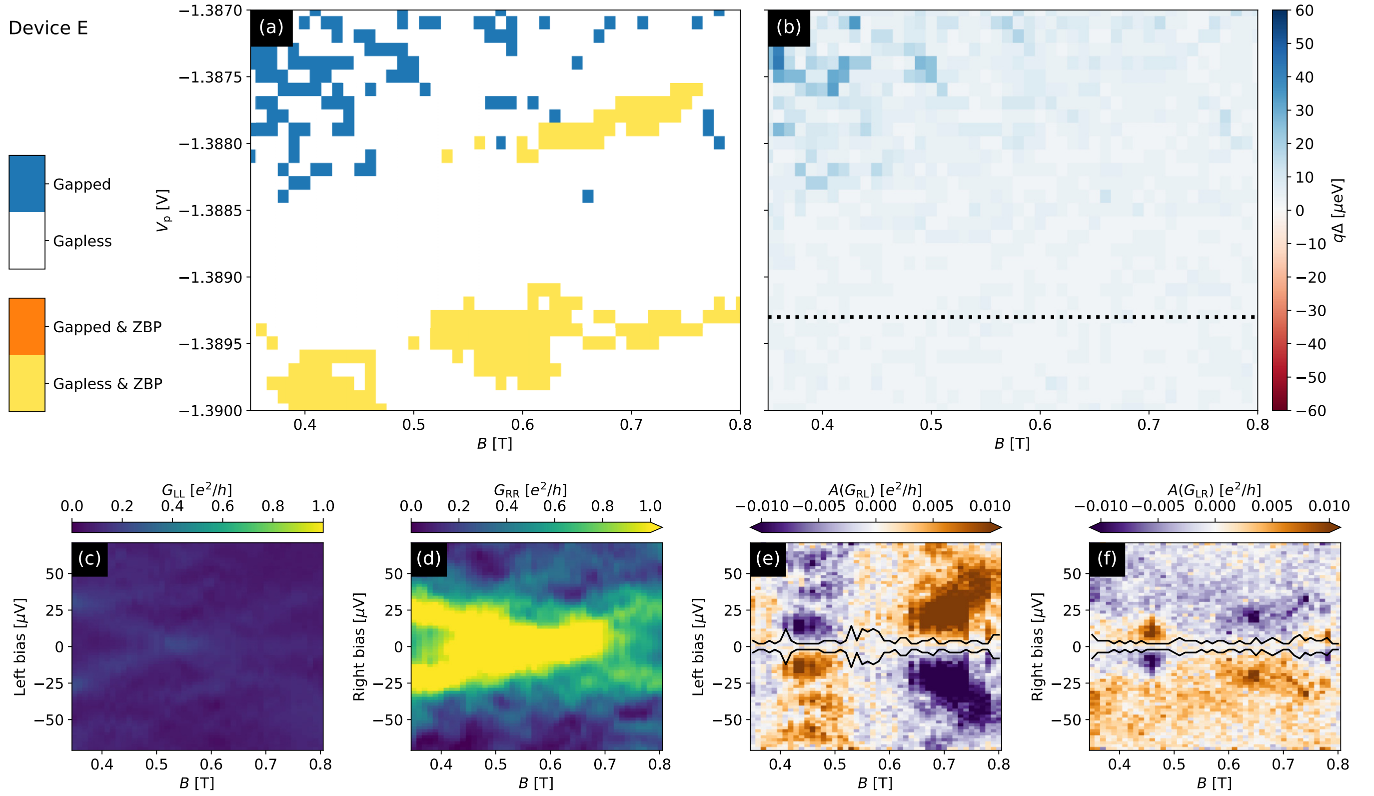

FIG. 20. Stage 2 data for device E. (a) The regions with stable ZBPs at both junctions. The stability of ZBPs is determined by varying the cutter gate settings so that the above gap conductances are 0.6 and $1.0e^2/h$ on the left and 0.2 and $0.4e^2/h$ on the right. (b) The gap as function of B, V_p. It vanishes in the region of interest, so this device fails the TGP. Measured local and antisymmetrized nonlocal conductances along the horizontal line in (b) at $V_p = -1.3893$ V: (c) G_{LL}, (d) G_{RR}, (e) $A(G_{RL})$, (f) $A(G_{LR})$. The local conductances in (c) and (d) show ZBPs, but there is no gap reopening visible in the antisymmetrized nonlocal conductances in (e) and (f). The cut shown in (c)–(f) is at G_N of approximately $0.6e^2/h$ on the left and $0.2e^2/h$ on the right.

2. *Devices C and D passing TGP*

The experimental phase diagram for device C is shown in Fig. 18. The TGP assigns this device a maximum topological gap $\Delta_{topo}^{max} = x19$ μeV, which is comparable to that of A1 and A3. The lowest B field at which the gap closes is 0.7 T, corresponding to $|g_{eff}| \approx 4.4$, which is comparable to but smaller than that of device A. The extent of the topological phase is $\delta V_p \approx 1.5$ mV and $\delta B = 0.2$ T. On the other hand, device C's ROI_2 is at significantly lower plunger gate voltage $V_p \approx -2.3655$ V than device A's. We attribute this to differences in the dielectric that that are evident from Hall bar measurements. In addition, the gap closing in device C is more clearly visible in $A(G_{RL})$ than in $A(G_{LR})$, and the ZBP has much higher amplitude in G_{LL} than in G_{RR}. The data are otherwise similar to that obtained from device A.

In Fig. 19, we show data from device D. There are two topological regions in the phase diagram. The TGP assigns maximum topological gaps of 17 μeV for the top and bottom regions, respectively. Even taken together, these regions occupy relatively small fraction of the phase diagram. The top cluster is detected at $B = 1.1$ T whereas the bottom one appears at $B \gtrsim 1.8$ T. The latter is a relatively high field, but it is consistent with the broad distribution of fields that we find in simulations.

Our results on device D show that the TGP can even identify small ROI_2s with small topological gaps.

3. *Devices E and F* **not** *passing TGP*

In Fig. 20, we show data from device E. This device has large regions with stable ZBPs at each end and thus shows a relatively large ROI_1 in the Stage 1 of the TGP. However, in Stage 2 the system appears gapless throughout the region of interest: The induced gap closes and there are no signatures of gap reopening in the nonlocal measurements. Since the system appears gapless in nonlocal conductances it is unclear if the correlated ZBPs correspond to a topological or trivial phase: either the topological gap is too small to be experimentally resolved or we observe a trivial state that couples to both sides because of the long coherence length that is expected in a system with very small gap. The fact that the ZBP is significantly brighter in G_{RR} than in G_{LL} as well as the similarity of finite-bias features in local measurements hints towards the second scenario. In both cases, such a phase would not be suitable for topological quantum computation. This example demonstrates the importance of Stage 2 of the TGP where nonlocal conductance is measured in order to identify false positives from Stage 1.

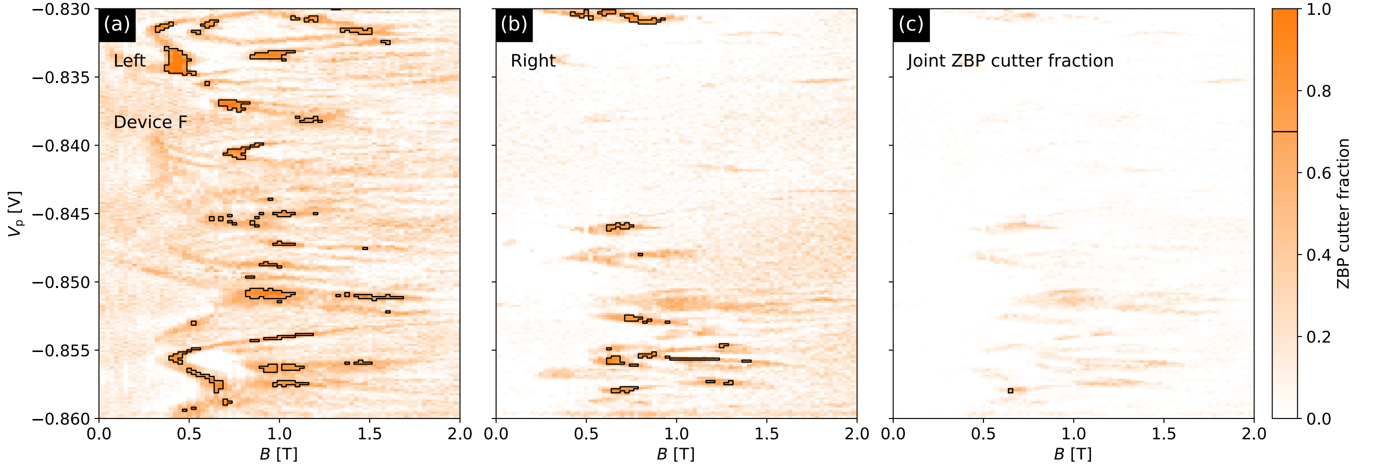

FIG. 21. Stage 1 data for device F. The ZBP probabilities at the (a) left and (b) right junctions as a function B and V_p. As may be seen in (c), there is no region that has stable ZBPs at both junctions.

Meanwhile, device F does not have any regions with stable ZBPs at both ends, as may be seen in Fig. 21. The absence of correlations may be due to an inhomogeneous slowly varying potential along the nanowire. The ZBPs that are seen at one end or the other are very similar to the ZBPs that are seen in devices passing the TGP. However, the ZBP that show up in more than 70% of cutter settings show no stable correlations between the two junctions. They may originate from trivial Andreev bound states (ABS) crossing zero energy or stable ZBPs, dubbed quasi-MZMs, that appear due to a slowly varying potential near the junction. Such states do not span over the whole length of the wire. The absence of a large enough cluster of correlated ZBPs causes this device to fail Stage 1 of the TGP.

V. SUMMARY AND DISCUSSION

In the previous sections, we have presented a summary of observed phenomena in gate-defined semiconductor nanowires coupled to a superconductor. We have demonstrated that, when devices A–D are tuned to the single-subband regime, they yield data passing the TGP at magnetic fields in the range 1–2.5 T. We have observed topological gaps as high as $\Delta_\mathrm{topo}^\mathrm{max} \approx 60\ \mu\mathrm{eV}$. We emphasize that our results are reproducible within the same cooldown and between different cooldowns, as we have shown for device A. In short, our main empirical result is that multiple devices have passed the TGP.

These measurements represent strong evidence for the observation of a topological superconducting phase supporting MZMs. The TGP has been tested with extensive simulations, reliably identifying topological regions of the phase diagram of simulated devices and correctly distinguishing trivial Andreev bound states from Majorana zero modes. We found that, for a simulated device, there is >90% probability that, when the TGP finds an ROI_2, there is a topological phase in this region of its phase diagram.

We note that the observed topological gaps are in the range of 17–61 μeV and occupy a correspondingly small size of the phase diagram. Mesoscopic fluctuations are significant, so device-to-device variation and cooldown-to-cooldown variation for the same device cannot be neglected for current devices.

In order to guide incremental progress towards passing the TGP, we relied on our estimates of the material and disorder requirements that gate-defined nanowires must satisfy. We developed designs and fabrication processes capable of meeting these requirements.

In the remainder of this section, we turn to the interpretation of our results. The stability of the identified topological phase as a function of B and V_p is an important consistency check for our results. For the extracted effective g_eff-factor in measurement A1, $\delta B \approx 500$ mT corresponds to a Zeeman energy of 80 μeV and, for the calculated lever arm of ≈85 meV/V, $\delta V_\mathrm{p} \approx 1.5$ mV corresponds to a chemical potential shift of 128 μeV [see Eq. (1)]. In other words, the phase space extent in field is 3.5 times and the extent in gate voltage is 3.9 times the maximum topological gap of 23 μeV. In measurement A2, we found that the topological region in Fig. 13 extends over a maximum B-field range $\delta B = 500$ mT and a maximum $\delta V_\mathrm{p} = 2.5$ mV, corresponding, respectively, to energy scales of 80 and 213 μeV. The other devices/measurements have similar stability in B and V_p. Since the topological phase has an irregular shape, its area is smaller than the product of B and V_p; it is listed in Table III, where the areas of the other measured topological regions are also listed. All of the devices have $\mathcal{V}_\mathrm{SOI2}$ in the range 0.1–0.5 mV T, and they have $\mathcal{V}_\mathrm{SOI2}$ values that are larger than $(\Delta_\mathrm{topo}^\mathrm{max})^2$, in some cases, substantially larger, except device B. Note, however, that device B may have a larger SOI_2 than what we can see in Fig. 16, extending below $V_\mathrm{p} = -1.1580$ V. In other words, the observed candidate MZMs are stable with respect to parameter changes comparable to or larger than the maximum topological gap, which is an intrinsic energy scale of the problem that was determined from nonlocal conductance measurements.

The summary of the simulated data in the magnetic field range $B \leqslant 2.5$ T, which is comparable to experiment, is shown in Table IV. Here we present a brief summary; the raw data set is available [98]. The TGP yield and the average vol-

TABLE III. For devices A–D passing the TGP, we list the the measured maximum topological gap $\Delta_{\rm topo}^{\rm max}$; the effective g-factor $g_{\rm eff}$; the volume of the $\rm SOI_2$ shown in Sec. IV, in units of mV T and $(\Delta_{\rm topo}^{\rm max})^2$; the "center-of-mass" magnetic field $B_{\rm SOI2}$ of the $\rm SOI_2$; and the percentage of the boundary of the $\rm SOI_2$ that is gapless (GB%). Device D has two $\rm SOI_2$, and we list the values associated with both. From simulations, we estimate the lever arm as $d\mu/dV_{\rm p}$ = 85 meV/V for device A, 78 meV/V for device B, and 79 meV/V for devices C and D (see Table I).

Device, measurement	Design, stack	$\Delta_{\rm topo}^{\rm max}$ [μeV]	$\lvert g_{\rm eff}\rvert$	$\mathcal{V}_{\rm SOI2}$ [mV T]	$\mathcal{V}_{\rm SOI2}$ $[(\Delta_{\rm topo}^{\rm max})^2]$	$B_{\rm SOI2}$ [T]	GB [%]
A, A1	SLG-β	23	5.6	0.5	12	1.7	78
A, A2	SLG-β	29	6.4	0.5	8.6	1.0	80
A, A3	SLG-β	22	6.4	0.2	5.7	1.0	90
B	DLG-ε	61	3.7	0.2	0.3	2.1	92
C	DLG-δ	19	4.4	0.1	2.0	1.0	100
D	DLG-δ	17	4.5	0.1	2.5	1.8	100
D	DLG-δ	21	4.5	0.1	1.4	1.1	93

ume of $\rm SOI_2$ decreases with disorder strength (leaving aside the case of $n_{\rm 2D,int} = 0.1\times10^{12}/\rm cm^2$ which requires a different TGP calibration). The observed phase space of the topological phase is consistent with the results of simulations presented in Table IV, where we found that simulated SLG-β and DLG-ε devices had mean $\bar{\mathcal{V}}_{\rm SOI2}$ in the range 0.1–0.2 mV T, but with a distribution that has long tails extending up to large volumes. Similarly, our simulated SLG-β devices have $\Delta_{\rm topo}^{\rm max}$ values in the range 23–35 μeV while our simulated DLG-ε devices have $\Delta_{\rm topo}^{\rm max}$ values in the range 25–29 μeV, both with long tails at large gaps. Device A would appear to be in the tail of the distribution, both with respect to $\Delta_{\rm topo}^{\rm max}$ and $\mathcal{V}_{\rm SOI2}$ while device B appears to be in the tail of the distribution with respect to $\Delta_{\rm topo}^{\rm max}$. In summary, the phase space for the topological phase is roughly as large as we would expect for a maximum topological gap of 20–60 μeV and broadly consistent with our simulations. We note that this is a larger gap than in early measurements of the $\nu = \frac{5}{2}$ fractional quantum Hall state [114,115] and further note that the topological gap at $\nu = \frac{5}{2}$ subsequently increased dramatically with material quality [116,117].

TABLE IV. Statistics of $\rm ROI_2$ and $\rm SOI_2$ properties for simulated transport data from SLG and DLG devices for the average disorder strengths given in the first column. The third and fourth columns show the TGP yield as a fraction of devices that have at least one $\rm ROI_2$. Its denominator indicates the total number of simulated devices; the numerator, the number of devices that pass the TGP. The TGP yield decreases with increasing disorder. All statistics in this table have been calculated with the magnetic field restricted to $B \leqslant 2.5$ T. The mean value of $\Delta_{\rm topo}^{\rm max}$ has weak dependence on the disorder strength, but the average phase space volume of an $\rm SOI_2$, $\bar{\mathcal{V}}_{\rm SOI2}$, decreases with increasing disorder, as may be seen in the fourth column. For all disorder strengths simulated, $\bar{\mathcal{V}}_{\rm SOI2} \sim O(0.1)$ mV T. The last column lists $\bar{B}_{\rm SOI2}$, the average B field of an $\rm SOI_2$, where the bar represents the statistical average over different disorder realizations. These regions occur at significantly higher magnetic field in the ε-stack, as expected since $\Delta_{\rm ind}$ is larger and $g^{\star}$ is smaller.

Design, stack	$n_{\rm 2D,int}$ $[10^{12}/\rm cm^2]$	Yield $\leqslant$2.5 T	$\bar{\Delta}_{\rm topo}^{\rm max}$ [μeV]	$\bar{\mathcal{V}}_{\rm SOI2}$ [mV T]	$\bar{B}_{\rm SOI2}$ [T]
SLG-β	1.0	47/50	23	0.2	1.9
	2.7	23/50	34	0.1	1.5
	4.0	24/49	34	0.1	1.5
DLG-ε	0.1	24/50	35	0.2	2.2
	1.0	28/50	29	0.2	2.3
	2.7	13/50	30	0.2	2.2
	4.0	16/50	30	0.1	2.2

The measured $\Delta_{\rm topo}^{\rm max}$, $\mathcal{V}_{\rm SOI2}$, $B_{\rm SOI2}$ values in Table III are consistent with the simulated values in Table IV, which further validates the simulation model that was used to estimate the FDR. The primary outliers are $\mathcal{V}_{\rm SOI2}$ for measurements A1 and A2 and $\Delta_{\rm topo}^{\rm max}$ for device B; they are substantially larger than the mean values in simulations, but within the long tails of the non-Gaussian distributions found in simulations (see Appendix E for details). This consistency between simulated and measured values validates the model used to test the TGP, as suggested in Ref. [112].

We now consider other potential explanations of our results. According to our simulations, the probability that a device that passes the TGP does not have a topological phase overlapping the $\rm ROI_2$ is less than 10%, so any other explanation is extremely unlikely, though not impossible. For an intuitive understanding of why other explanations are unlikely, let us discuss trivial ZBPs. First, we observe that all of our devices have trivial ZBPs, even the ones that pass the TGP. Often, they occur at only one junction, but they sometimes occur at both junctions and they can even be stable to changes in junction transparency and also to changes in B and $V_{\rm p}$. For instance, there are stable ZBPs at both junctions in measurement A1 for 1 T $< B <$ 2 T and $V_{\rm p} \approx -1.173$ V, as may be seen in Fig. 11. In device E, there are stable ZBPs at both junctions for 0.5 T $< B <$ 0.6 T and $V_{\rm p} \approx -1.138\,95$ V, as may be seen in Fig. 19. These are all trivial and fall outside the topological region because the observed bulk transport gap is zero.

Now, let us consider the causes of trivial ZBPs. One possible origin is a slowly varying potential near the end of a device, which can be caused by certain tunnel barriers. In sufficiently clean devices, this can lead to quasi-MZMs *before* a bulk gap closing, where they are a precursor to the topological phase transition [46–49,51]. Quasi-MZMs do not appear *after* a gap closing/reopening. If the bulk gap never reopens, as in Figs. 31(g)–31(j), then quasi-MZMs fail to become MZMs. However, if the bulk gap reopens, as in Figs. 31(c)–31(f), then quasi-MZMs evolve into true MZMs. By design, Stage 2 of the TGP weeds out stable ZBP clusters in which quasi-MZMs do not evolve into true MZMs.

Trivial ZBPs can also be induced by disorder in proximitized semiconductor nanowires with spin-orbit coupling [43–45]. However, this scenario does not entail a gap closing and reopening in the nonlocal signal, from which we conclude that it does not apply to devices A, B, C, and D. ZBPs can also be caused by trivial ABS, which can "accidentally" pass through zero energy. It is very difficult to discern a trivial ABS from an MZM purely from the local conductance spectroscopy, which can be virtually identical. However, as in the case of disorder-induced ZBPs, a trivial ABS need not be accompanied by a gap closing and reopening in the nonlocal signal.

A gap closing/reopening could be caused by the orbital effects of the magnetic field. When half a flux quantum is threaded through the effective cross-sectional area of the device, the proximity effect is suppressed, and the gap closes. It reopens when the flux increases still further, closing a second time when $\frac{3}{2}$ flux quanta thread the active region. For device A, we expect a gap closing due to orbital effects at $\gtrsim$2.5 T in higher sub-bands and even higher fields $>$3 T in the lowest sub-band. The observed gap closing is at much lower fields. Crucially, a gap closing due to orbital effects would be weakly dependent on the gate voltage, as illustrated by the simulated phase diagrams of clean systems in Fig. 4, where the first closing due to orbital effects is a wide, nearly vertical white bar at $B \approx 2.5$ T that intersects the topological lobes at $V_\mathrm{p} \approx -0.8$ V and $V_\mathrm{p} \approx -1.0$ V (SLG-β) or $V_\mathrm{p} \approx -0.95$ V (DLG-ε). We find similar behavior in the simulations that we used to test the TGP, which include disorder. On the other hand, as may be seen in Fig. 13, the gap closing that is observed in measurement A2 is strongly dependent on the gate voltage: at $V_\mathrm{p} \approx -1.407$ V, the gap closes at $B \approx 0.6$ T, but at $V_\mathrm{p} \approx -1.398$ V, it is still open at $B = 2$ T. Similarly, device C has a gap closing that occurs at $B \approx 0.7$ T at $V_\mathrm{p} \approx -2.363$ but it is still open at $B = 1.3$ T at $V_\mathrm{p} \approx -2.360$. Devices B and D have ROI_2s that occur at higher fields, but still below 2.5 T, and the gap closings are at, respectively, $B \approx 1.6$ T and $B \approx 1$ T. To determine the V_p dependence of the gap closing in device B, we performed a large-scale Stage 1 scan, which shows clear dependence, with a trivial gap that that is still open at $B = 2$ T for some values of V_p. Hence, an explanation relying on the orbital effect of the magnetic field is not consistent with either the B-field value or the V_p dependence of the observed gap closings/reopenings in devices A–D.

Of course, it is conceivable that the bulk gap closes and reopens accidentally and that trivial ZBPs also accidentally occur for the same B and V_p. But to pass the TGP, the accidental closing would have to occur over an entire curve in the B-V_p phase space and, moreover, the trivial ZBPs would have to persist over the enclosed region. Of course, we cannot rule this out completely. However, such coincidences do not require any physics that is not incorporated in our simulations. Hence, they could occur in our simulations, and we can quantitatively bound their probability. The false discovery rate (FDR) that we estimate from simulations is $\leqslant 8\%$ at a 95% confidence level for all of the device designs, material stacks, and disorder levels that we have simulated, which implies that there is a low probability that data from devices A–D can be explained by trivial ZBPs that occur coincidentally with an accidental gap closing/reopening instead of a topological phase.

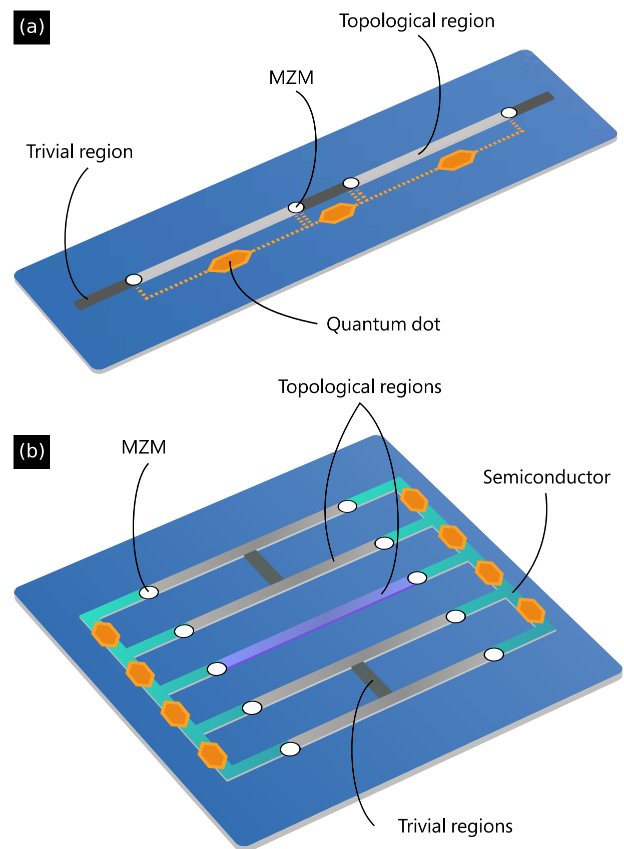

FIG. 22. (a) The linear tetron, a minimal device for performing fusion. The two outer regions must be tuned into the topological phase via the TGP, while the middle section must be in the trivial phase. This results in a device with four MZMs. (b) Two two-sided tetrons, with which measurement-based braiding can be performed. There are 5 topological sections. The middle (purple) one is a coherent link that is used for connecting the left and right of the two tetrons.

VI. LOOKING AHEAD

A reliable process for tuning devices into the topological phase is an essential step on the journey to topological quantum computation, which relies on the fusion and braiding of anyons. Networks of such wires can be assembled into a many-qubit device, and this protocol can be used to tune each wire within a qubit into the topological phase. The linear tetron qubit [118,119] is a minimal device for performing two noncommuting fusion operations;[7] it is shown schematically in Fig. 22(a). There are two outer topological sections, separated by a trivial section. Fusion outcomes for different pairs of MZMs are measured by coupling these MZMs to adjacent quantum dots. By measuring different sequences of pairs of MZMs, we can directly measure the fusion rules, a topological invariant of the state. The parameter space of such a device is simply too large to explore in the hope of finding a suitable operating point unless each of the outer sections of the nanowire is individually tuned into a topological phase, which can be achieved using the TGP.

[7]See Refs. [120–124] for related alternate qubit designs.

Coherent manipulation of the encoded quantum state, for example through measurement-based implementations of braiding transformations [125,126], requires an even more complex device, as shown in Fig. 22(b). This device consists of two superconducting islands, each comprised of two topological segments linked together by a short region of trivial superconductor, and thus contains two qubits. We refer to this configuration as a two-sided tetron because MZMs are on each side of the device. The additional topological wire between the qubit islands, shown in purple, is added to allow measurements between MZMs on opposite sides of the islands. In this device, unitary Clifford gates on one of the two qubits can be performed by using the other as an auxiliary qubit and performing a sequence of single- and two-qubit measurements [119]. Despite the even larger parameter space, these devices can be tuned using the TGP. Continued improvement in simulation, growth, fabrication, and measurement capabilities will be required to achieve the topological gap required for such coherent operations.

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Correspondence and requests for materials should be addressed to C. Nayak (cnayak@microsoft.com). Experimental and simulated data sets, as well as the source code that performs the analysis and produces the corresponding figures, are available at GitHub and Azure Quantum [98]. Some Microsoft trade secrets are not divulged here, as detailed in Sec. II G, but this manuscript contains enough information for other researchers to replicate and build upon this research. We intend to lift the restrictions on sharing the device fabrication details on December 31, 2024, after which they can be obtained from the corresponding author. An editorial on this topic may be found at https://doi.org/10.1103/PhysRevB.107.210001.

APPENDIX A: EFFECTS OF DISORDER

1. Projection to proximitized nanowire model

The disorder-free limit of the single-sub-band regime is well-represented by a Hamiltonian of the form of Eq. (1):

$$H = Z^{\dagger}(H_{\text{SM}} - \tilde{\Gamma} O_{\text{SC}})Z. \tag{A1}$$

In Eq. (A1), the effective mass, g-factor, and spin-orbit coupling in H_{SM}, obtained by projecting the full model for the device designs and material stacks described in Secs. II B and II C into the lowest sub-band, take the values given in Table I. The parameters in Table I are weakly density dependent within the range of $n \sim 0.02$–$0.04\ \text{nm}^{-1}$, which corresponds to the range of a Fermi wavelength $k_{\text{F}}^{-1} \simeq$ 40–80 nm. Compared to Eq. (1), there is a transformation Z, described below, which is due to the renormalization of the electrons in the semiconductor by their coupling Γ to the Al, which has a superconducting gap $\Delta_{\text{Al}} = 300\ \mu\text{eV}$ and a Zeeman potential $V_{x,\text{SC}} = g_{\text{SC}}\mu_{\text{B}}B/2$ with g-factor $g_{\text{SC}} = 2$.[8] In the following we will neglect the orbital effect of the magnetic field on the superconductor, despite keeping the Zeeman splitting. The justification for this is that the SC thickness is $d < 10$ nm and we estimate the disordered coherence length in the Al, ξ_{Al}, to be around 40 nm. Orbital effects can be neglected when the depairing energy is small compared to the gap; this ratio goes as the square of the ratio of flux through the effective cross-section $d\xi_{\text{Al}}$ to the flux quantum, yielding a condition $(B\xi_{\text{Al}}d/\Phi_0)^2 \ll 1$ [127]. For fields $B < 2.5$ T, the left-hand side is less than $\frac{1}{4}$, so we expect the corrections due to orbital effects to be correspondingly small. The effective pairing depends on the Zeeman potential in the SC as $\tilde{\Gamma} = \Gamma\Delta_{\text{Al}}/\sqrt{\Delta_{\text{Al}}^2 - V_{x,\text{SC}}^2}$. Additionally, the Zeeman potential experienced by the SM now includes an induced contribution from the Al, $\tilde{V}_x = V_x + \Gamma V_{x,\text{SC}}/\sqrt{\Delta_{\text{Al}}^2 - V_{x,\text{SC}}^2}$.

In all three cases, SLG β stack and DLG δ and ε stacks, the transformation by Z as well as the induced Zeeman energy from the Al suppress the effective g-factor below g_{SM}. Hence, as discussed in the previous section, the coupling between the semiconductor and the superconductor, Γ, should not be too large or else the g-factor will be strongly suppressed and the topological phase will be pushed to high B fields where the Al approaches the Clogston limit. On the other hand, Γ cannot be too small, either, or else the induced gap $\Delta_{\text{ind}} \sim \Gamma\Delta_{\text{Al}}/(\Gamma + \Delta_{\text{Al}})$ will be small.

We now turn to the renormalization factor Z. The Green's function of a hybrid SM-SC system is given, in general, by

$$G(\omega) = [\omega - H_{\text{SM}} - \Sigma(\omega)]^{-1} \tag{A2}$$

with a self-energy $\Sigma(\omega)$ obtained by integrating out the SC degrees of freedom using the tunneling Hamiltonian model defined in Ref. [128],

$$\Sigma(\mathbf{r}, \mathbf{r}', \omega) = -\int d\mathbf{x}_1 d\mathbf{x}_2\, T^{\dagger}(\mathbf{r}, \mathbf{x}_1)T(\mathbf{x}_2, \mathbf{r}')\, G_{\text{SC}}(\mathbf{x}_1, \mathbf{x}_2, \omega). \tag{A3}$$

Here, the integrals are taken over the superconducting domain with $\mathbf{x} = (z, \mathbf{r})$ where z and $\mathbf{r}$ are out of plane and in the plane of the interface, respectively; the tunneling matrix element reads as

$$T(\mathbf{x}_1, \mathbf{r}) = t\delta(\mathbf{r}_1 - \mathbf{r})\delta(z_1)\partial_{z_1}. \tag{A4}$$

The delta function here corresponds to momentum conservation parallel to the interface whereas ∂_{z_1} enhances transmission for electrons in the superconductor that are incident with momentum normal to the interface. After some algebra [27], one finds that $\Sigma(r, r', \omega) \propto \delta(r - r') \int d\xi_k G_{\text{SC}}(\omega, k)$ where $\delta(r - r')$ represents the rapid decay of the self-energy on the scale of the Fermi wavelength in the metal.

We now derive the expression for the self-energy in the presence of disorder in Al which is crucial for understanding the proximity effect [27,129–132]. Indeed, disorder removes momentum conservation constraints and effectively increases

[8]Note that this effective Hamiltonian is only valid provided Δ_{Al} is not too small. In the more general case, integrating out the superconductor leads to an effective action that is nonlocal in time and has an energy-dependent renormalization.

the tunneling rate Γ. The disorder-averaged self-energy can be written as

$$\Sigma(\mathbf{r}, \mathbf{r}', \omega) = \Gamma g(\omega)\delta(\mathbf{r} - \mathbf{r}'), \quad \text{(A5)}$$

where the Usadel Green's function $g(\omega)$ represents the diffusive limit of a spin-split s-wave superconductor. Here we neglect the orbital contribution of the magnetic field, as justified above. Analytic expressions for this Green's function in this limit have been recently reported in Refs. [133,134].

Now, we would like to obtain a frequency-independent effective Hamiltonian with eigenvalues that approximate the poles of $G(\omega)$ [Eq. (A2)], but, in order to do so, it is insufficient to take the static limit by replacing $\Sigma(\omega)$ by $\Sigma_0 \equiv \Sigma(0)$. A better, widely used, approximation involves grouping the linear-in-frequency part of the self-energy, $\Sigma_1 \equiv \partial_\omega \Sigma(\omega)|_{\omega=0}$, with the frequency of the Green's function to define an overall renormalization of the energy scale before taking the static limit. Here we describe a generalization of that method.

Specializing the expressions in [133,134] to the static and linear-in-frequency parts, we obtain

$$\Sigma_0 = -\frac{\Gamma(-V_{x,\mathrm{sc}}\sigma_x\tau_z + \Delta_{\mathrm{Al}}\sigma_y\tau_y)}{\sqrt{\Delta_{\mathrm{Al}}^2 - V_{x,\mathrm{sc}}^2}}, \quad \text{(A6)}$$

$$\Sigma_1 = -\frac{\Gamma\left(\Delta_{\mathrm{Al}}^2 - V_{x,\mathrm{sc}}\Delta_{\mathrm{Al}}\sigma_z\tau_x\right)}{\left(\Delta_{\mathrm{Al}}^2 - V_{x,\mathrm{sc}}^2\right)^{3/2}}, \quad \text{(A7)}$$

and the Green's function in this linearized representation is

$$\tilde{G}(\omega) = [\omega(1 - \Sigma_1) - H_{\mathrm{SM}} - \Sigma_0]^{-1}. \quad \text{(A8)}$$

As a consistency check, we can consider the well-known $V_{x,\mathrm{sc}} = 0$ limit, where $\Sigma_0 = -\Gamma\sigma_y\tau_y$ and $\Sigma_1 = -\Gamma/\Delta_{\mathrm{Al}}$ and recover

$$\tilde{G}_{V_{x,\mathrm{sc}}=0}(\omega) = \frac{\Delta_{\mathrm{Al}}}{\Delta_{\mathrm{Al}} + \Gamma}\left[\omega - \frac{\Delta_{\mathrm{Al}}}{\Delta_{\mathrm{Al}} + \Gamma}(H_{\mathrm{SM}} - \Gamma\sigma_y\tau_y)\right]^{-1} \quad \text{(A9)}$$

with poles at the eigenvalues of the renormalized effective Hamiltonian

$$H_{\mathrm{eff}} = \frac{\Delta_{\mathrm{Al}}}{\Delta_{\mathrm{Al}} + \Gamma}(H_{\mathrm{SM}} - \Gamma\sigma_y\tau_y), \quad \text{(A10)}$$

recovering the previous results of Ref. [27]. In the more general case where $V_{x,\mathrm{sc}} \neq 0$, Σ_1 is not proportional to the identity. Hence, we have to be careful in factoring out the coefficient of ω. This is because we require a Hermitian H_{eff}, and in general the matrix $(1 - \Sigma_1)^{-1}(H_{\mathrm{SM}} + \Sigma_0)$ is not Hermitian. To resolve this, we take a symmetric product, defining $Z = (1 - \Sigma_1)^{-1/2}$ and obtain the result

$$H_{\mathrm{eff}} = Z^\dagger(H_{\mathrm{SM}} + \Sigma_0)Z. \quad \text{(A11)}$$

Finally, we now extend the model to include potential disorder in the semiconductor:

$$H = Z^\dagger\left(H_{\mathrm{SM}} - \tilde{\Gamma}O_{\mathrm{SC}} + H_{\mathrm{Dis}}\right)Z, \quad \text{(A12)}$$

where the disorder potential, projected into the lowest subband, is

$$H_{\mathrm{Dis}} = \int_0^L dx\, V(x)\, \psi_\sigma^\dagger(x)\psi_\sigma(x). \quad \text{(A13)}$$

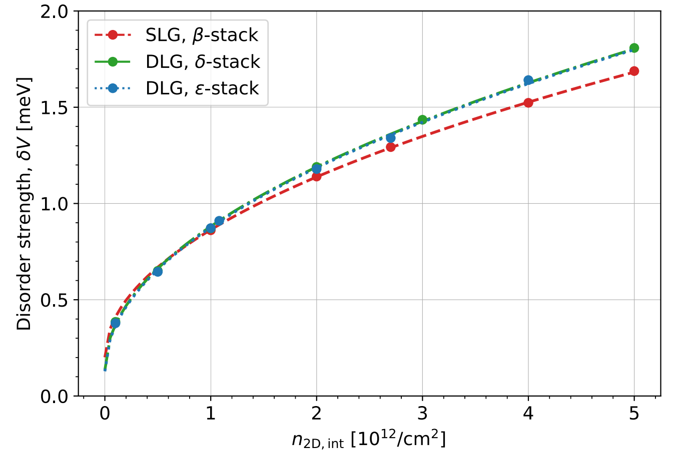

FIG. 23. The effective parameter δV describing the disorder strength as a function of $n_{\mathrm{2D,int}}$, the density of charged defects at the semiconductor-dielectric interface, for the SLG-β, DLG-δ, and DLG-ε design and material stacks.

For the disorder mechanisms we have included, we find that the random potential can be approximately characterized by its sample-averaged autocorrelation:

$$\langle V(x)V(x')\rangle = \delta V^2 \exp(-|x - x'|/\kappa). \quad \text{(A14)}$$

Similar to our extraction of other single-sub-band parameters, we generate disorder potentials using the full 3D electrostatics model,[9] project the disorder potentials to the lowest subband, obtain the autocorrelation averaged over several disorder realizations, then fit the values δV, κ. These projected disorder parameters, variance $\delta V < 2$ meV and correlation length $\kappa = 80$, 115, and 120 nm (for β, δ, and ε stacks, respectively), are obtained for the same design and materials stack as the uniform parameters given in Table I. Here, the various sources of disorder and their strengths have been distilled to two numbers. These parameters' relation to the underlying microscopic disorder depends on both the device geometry and the defect types and densities. We show the relation between δV and $n_{\mathrm{2D,int}}$ for SLG and DLG designs for the β, δ, and ε stacks in Fig. 23.

2. Disorder-driven phase transition

In general, disorder suppresses the topological phase [135–145], causing important changes to the phase diagram of Fig. 1. For weak disorder, this leads to a decrease of the topological gap and an increase of the disordered superconducting coherence length in the topological phase. As

[9]In this paper we have used the 3D Thomas-Fermi model for screening in device electrostatics simulations. In the relevant parameter regime (i.e., in the lowest sub-band) we have compared the Thomas-Fermi (TF) approximation with Schrödinger-Poisson (SP) calculations and find values of δV that agree within 20% accuracy. SP calculations yield a slightly smaller δV at low densities, and a slightly larger δV at higher densities within the lowest sub-band. We attribute this to a difference in screening due to the difference between the 3D density-of-states assumed by TF and the 1D density-of-states of the actual gate-defined nanowire.

the disorder strength is increased, these variations can create small nontopological regions in an otherwise topological wire, thus nucleating additional subgap states at the domain walls between topological and nontopological regions. Eventually, these subgap states hybridize and lead to the breakdown of the topological phase through Griffiths' effects [135]. In the limit in which the clean topological gap $\Delta_{\rm T}$ is small compared to the Fermi energy, the stability condition for the topological phase is $\ell_{\rm loc} > \xi_{\rm T}$ [138], where $\ell_{\rm loc}$ is the localization length in the normal state and $\xi_{\rm T}$ is the coherence length in the clean topological superconductor. Equivalently, this can be rephrased in terms of energy scales as $\Delta_{\rm T}\tau > \hbar/2$, where τ is the elastic scattering time. In the effective model governed by $H = H_{\rm SM} + \Delta_{\rm ind} O_{\rm SC} + H_{\rm Dis}$, the scattering rate due to the random potential $V(x)$ can be evaluated to lowest order in δV:

$$\frac{\hbar}{\tau} = \frac{\delta V^2}{2E_{\rm F}} \frac{2k_{\rm F}\kappa}{1 + (2k_{\rm F}\kappa)^2}. \tag{A15}$$

Here, $E_{\rm F}$ and $k_{\rm F}$ are the Fermi energy and momentum. Thus, the transition at $\Delta_{\rm T}\tau = \hbar/2$ occurs at a critical value δV_c^2:

$$\delta V_c^2 = 4E_{\rm F}\Delta_{\rm T}[1 + (2k_{\rm F}\kappa)^2]/2k_{\rm F}\kappa. \tag{A16}$$

This expression for the critical disorder strength is valid in the regime of weak disorder and small gap, $\Delta_{\rm T} \ll E_F$. However, the nanowire in the single-sub-band regime has a small Fermi energy, so the latter requirement is difficult to satisfy. Moreover, disorder sources with correlation lengths $\kappa \gtrsim k_{\rm F}^{-1}$ cause stronger scattering than short-range disorder $\kappa k_{\rm F} \ll 1$, as may be seen from Eq. (A15). For realistic disorder levels, it is necessary to go beyond lowest order in δV [103]. Consequently, the precise location of the disorder-driven phase transition is more complicated than Eq. (A16) when the clean topological gap and disorder strength are comparable to the Fermi energy [103,141]. Finally, there are important differences between the thermodynamic limit and finite-sized systems, where the phase transition is rounded into a crossover. In order to understand these additional complexities, we calculate the disordered coherence length numerically using the transfer matrix method, as we discuss in the next two subsections.

3. Length scales and topological phases in finite systems

Since we are concerned in this paper with topological phases in finite systems with disorder, we must pay attention to several important length scales. We will denote the superconducting coherence length in the wire by $\xi(0)$. It is the distance that a zero-energy unpaired electron can penetrate into the proximitized nanowire. In the topological phase, $\xi(0)$ corresponds to the localization length of a Majorana zero mode. The coherence length $\xi(0)$ diverges at the phase transition between the trivial and topological superconducting phases. In the topological phase, when disorder is very weak, $\xi(0)$ approaches its clean value $\xi_{\rm T}$. Increased disorder elongates $\xi(0)$ in the topological phase, while it shortens $\xi(0)$ in the trivial phase.

In a perfectly clean system, there would be no states below the clean topological gap $\Delta_{\rm T}$, apart from the MZMs, and states above the gap would all be extended. However, even weak disorder localizes all states except the zero-energy state at the critical point, as noted in Sec. II A. It also causes localized states to appear below $\Delta_{\rm T}$. We will call the energy-dependent localization length, calculated for the Bogoliubov–de Gennes Hamiltonian (1), $\xi(E)$. At low energy, $\xi(E) \to \xi(0)$. When disorder is very weak, the density of states is very low for $E < \Delta_{\rm T}$, and these states have localization lengths that grow smoothly as a function of E, increasing from $\xi(0)$ to $\xi(\Delta_{\rm T})$. If $\xi(\Delta_{\rm T}) > L$, then states above $\Delta_{\rm T}$ will appear to be extended and there will be an apparent *transport gap* $\Delta_{\rm tr} \lesssim \Delta_{\rm T}$, which is the gap to "extended states," namely the states whose localization lengths $\xi(E)$ are larger than the system size. Turning now to the case of more general disorder strengths, we define $\xi(\Delta)$ as the maximum value of $\xi(E)$ for $E < \Delta_{\rm ind}$. Our devices are designed so that $\xi(\Delta) \gtrsim L$. When this holds, we can measure the transport gap $\Delta_{\rm tr}$, which is the minimum E for which $L/\xi(E)$ is small enough that states at energy E are visible in bulk transport. We explain these measurements in Sec. III and Appendix D 1.

The decay of subgap states at small energies $E \ll \Delta_{\rm T}$ is controlled by $\xi(0)$ while transport by excited states is controlled by $\xi(\Delta)$. Hence, if we observe a ZBP at one junction, the amplitude to observe it at the other junction decays as $e^{-L/\xi(0)}$, but if we observe an excited state of the bulk at one junction, the amplitude to observe the same state at the other junction decays at least as fast as $e^{-L/\xi(\Delta)}$.

Thus, depending on the disorder level and device length, there are three parameter regimes for the operation of a topological device. The first regime is when $\xi(0) < \xi(\Delta) \ll L$. In this limit, the device is longer than any of the finite length scales that characterize the topological phase. Hence, there is no characteristic energy scale of the bulk topological phase that can be extracted from transport measurements.

In the second regime, $\xi(0) \ll L \lesssim \xi(\Delta)$. In this regime, which we will call the asymptotic regime, the device is much longer than the localization length of a low-energy bound state. When ZBPs are observed at both junctions, we know that there are two distinct bound states, one at each junction. Since $L \lesssim \xi(\Delta)$, there are excited states that are effectively extended, i.e., have localization lengths that are comparable to or longer than the system size. The transport gap is the energy gap to such states.

Finally, there is a third regime, in which $\xi(0) \lesssim L \lesssim \xi(\Delta)$. This is a crossover regime in which the system is longer than the MZM localization length but it may not be so much longer that we are in the asymptotic limit. In this case, there may be some bulk transport at zero energy even when $\Delta_{\rm tr} > 0$ because the $e^{-L/\xi(0)}$ contribution is not negligible. Consequently, the system will be intermediate between the asymptotic regime and the critical regime that we define in the next paragraph. As $\xi(0)$ is reduced, the system will move more firmly into the asymptotic topological regime. However, there is not a particular value of the ratio $L/\xi(0)$ that separates the crossover regime from the asymptotic regime; the evolution from one to the other with increasing $L/\xi(0)$ is smooth.

None of the three regimes mentioned above, thermodynamic, asymptotic, and crossover, are possible near the critical point, where $\xi(0) = \infty$. When $L \ll \xi(0)$, the system is in the critical regime, and we cannot distinguish it from a critical system. Even in a device of length $L = 3\,\mu$m, this is a fairly broad region. As we shall see, for intermediate disorder

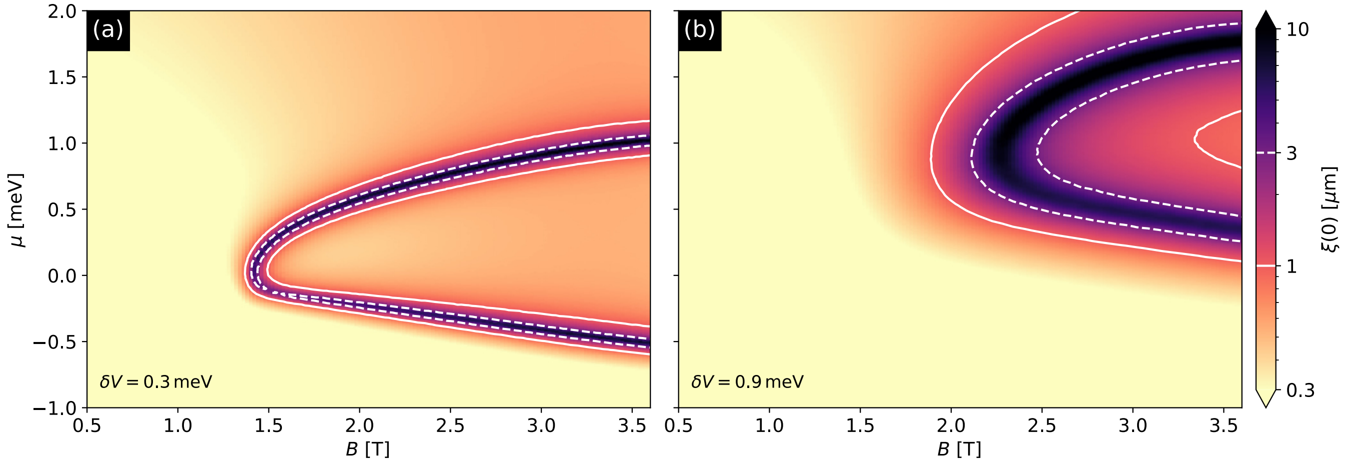

FIG. 24. The coherence length $\xi(0)$ evaluated numerically by the transfer matrix method for the model in Eq. (A12) with DLG, ε-stack parameters from Table I, and characteristic disorder strengths (a) $\delta V = 0.3$ meV and (b) $\delta V = 0.9$ meV. The color scale saturation highlights the divergence of $\xi(0)$, indicating the phase transition from the low-field trivial phase to the high-field topological phase. The solid and dashed lines mark contours of constant $\xi(0) = 1$ and $3\,\mu\text{m}$, respectively. For our $3\,\mu\text{m}$ simulations in Sec. II F, the region enclosed by dashed lines roughly represents the "critical" regime, while the area between dashed and solid lines is in the "crossover" regime where $L > \xi(0)$, but we still expect finite-size effects and mesoscopic fluctuations.

strengths, over much of the parameter range in which the system would be in the topological phase for $L \to \infty$, the system is in the critical regime because the correlation length is long and $L \ll \xi(0)$.

As an illustration of these various regimes, we calculate $\xi(0)$ for the model Eq. (A12) using the transfer matrix method [146]. In Fig. 24 we plot the result for DLG, ε-stack parameters from Table I and characteristic disorder strengths $\delta V = 0.3$ and 0.9 meV. As $\xi(0)$ is a function of the chemical potential and applied magnetic field, a finite wire can go from the critical to crossover to asymptotic regimes depending on these parameters. When the system is in the thermodynamic, asymptotic, or crossover regimes, it is deep in a $\Delta_{\text{tr}} > 0$ phase. The devices discussed in this paper are in the asymptotic or crossover regimes. We discuss the implications for transport measurements when we described the topological gap protocol in Sec. III and Appendix D 1.

4. Finite-size behavior of topological invariants

We now consider the finite-size behavior of the invariants distinguishing the topological and trivial phases. We consider the "scattering invariant" [111] and the Pfaffian invariant [9,99]. The scattering invariant is defined for an open system with a junction to a normal lead: $\text{SI} = \text{sgn}\det r \in [-1, 1]$, where r is the reflection matrix. When $\text{SI} = -1$, there is an MZM at the junction. The scattering matrix r depends on how open or closed the junction is. In a finite-sized system, an MZM at a junction will hybridize with the MZM at the other end of the wire with strength $e^{-L/\xi(0)}$ (giving $\text{SI} = +1$) unless it is coupled more strongly to the lead. If the MZM couples poorly to the leads, then we will erroneously find $\text{SI} = +1$. If the MZM couples more strongly to the lead than to its partner at the other end, then we will have $\text{SI} = -1$ in a finite-size system. Note, however, that we will also find $\text{SI} = -1$ if the second MZM is much closer than distance L but has small hybridization with the one at the junction, namely, the "quasi-MZM" scenario [46–49,51]. The Pfaffian invariant $\mathcal{Q}$ is defined for a closed system as the relative sign of the ground state parity between periodic (PBC) and antiperiodic (APBC) boundary conditions. $\mathcal{Q} = \text{sgn}[\text{Pf}(A_{\text{PBC}})]\,\text{sgn}[\text{Pf}(A_{\text{APBC}})]$ when the Bogoliubov–de Gennes Hamiltonian is written in terms of real fermionic operators $\gamma_{2i-1} = c_i + c_i^\dagger$, $\gamma_{2i-1} = -i(c_i - c_i^\dagger)$ so that it takes the form $H = (i/2)\sum_{i,j} A_{ij}\gamma_i\gamma_j$. In a finite system, we will have $\mathcal{Q} = -1$ when the hybridization of the two MZMs is larger via the periodic boundary condition that connects the two ends than the $e^{-L/\xi(0)}$ hybridization that occurs through the bulk of the wire. In summary, both invariants rely on $e^{-L/\xi(0)}$ being smaller than the coupling to the lead or the boundary condition. This is the limit in which the topological phase can be defined; it becomes more clearly distinct from the trivial phase in a continuous fashion as $e^{-L/\xi(0)} \to 0$. In the next section, we will use the Pfaffian invariant to illustrate the combination of finite-size effects and disorder on the phase diagram. In Appendix E 3, we will use the scattering invariant to test the accuracy of the TGP because the scattering invariant can be calculated for the same device geometry and junction settings as used in transport simulations and measurements.

APPENDIX B: ELECTROSTATIC CALIBRATION FROM HALL BARS

Each of the topological gap devices described in the main text is accompanied by a Hall bar device subject to the same growth and fabrication processes; this Hall bar enables a characterization of the bulk material quality. The full density dependence of the Hall mobility has been widely used previously to identify and quantify dominant scattering mechanisms in 2DEGs [109,145,147–154]. In particular, across all samples, the low-density mobility rapidly increases with increasing density, consistent with the mobility being dominated there by scattering from the long-range Coulomb potential of remote impurities.

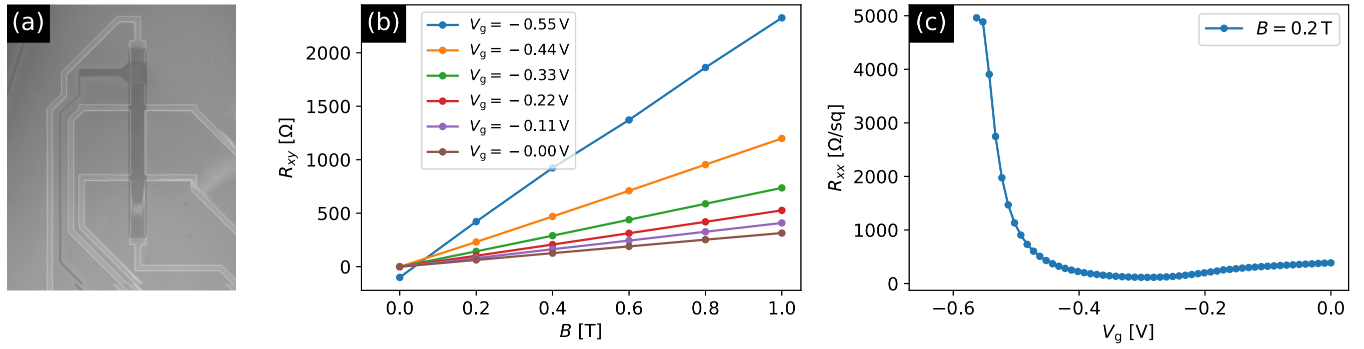

FIG. 25. Measurements of transverse and longitudinal resistance in the Hall bar device proximate to device A. These raw data underpin the density and mobility data used in the impurity density extraction. (a) Image of the Hall bar device on the same chip as device A. (b) Transverse resistance (R_{xy}) as a function of the applied magnetic field at selected top gate V_g voltages. (c) Longitudinal resistivity as a function of applied top gate voltage V_g at $B = 0.2$ T to avoid effects due to weak antilocalization. Different colors correspond to sweeps down (blue) and up (orange) from $[V_{th}, V_{sat}]$, and down (green) and up (red) from $[V_{th} - 0.5\text{ V}, V_{sat}]$ where V_{th} is the threshold voltage and V_{sat} is the saturation voltage of the Hall bar.

In our simulations, we calculate (i) the gate-voltage dependence of carrier density $n_e(V_g)$ for a 2DEG in our materials stack in a standard Schrödinger-Poisson framework; and (ii) the remote-impurity-limited mobility $\mu(V_g)$ in the Boltzmann-Born formalism. Both of these functions are parametrized by the density and location of impurities, and an effective composite dielectric permittivity. These parameters are used to *simultaneously* fit the model traces to experimental data. As mentioned in the main text, our best fits to density and mobility measurements over a variety of samples suggested a simplification in which an effective 2D impurity density $n_{2D,int}$ is placed in an "impurity layer" at the interface between the barrier and the gate dielectric. Small changes in the position or width of the impurity layer can be compensated by tuning the impurity density, but large changes modify the overall density dependence of the mobility and result in poor fits. Therefore, the values of charge impurity density that we quote here depend on the disorder model employed, with the goal of this model being to provide a *consistent* description of the impact of fixed charges on *both* the Hall mobility and TGP measurements. Figure 25(a) shows an SEM image of a Hall bar used for 2DEG mobility measurements on the same chip as device A (with the proximity shown in the optical image in Fig. 5). Figure 25(b) shows the Hall resistance as a function of perpendicular field for a sequence of gate voltages, from which we extract the density as a function of gate voltage. Figure 25(c) shows the longitudinal conductance as a function of gate voltage. By combining Figs. 25(b) and 25(c), we obtain the mobility as a function of density.

Figure 26 shows the mobility versus density for this Hall bar proximate to device A [note that the low-density upturn in $n_e(V_g)$ and non-single-valued $\mu(V_g)$ arise due to a measurement artifact and these points are excluded from the fitting]. The solid black lines represent our point estimate traces corresponding to the most-probable values of the effective impurity density, $n_{2D,int} = 2.7\times 10^{12}/\text{cm}^2$, and effective dielectric permittivity.

Using similar analyses, we extracted the corresponding effective charged impurity densities at the interface with the dielectric for devices C–F yielding $1.1\times10^{12}/\text{cm}^2$, $10^{12}/\text{cm}^2$, $3.1\times10^{12}/\text{cm}^2$, and $3\times10^{12}/\text{cm}^2$, respectively.

APPENDIX C: LOCALIZATION LENGTH UNDER ALUMINUM

In this Appendix, we elaborate on the measurement of the localization length ℓ_{loc} in proximitized nanowires, which was briefly summarized in Sec. II E. We begin with the following observations. A modest in-plane magnetic field ($B \sim 1$ T) perpendicular to the wire will close the induced gap in all the segments of the semiconductor nanowire while the aluminum remains superconducting with a slightly suppressed parent gap $\Delta_{Al} \approx 200$ μeV. When this occurs, G_{RL} will be nonzero over the entire range of bias voltages from $V_b = 0$ to Δ_{Al}. At small bias, the typical nonlocal conductance G_{RL} depends on the length of the wire as $G_{RL}(V_b) = A\exp[-2L/\ell_{loc}(V_b)]$ and similarly for G_{LR}. To extract ℓ_{loc}, we will measure the nonlocal conductances of segments of different length L.

A schematic of the device used for this measurement is shown in Fig. 27. The device consists of a hybrid InAs/Al

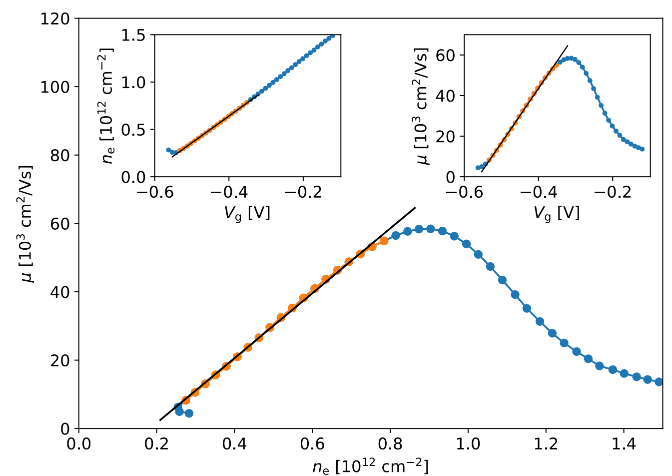

FIG. 26. Measured density and mobility vs gate voltage (as well as mobility vs density) from a Hall bar proximate to device A. Orange points indicate the low-density data used in the fit. Solid lines are the simulation result corresponding to the most-probable impurity density, $n_{2D,int} = 2.7\times10^{12}/\text{cm}^2$, and dielectric permittivity.

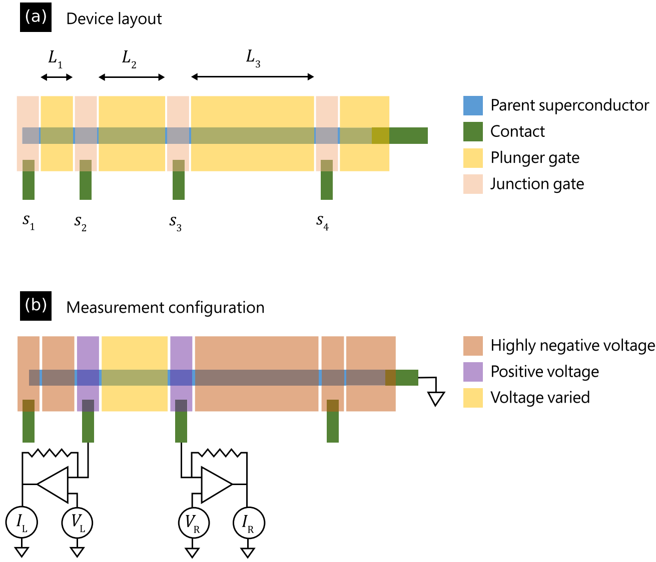

FIG. 27. (a) Schematic of a nanowire device design with multiple gate-defined sections of different lengths. Sources $s_{1\text{–}4}$ contact the semiconductor quantum well. (b) The measurement configuration to measure conductance of a single section. The junction gates for the section under measurement are set to a positive voltage to contact the semiconductor. The plunger gate of this section will be varied during the measurement and all other gates are set to highly negative voltages to deplete all semiconductor states as described in the main text. The nonlocal conductance is then measured with the aluminum nanowire grounded. This measurement is then repeated for all sections of the nanowire.

nanowire as described in the main text. Sections of different length are defined by the plunger gates, having $L_{1\text{–}3}$ in the schematic. Ohmic contacts are made to the semiconductor at several positions along the wire ($S_{1\text{–}4}$) and the coupling to the wire is controlled by junction gates. By measuring $G_{\rm RL}$ and $G_{\rm LR}$ between sources 3 and 4, we obtain these conductances for a wire of length $L = 1\,\mu$m. Between sources 2 and 3, a wire of length $L = 2\,\mu$m; between sources 2 and 4, a wire of length $L = 3.5\,\mu$m; sources 1 and 3, a wire of length $L = 6.5\,\mu$m; sources 1 and 4, a wire of length $L = 8\,\mu$m. The wire width, charged disorder $n_{\rm 2D,int}$, and junction transparencies are kept similar for different length wire segments. The latter is accomplished by opening the junctions to reduce the dependence of $G_{\rm RL}$ and $G_{\rm LR}$ on the disorder configurations within each of the junctions.

We now describe the measurement of the semiconductor conductance for the section between s_2 and s_3. The gate voltages are configured as illustrated in Fig. 27(b). The gates controlling the coupling between the contacts and the nanowire are set at a positive voltage, so that the semiconductor underneath these gates is in accumulation. In this configuration each source has approximately the same contact resistance to the semiconductor under aluminum.

As noted above, a modest in-plane magnetic field is applied so that the semiconductor enters the normal state while the aluminum remains superconducting. The nonlocal conductance is then measured between s_2 and s_3 while the aluminum is grounded. All gates outside the section under measurement are set to highly negative voltages so that no semiconductor states are populated. Transport is then allowed at energies below the aluminum gap between the two contacts, while carriers that tunnel through the barrier material into the aluminum are drained to ground and do not contribute to the measured conductance. This behavior can be seen in Fig. 6(a), the conductance is approximately zero at energies above the aluminum gap. At energies below the parent gap the conductance of the semiconductor is measured.

APPENDIX D: TGP SUBTLETIES

1. TGP measurements

First, to accelerate the search for ZBPs in Stage 1, rather then doing lengthy bias-voltage sweeps, we employ the third-harmonic (3ω) technique described in Ref. [155]. This gives a direct measurement of $d^3I_{\rm R}/dV_{\rm R}^3$, which is the curvature of the local conductance $dI_{\rm R}/dV_{\rm R}$. When $d^3I_{\rm R}/dV_{\rm R}^3$ is negative and above the noise level, it indicates the presence of a ZBP. Using this technique, we are able to scan over a large area in phase space by varying four parameters: $B, V_{\rm p}$, and the two cutter gate voltages $V_{\rm lc}$, $V_{\rm rc}$ that modulate the junction transparencies. We further facilitate this by restricting the cutter gate voltages so that $G_{\rm N}$ at each junction is limited to the range 0.1–1 e^2/h as a compromise between sufficient visibility and remaining in the tunneling regime. In Stage 2, we will also sweep $V_{\rm b}$, but will restrict $(B, V_{\rm p})$ to smaller ranges.

Second, $G_{\rm LR}$ and $G_{\rm RL}$ may receive contributions from line impedances in the measurement circuit, which we account for by taking the full impedance network into account [156]. In addition, we correct for finite-frequency effects by calibrating the resistances and capacitances in the measurement circuit, as explained in Appendix G. Finally, we remove any remaining voltage divider corrections and improve SNR by focusing on the parts of the nonlocal conductances that are antisymmetric in bias voltage, $A(G_{\rm RL})$, $A(G_{\rm LR})$:

$$A[(G_{\rm RL}(V_{\rm b})] \equiv [G_{\rm RL}(V_{\rm b}) - G_{\rm RL}(-V_{\rm b})]/2 \tag{D1}$$

and similarly for $G_{\rm LR}$. A discussion of relevant multiterminal conductance symmetry relations may be found in Ref. [157].

Third, the transport gap extracted from $A(G_{\rm RL})$ will not, in general, be the same as that extracted from $A(G_{\rm LR})$. The underlying transport gap is the same, but the two nonlocal conductances may not be the same due to the different ways in which local matrix elements enter $G_{\rm LR}$ and $G_{\rm RL}$. [We will see an example of this in simulated data in Figs. 29(b) and 29(c) in Appendix E 3.] This can obscure a gap narrowing or closing. Hence, for any given $V_{\rm p}$ and B, we determine the induced gap as the lower of the gaps extracted from $A(G_{\rm RL})$ and $A(G_{\rm LR})$. Consequently, the observation of nonvanishing $A(G_{\rm LR})$ *or* $A(G_{\rm RL})$ at bias voltages approaching zero is a signature of a bulk gap closing. Note that the energy spectrum can be gapless due to the presence of disorder-induced localized states at low energies. The observed transport gap, extracted from $A(G_{\rm LR})$ and $A(G_{\rm RL})$, is the gap that we really care about since it is more predictive of qubit performance.

A fourth subtlety is that $A[G_{\rm LR}(V_{\rm R})], A[G_{\rm RL}(V_{\rm L})]$ can be either positive or negative, depending on whether transport at

that bias voltage is primarily due to electrons or holes. It can change sign as the matrix elements change as a function of B or V_p, passing through zero when this occurs [110]. Such a sign change can appear as a very sharp increase in the induced gap, centered about some B or V_p value. In determining the zero-field induced gap, we simply avoid these points. The situation is slightly more complicated for the topological gap since it varies between zero at the phase transition and a maximum value that determines the stability of the topological phase. Hence, we will report both the median value of the gap over the SOI_2 and also its maximum value. However, we will not extract the maximum from the single point at which it is largest. It is not uncommon to have a very small region over which the extracted topological gap is very large because one of the aforementioned sign changes occurs, suppressing the signal in G_LR and G_RL. Hence, we define the "maximum topological gap" $\Delta_\mathrm{topo}^\mathrm{max}$ to be the upper quintile of measured gap values within SOI_2.

We add a note of caution here that the measured values of Δ_ind and $\Delta_\mathrm{topo}^\mathrm{max}$ are transport gaps, which are the lowest energy at which there is an excited state whose localization length is longer than the device length; they can be larger than the Δ_ind or $\Delta_\mathrm{topo}^\mathrm{max}$ expected for a clean system.

Fifth, we clarify the definition of the gapless boundary of an SOI_2. The boundary of the region is defined to consist of all points inside the SOI_2 that neighbor the exterior of the SOI_2 on the side or diagonally. Each such boundary point is then considered gapped if all of the neighboring points outside SOI_2 are gapped. Otherwise, the boundary point is considered gapless. Using this definition, we extract the fraction of the boundary points that are gapless.

2. TGP parameters

The TGP is parametrized by thresholds that were fixed by an initial set of calibration simulations described in Appendix E 2 and then tested extensively by large-scale simulations for different disorder levels and device designs, as described in Appendix E 1. As a result, we have high confidence that ROI_2s overlap with the regions in parameter space where there is a topological phase, as we quantify in Appendix E 1.

In principle, this protocol is designed to detect any topological phase with a sizable gap. Finite experimental resolution and temperature, however, may obfuscate some of the topological signatures, giving rise to subtleties when interpreting the data that we discuss here.

A wire may have MZMs, but one or both of them may be slightly displaced from the end of the wire for some choices of junction transparency and, therefore, may not be visible. [Indeed, we see in Fig. 2(c) that the local density of states can be peaked a few hundred nanometers away from the junction in a simulation of an ideal disorder-free device.] For this reason, we do not insist that a ZBP be present for all junction configurations and, instead, consider a ZBP to be stable in Stage 1 if it is visible for at least 70% of measured junction transparencies. We define the "cutter gate fraction" as the fraction of junction transparencies (or, equivalently, cutter gate settings) for which a ZBP is present. For instance, suppose we pick 5 cutter gate voltages V_rc at the right junction such that G_N at the right junction takes the values 0.35, 0.49, 0.62, 0.76, $0.9e^2/h$ and similarly pick 5 cutter gate voltages V_lc at the left junction so that G_N at the left junction ranges over the same five values. The precise sampling over cutter pairs varies between the measurements presented in this paper, but there are always at least 20 cutter gate voltage pairs. Then, a (B, V_p) point will be said to exhibit stable ZBPs at both junctions if there are ZBPs at both junctions for >70% of cutter gate pairs $(V_\mathrm{lc}, V_\mathrm{rc})$.

For Stage 2, we set a threshold percentage $(\mathrm{ZBP}\%)_\mathrm{th}$ and define a stable ZBP as one that is visible for at least $(\mathrm{ZBP}\%)_\mathrm{th}$ of junction transparencies. As we discuss further in Appendix E 2, we use calibration simulations to inform the choice $(\mathrm{ZBP}\%)_\mathrm{th} = 60\%$ for the device parameters considered in this paper. For the junction transparencies given as an example in the previous paragraph, we would perform Stage 2 measurements for 5 different cutter gate pairs $(V_\mathrm{lc}, V_\mathrm{rc})$ such that $G_\mathrm{N}^R = G_\mathrm{N}^L = 0.35, 0.49, 0.62, 0.76, 0.9e^2/h$. A stable ZBP in Stage 2 would then need to be present for 3/5 cutter gate pairs.

A gap closing may not be visible even when it is present because $A(G_\mathrm{RL})$ and $A(G_\mathrm{LR})$ tend to be small at low-bias voltage (due to their antisymmetry in bias voltage) and will be suppressed even further by disorder and nonuniformity. Another reason why an SOI_2 may be gapless along less than 100% of its boundary is that neighboring gapped regions may have been misidentified as nontopological (e.g., due to weak coupling of the MZMs to the leads or ZBP splitting due to a small topological gap). In case of such misidentification, such regions should actually be included in the SOI_2, which would be larger and gapless along its entire boundary. To account for both of these possibilities, we set a threshold percentage $(\mathrm{GB}\%)_\mathrm{th}$. In order to qualify as an SOI_2, a cluster must be gapless along at least $(\mathrm{GB}\%)_\mathrm{th}$ of its boundary. As we discuss in Appendix E 2, we use simulated transport data to inform the choice $(\mathrm{GB}\%)_\mathrm{th} = 60\%$ for the device parameters discussed in this paper.

The nonlocal conductances $A(G_\mathrm{RL})$ and $A(G_\mathrm{LR})$ will never truly vanish at zero bias because there will at least be tunneling $e^{-L/\xi(0)}$ and thermally activated $e^{-\Delta_\mathrm{tr}/T}$ contributions.[10] Hence, we need to give an operational definition for $A(G_\mathrm{RL}) \approx 0$ and $A(G_\mathrm{LR}) \approx 0$. To do this, we define a threshold value G_th. Then, if $A[G_\mathrm{LR}(V_\mathrm{R})]$, $A[G_\mathrm{RL}(V_\mathrm{L})] < G_\mathrm{th}$, we interpret this as $A[G_\mathrm{LR}(V_\mathrm{R})]$, $A[G_\mathrm{RL}(V_\mathrm{L})] \sim O(e^{-L/\xi(0)}, e^{-\Delta/T})$. The extracted gap is obtained using the highest bias voltage V_b below which $A[G_\mathrm{LR}(V_\mathrm{b})] < G_\mathrm{th}$ and $A[G_\mathrm{RL}(V_\mathrm{b})] < G_\mathrm{th}$. The choice of G_th should depend on Δ/T and $L/\xi(0)$ and also on the transparency of the junctions. For the disorder strengths expected in our devices, we take G_th equal to $\exp(-3) \approx 0.05$ times the maximal value $\max\{G_\mathrm{NL}\}$ of the nonlocal conductance at bias voltages greater than the induced gap (scanning over all B for each V_p for a given cutter configuration). As we discuss later in this section, this choice of G_th was set by applying the TGP to calibration data from simulated devices with $n_\mathrm{2D,int} = 2.4\times10^{12}/\mathrm{cm}^2$. For weaker disorder $n_\mathrm{2D,int} \ll 10^{12}/\mathrm{cm}^2$, the optimal value of G_th should be smaller because $L/\xi(0) \gg 1$

[10] See also Ref. [158] for additional considerations that are relevant to the nonlocal conductance.

and the transition becomes sharper in this limit. If we do not take a smaller $G_{\rm th}$, the TGP will miss gap closings and will erroneously interpret $A(G_{\rm RL})$ and $A(G_{\rm LR})$ data as indicating that the gap remains open. Defining $G_{\rm th}$ in terms of the high-bias conductance $\max\{G_{\rm NL}\}$ enables us to define it equally well for simulated data as for measured data (unlike, for instance, a $G_{\rm th}$ that depends on the noise level in a particular measurement setup). When we plot either simulated or measured $A[G_{\rm LR}(V)]$, $A[G_{\rm RL}(V)]$, we will use a black curve to indicate the bias voltage (as a function of B field) below which each one is less than $G_{\rm th}$ [see, e.g., Figs. 29(e) and 29(f)]. We can restate the threshold defined in this paragraph as follows: There is a truly sharp distinction between the trivial and topological phases only in the infinite-size, zero-temperature, and infinitesimal transparency limits; hence the threshold gives a simulation-tested method for finding the rounded transition.

Finally, we note that the extracted transport gap and, therefore, the phase diagram depend on the junction transparencies (and, thereby, on the cutter gate voltages that control them). The phase diagram must be stable to changes in the cutter gate voltages in the following sense: we require that a device passing the TGP must have a $\mathcal{C}_i^A \in T$ for a threshold percentage $(\mathcal{C}_i\%)_{\rm th}$ (see below) of cutter gate pairs i. In other words, in order to pass the TGP, a fraction $(\mathcal{C}_i\%)_{\rm th}$ of cutter gate settings must have at least one $\mathcal{C}_i^A$ that is a subset of the ROI_2. We will take $(\mathrm{C}_i\%)_{\rm th} = 50\%$. This combination of the stability thresholds for ZBPs, gap closing and reopening requirements, and the overlap of the resulting SOI_2 is sufficient to virtually eliminate false positives when analyzing simulated data, as we shall see below in Appendix E 1.

APPENDIX E: CALIBRATING AND TESTING THE TGP WITH DATA FROM SIMULATED DEVICES

In this Appendix, we use simulations to quantify the reliability of the TGP. Our transport simulations begin with three-dimensional models of the devices in Figs. 2 and 3 that include the electrostatic environment defined by the set of gate voltages. We identify the $V_{\rm p}$ range for which the chemical potential is in the lowest sub-band and the cutter gate voltages for which the junction transparencies take the 5 values $G_{\rm N} = 0.35, 0.49, 0.62, 0.76, 0.9e^2/h$. The resulting single-sub-band parameters are given in Table I and Fig. 23. For this gate voltage set, we perform transport simulations and calculate the scattering matrix of the system. The local and nonlocal conductances $G_{\rm LL}, G_{\rm RR}, G_{\rm LR}, G_{\rm RL}$ are then obtained by convolution with the derivative of the Fermi function at temperature T. We analyze these data according to the TGP according to the same procedure that we will use in Sec. IV to analyze experimental data.

1. False discovery rate

The basic question that we wish to answer is as follows: Suppose the TGP returns an ROI_2 that passes; what is the probability that it does *not* have any overlap with the topological phase? The goal of TGP calibration is to set thresholds that minimize this probability. Once the TGP has been calibrated, we test it to assess whether this probability is low when the TGP is applied to a range of device types and parameters: different junction designs, different material parameters such as spin-orbit coupling, different disorder strength.

To compute this probability in simulations, we compare ROI_2s with a topological index (the "scattering invariant" [111]). We classify ROI_2s as follows: if an ROI_2 has any overlap with a region of the simulated phase diagram with scattering invariant -1, then we will call it a true positive; otherwise, it is a false positive. In Sec. III [see Eq. (4)], we defined the classification of regions as TP and FP, and derived the FDR from these numbers in order to quantitatively measure the reliability of the TGP.

Note that this is a classification of regions, rather than a classification of devices. Hence, if a device that does have a topological region were to pass the TGP but its ROI_2 were completely disjoint from the topological region, then this ROI_2 would be a false positive. We do not attempt to count negative regions: an arbitrary region is very likely to be negative, so the number of negative regions is not a useful statistic.[11] Therefore, we do not compute the false positive rate (FPR), given by FP/(FP + TN), where TN is the number of true negatives. The FPR is less useful for the present discussion.

There is a further subtlety, which is that the scattering invariant depends on the junction transparencies. Since our device has two junctions, the scattering invariant can be defined at either one: $\mathrm{SI}_i = \mathrm{sgn}\det r_i \in [-1, 1]$, where r_i is the reflection matrix and $i = \mathrm{L, R}$. When the junctions are completely closed, both SI_i are trivially equal to $+1$. When the junctions are opened, $\mathrm{SI}_i = -1$ regions can appear, and they tend to grow as the junctions are opened further. Thus, we must decide how to assign a topological index to a finite system. We will define the topological region of the phase diagram as the union of the $\mathrm{SI}_i = -1$ regions over $i = \mathrm{L, R}$ and the 5 different pairs of junction transparencies used in TGP Stage 2. We will call this union the "$\mathrm{SI} = -1$ region." Instead of taking the union of the $\mathrm{SI}_i = -1$ regions, we could have taken the intersections. In our simulations, $\mathrm{SI}_{\rm R} = -1$ and $\mathrm{SI}_{\rm L} = -1$ regions overlap but not completely. For some cutter gate settings, only $\mathrm{SI}_{\rm R} = -1$ while for others $\mathrm{SI}_{\rm L} = -1$ because a zero-energy state can couple poorly to the lead at one junction or the other for different cutter gate settings. Our definition of the topological index is relatively insensitive to these details of the junctions. If we had wanted to use the Pfaffian invariant [9], we would have had to truncate the system to remove the junctions and then imposed periodic/antiperiodic boundary conditions. This would no longer be the same device as we would be probing in transport.

A final technical detail: the conductance matrix is temperature dependent, and the output of the TGP has a resulting temperature dependence. As we discuss in Sec. IV, the base temperature of our dilution refrigerators during these measurements is 20 mK, and the electron temperature is estimated to be $\lesssim 40$ mK. We use transport data at 30 mK for our

[11] On the other hand, a "negative device," which is a device that fails the TGP, is a natural concept. We return to it later when we define the TGP yield, which is the probability that a *device* will pass the TGP: in other words, the complement of the probability of a negative device.

calibration simulations. We test the TGP using simulated data at 40 mK, and we used these simulated data in our estimates of the FDR and other statistical properties.

The main result of the subsections that follow is that we estimate that the FDR is $\leqslant 8\%$ at a 95% confidence level for all device designs, material stacks, and disorder levels simulated. Thus, when a device passes the TGP, there is $>92\%$ probability that it has a nonzero gap and $\mathrm{SI} = -1$. The details are in Table II.

2. Setting the TGP thresholds

As discussed in Appendix D 2, there are three key thresholds which parametrize the TGP: $(\mathrm{ZBP}\%)_{\mathrm{th}}$, $(\mathrm{GB}\%)_{\mathrm{th}}$, and G_{th}. We choose these parameters so that the TGP has a low FDR. If we were to make it very difficult to pass the TGP, then we would have very few false positives but also few true positives, and the FDR could be large. If we make it too easy to pass the TGP, then will have many more true positives but also more false positives. However, the right choices of $(\mathrm{ZBP}\%)_{\mathrm{th}}$, $(\mathrm{GB}\%)_{\mathrm{th}}$, and G_{th} lead to a TGP which is reliable because it has low FDR.

We performed an initial calibration of the TGP by analyzing simulated transport data at $T = 30$ mK from 28 disorder realizations of an SLG-β device with an average charged defect density of $n_{\mathrm{2D,int}} = 2.4\times10^{12}/\mathrm{cm}^2$ and spin-orbit interaction $\alpha \simeq 13$ meV nm. We did not find any false positives: every ROI_2 has at least some subset with $\mathrm{SI} = -1$. However, the number of true positives and, hence, the FDR varies with the threshold values. We find that $(\mathrm{ZBP}\%)_{\mathrm{th}} = 60\%$, $(\mathrm{GB}\%)_{\mathrm{th}} = 60\%$, and $G_{\mathrm{th}} = 0.05\max\{G_{\mathrm{NL}}\}$ is close to optimal. There are 53 ROI_2s spread across the 28 devices (all true positives) for these threshold settings. Hence, the FDR is $<6.7\%$ at the 95% confidence level. Had $(\mathrm{ZBP}\%)_{\mathrm{th}}$ and $(\mathrm{GB}\%)_{\mathrm{th}}$ been set lower, we would have found ROI_2s that did not contain a region with $\mathrm{SI} = -1$. For higher $(\mathrm{ZBP}\%)_{\mathrm{th}}$ and $(\mathrm{GB}\%)_{\mathrm{th}}$, we would have had fewer devices passing the TGP. If we had set G_{th} too low, then too much of the phase diagram would have been classified as gapless, thereby concealing gap reopenings. If we had set G_{th} too high, then too much of the phase diagram would have been classified as gapped, obscuring gap closings. Note that the two thresholds $(\mathrm{GB}\%)_{\mathrm{th}}$ and G_{th} are correlated.

We show two realizations of simulated SLG, β-stack devices in Appendix E 5, one that passes the TGP and one that fails.

3. Testing the TGP

With the TGP thus calibrated and validated, we turn to simulations estimating the FDR. Since we will be analyzing experimental data from devices with different designs, material stacks, and disorder levels, we apply the TGP to simulated SLG-β and DLG-ε devices with several different charge disorder levels. For charge disorder given by $n_{\mathrm{2D,int}} \geqslant 10^{12}/\mathrm{cm}^2$, we use the thresholds obtained in the calibration described above, whereas in the cleaner case of $0.1\times10^{12}/\mathrm{cm}^2$ we lower G_{th} from 0.05 to 0.01 while leaving the other thresholds unchanged. Although the *optimal* values of the thresholds in the TGP depend on the temperature, design, material stack, and disorder level, our goal here is to show that, for the thresholds chosen, the TGP remains *reliable* across a range of designs, material stacks, and disorder levels, and at a slightly higher temperature. The motivation is that we would like to apply the TGP in cases in which neither the electron temperature nor the disorder level is known precisely. Note, however, that if either the disorder level or temperature were very different, then we would probably need to adjust $(\mathrm{ZBP}\%)_{\mathrm{th}}$, $(\mathrm{GB}\%)_{\mathrm{th}}$, and G_{th}.

To estimate the FDR, we performed large-scale simulations involving 349 different disorder realizations, distributed across SLG-β and DLG-ε devices with intermediate to strong disorder levels defined by charge impurity densities of 0.1, 1, 2.7, and 4 in units of $10^{12}/\mathrm{cm}^2$, as shown in Table II. The Hall bar measurements described in Appendix B indicate that the devices experimentally measured in this paper have $n_{\mathrm{2D,int}}$ values in this range. The defect density $n_{\mathrm{2D,int}} = 2.7\times10^{12}/\mathrm{cm}^2$ is the largest of any of the measured devices reported in this paper that has passed the TGP, while $n_{\mathrm{2D,int}} = 4\times10^{12}/\mathrm{cm}^2$ is larger than in of any of the devices reported in this paper, including those that failed the TGP. Several of our measured devices have $n_{\mathrm{2D,int}}$ values at or below $10^{12}/\mathrm{cm}^2$.

We calculate the conductance matrix (2) for each simulated disorder realization at $T = 40$ mK and analyze these data according to the TGP, as we would with experimental data. This analysis yields ROI_2s; many disorder realizations, especially with stronger disorder, have none, while some disorder realizations, typically with weaker disorder, have multiple ROI_2s. We compare these ROI_2s to the scattering invariant and classify each ROI_2 as a TP or FP depending on whether any subregion of the ROI_2 has $\mathrm{SI} = -1$. We find the statistics given in Table II. From the TP and FP values obtained from these simulations, we estimate the FDR by assuming a binomial distribution and use the Clopper-Pearson confidence interval at a 95% confidence level.

We do not have a single false positive in these data. This does not mean that the TGP perfectly identifies the topological region. Our results show that the TGP identifies an ROI_2 that has nonzero overlap with the $\mathrm{SI} = -1$ regions in the phase diagram. However, part of the ROI_2s identified by the TGP do not have $\mathrm{SI} = -1$ and much of the $\mathrm{SI} = -1$ region lies outside the ROI_2, as we will see in the examples that we discuss in Appendix E 4 and Appendix E 5. This is not surprising since, as we discussed in Appendix A 4, there is some inherent ambiguity in defining the topological phase in a finite system. When we restrict the magnetic field to $B \leqslant 2.5$ T, we find one false positive for an SLG-β device with $n_{\mathrm{2D,int}} = 1.0\times10^{12}/\mathrm{cm}^2$. By restricting the magnetic field, the normalization of the conductance changes slightly, and a candidate SOI_2 for one cutter gate setting is classified as gapped with a very small gap; for a larger B-field range, it is classified as gapless and the regions fail the TGP.

Our analysis of the FDR indicates that TGP reliably identifies an $\mathrm{SI} = -1$ region for different disorder levels and for different device designs. Indeed, as summarized in Table II, there are only small differences in the estimated FDR values for the above-mentioned parameters, and they are primarily due to the different numbers of ROI_2s for various disorder levels. Thus, the TGP at these threshold values can be applied

TABLE V. The analogous table to Table IV with magnetic field restricted to the range $B \leqslant 3$ T.

Design, stack	$n_{\rm 2D,int}$ $[10^{12}/\mathrm{cm}^2]$	Yield $\leqslant$3 T	$\bar{\Delta}_{\rm topo}^{\rm max}$ [μeV]	$\bar{\mathcal{V}}_{\rm SOI2}$ [mV T]	$\bar{B}_{\rm SOI2}$ [T]
SLG-β	1.0	48/50	23	0.2	2.1
	2.7	24/50	34	0.1	1.5
	4.0	26/49	36	0.1	1.5
DLG-ε	0.1	48/50	26	0.2	2.6
	1.0	43/50	29	0.2	2.6
	2.7	33/50	28	0.2	2.6
	4.0	35/50	28	0.2	2.6

to a large class of topological gap devices with intermediate disorder strength.

Our simulations also give us information about how the disorder level and device design affect the probability that a device will pass the TGP. We define the *TGP yield* as this probability:

$$\text{TGP yield} \equiv P(\text{Device passes TGP}). \tag{E1}$$

As may be seen from Table IV, the TGP yield depends strongly on $n_{\rm 2D,int}$. More disordered devices are less likely to pass the TGP because they are less likely to have a topological phase.

We now consider the statistics of the SOI_2s that the TGP finds. Table IV shows these statistics when the magnetic field is restricted to $B \leqslant 2.5$ T, while $B \leqslant 3$ T in Table V. We find that $\Delta_{\rm topo}^{\rm max}$ has mean value $\bar{\Delta}_{\rm topo}^{\rm max}$ that varies between 25 and 35 μeV for different disorder strengths and has a non-Gaussian distribution with long tails towards larger gap. A smaller mean value is observed at the lowest disorder levels because there are significantly more SOI_2s at weak disorder, and many of them have small $\Delta_{\rm topo}^{\rm max}$. The mean volume in the B-$V_{\rm p}$ parameter space of an SOI_2, denoted $\bar{\mathcal{V}}_{\rm SOI2}$, is of the order 0.1 mV T and decreases with increasing disorder strength (see Table IV). As with $\bar{\Delta}_{\rm topo}^{\rm max}$, the distribution of $\bar{\mathcal{V}}_{\rm SOI2}$ is non-Gaussian with long tails. Finally, the average B field at which we observe SOI_2s ranges between 1.5 and 2.6 T. As expected, ε-stack devices have SOI_2s that occur at higher magnetic fields >2 T since they have larger $\Delta_{\rm ind}$ and smaller $g^\star$.

4. Example of the TGP applied to a single disorder realization

To illustrate the TGP, we now focus on a particular disorder realization in a narrow 3 μm long device based on the DLG, ε-stack design. This is one of the devices that appears in Tables II and IV. We will call this simulated disorder realization DLG-ε-R1 for brevity. We have applied the TGP to $T = 40$ mK transport data for this device, which we discuss in detail below, explaining the different stages of the TGP through this example. We also compare an SOI_2 identified by the TGP with the topological region determined by SI $= -1$. In Appendix E 5, we discuss simulated data from two other devices that we call realizations SLG-β-R1 and SLG-β-R2.

Stage 1: Stage 1 focuses on ZBPs in the local conductance. From the local conductances $G_{\rm RR}$ and $G_{\rm LL}$, we can map out the regions in $(B, V_{\rm p})$ space where there are stable ZBPs at the two junctions, where "stable" means that the ZBPs are present for a cutter gate fraction >70%, as described in Appendix D 2. For simulated disorder realization DLG-ε-R1, the locations of stable ZBPs at the left junction are shown in Fig. 28(a) and at the right junction in Fig. 28(b). A topological phase should have stable ZBPs at both junctions at the same B and $V_{\rm p}$, so Fig. 28(c) shows the phase space locations where there are stable ZBPs at both junctions. This is the output of Stage 1 of the TGP. The entire gate voltage range shown here, $-0.735\ \mathrm{V} \leqslant V_{\rm p} \leqslant -0.665$ V, lies within the lowest sub-band. There is a trivial zero-energy state at the left junction over a region in the B-$V_{\rm p}$ plane that traces out a parabolic shape starting around $(B, V_{\rm p}) = (1.2\ \mathrm{T}, -0.69\ \mathrm{V})$. However, this ZBP is unstable (i.e., fine-tuned) with respect to cutter changes and, therefore, is filtered out by the TGP. The ROI_1 identified by the TGP is a smaller region at higher B and lower $V_{\rm p}$ where there are stable ZBPs at both junctions.

Stage 2: In Stage 2, we focus on the neighborhood of the ROI_1 identified in Stage 1. Stage 2 analyzes local and nonlocal transport data over a range of bias voltages. In the simulated data, unlike in the experimental data discussed in Sec. IV, there is no drift of the plunger gate voltage $V_{\rm p}$, so the ROI_1 is automatically recovered from local transport data. However, we do obtain the dependence of $G_{\rm RR}$ and $G_{\rm LL}$ on the bias voltage, as seen in Figs. 29(c) and 29(d). The more significant new ingredient in Stage 2 is the bias dependence of the nonlocal conductances $G_{\rm RL}$ and $G_{\rm LR}$, from which we determine the transport gap as a function of B and $V_{\rm p}$. For simulated disorder realization DLG-ε-R1, the nonlocal conductances $G_{\rm RL}$, $G_{\rm LR}$ and the derived gap (indicated by black curves) as a function of B for $V_{\rm p} = -0.7205$ V are shown in Figs. 29(e) and 29(f). We give 5 significant digits after the decimal point for $V_{\rm p}$ so that these values can serve as indices in the relevant data files; this may be convenient for readers wishing to look directly at the data underlying the figures in this paper. Note that this cut passes through the topological phase transition and the topological phase; a gap closing and reopening is seen in $G_{\rm RL}$ and $G_{\rm LR}$. Combining the local and nonlocal information, we can classify any point in phase space as gapped without stable ZBPs, gapped with stable ZBPs, gapless without stable ZBPs, or gapless with stable ZBPs. These are depicted in Fig. 29(a) as, respectively, blue, orange, white, or yellow. If an orange region is surrounded by white or yellow along more than 60% of its boundary, we identify it as an SOI_2, and give it a black boundary in Fig. 29(a).

In addition to stable ZBPs, we also observe some zero-energy states that have a nontopological origin, as noted in our Stage 1 analysis. These trivial Andreev bound states (ABS) can be caused by resonances arising from the local electrostatic potential, local disorder, or a combination. We give some examples of their spectroscopy in Appendix E 5. While the presence of these ABSs can be limited by careful design of the junctions, they can never be fully suppressed. When running the TGP in experiments, we take care to tune away from pathological points in junction phase space as much as possible, while stepping between different junction configurations as we tune $G_{\rm N}$ to span from $0.1e^2/h$ to e^2/h.

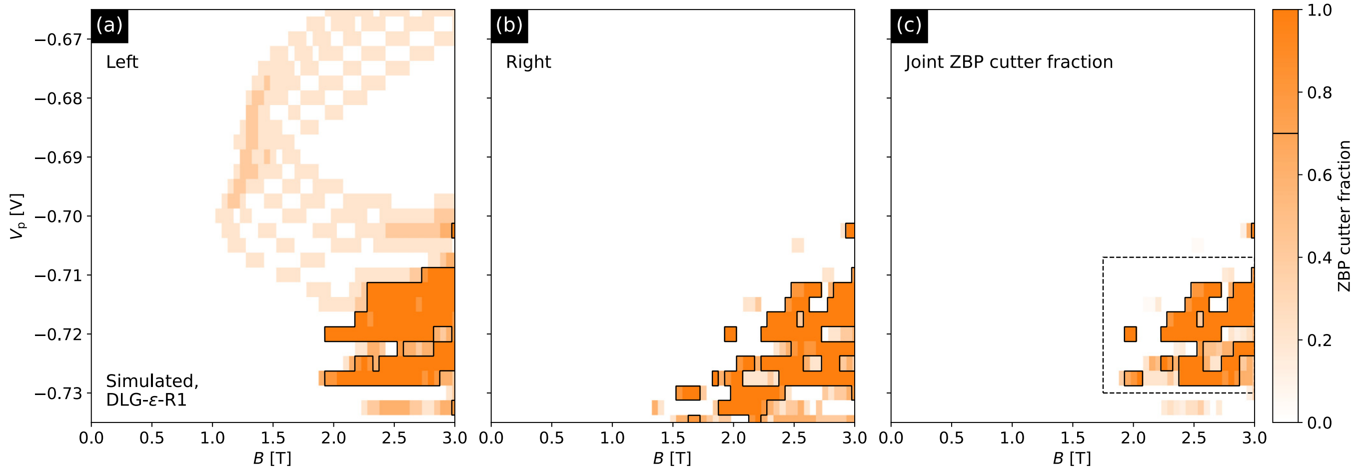

FIG. 28. The TGP applied to simulated transport data for DLG with $n_{2D,\text{int}} = 10^{12}/\text{cm}^2$ and 40 mK temperature broadening, highlighting regions of phase space with stable ZBPs in (a) G_{LL} and (b) G_{RR}. (c) Regions of phase space with stable ZBPs in both G_{LL} and G_{RR}. Simulated transport data such as this are used to test the TGP. Here, we show one particular disorder realization for illustrative purposes. Any possible visible resemblance to measured data is dependent on the disorder realization and does *not* play a role in our analysis.

As we can see in Figs. 29(a) and 29(b), the TGP finds a region of topological phase [shown in orange in Fig. 29(a) and red in Fig. 29(b)] around $B = 2.55$ T, $V_p = -0.72$ V with a maximum topological gap $\Delta_{\text{topo}}^{\max} = 41$ μeV, which is the upper quintile of the gaps extracted in the SOI_2.

The topological gap increases from zero at the phase transition to $\Delta_{\text{topo}}^{\max}$ in such a way that its median value over the red region within the black line in Fig. 29(b) is 26 μeV. The TGP phase diagram is compared with the scattering invariant. In Fig. 29(a), the region with SI $= -1$ is hatched. As may be seen in Fig. 29(a), the region identified by the TGP lies almost entirely within the region with negative topological index, i.e., the TGP is fairly conservative and identifies a subset of the topological phase. It is not a perfect match, of course, since the TGP is not directly calculating the scattering invariant and, moreover, the phase transition is rounded by finite temperature and finite-size corrections. Note the similarity between the hatched regions with negative topological index in Fig. 29(a) and the bright orange regions. The regions that pass the TGP are smaller *pockets* within these splinters.

Figure 29(b) is another version of the phase diagram for this disorder realization: it shows the transport gap extracted from G_{RL} and G_{LR} multiplied by $q = \pm 1$, depending on whether that point lies outside or inside the SOI_2. Note that q is *not* the same as the topological invariant $\mathcal{Q}$ that is used analogously in the color scale in Fig. 4 (where $\mathcal{Q}$ is the Pfaffian invariant); rather, q is the proxy for $\mathcal{Q}$ that results from the TGP. The color scale of Fig. 29(b) can be viewed intuitively as the magnitude of the bulk gap multiplied by a proxy for the sign of the topological invariant. Darker red corresponds to larger topological gap.

As expected, there are some points along the boundary of the SOI_2 where the closing is not visible in either G_{RL} or G_{LR}. For this cutter gate pair in this particular disorder realization, 67% of the boundary of the SOI_2 shows a gap closing in G_{RL}, G_{LR}, which is above $(\text{GB}\%)_{\text{th}}$.

A comparison between the orange region in Fig. 29(a) and the hatched region lends credence to the idea that the part of the boundary that is gapped is not actually a boundary at all, and the true boundary is at higher B and lower V_p. The blue region below and to the right of the orange region is hatched, indicating that it has been misclassified as nontopological. However, as may be seen in Fig. 29(b), this gapped (and ostensibly topological) region below and to the right of the SOI_2 is light blue, indicating that it has a small gap. Hence, if it were topological, it would have a small topological gap and would not be useful for a topological qubit, in contrast to the darkest red regions within the SOI_2. The same observation applies to all of the hatched SI $= -1$ region that lies outside of the SOI_2: it may be topological, but it has a small transport gap. Moreover, since they do not have stable ZBPs in G_{LL} and/or G_{RR}, it is unlikely that it would be possible to couple to these ZBPs in a qubit.

In this section, we discussed a disorder realization for a DLG-ε device that passed both stages of the TGP and correctly found the topological phase. In Appendix E 5, we will show additional data from calibration simulations and discuss examples that fail the TGP.

5. Simulated disorder realizations used for the calibration of TGP

In this Appendix, we discuss two examples of simulated data that were used to calibrate the TGP. One example passes the TGP and one fails. The parameters of the simulation are equivalent to those of SLG-β devices with a larger spin-orbit coupling $\alpha \simeq 13$ meV nm.

The first realization, called SLG-β-R1, represents the 3 μm long device with $n_{2D,\text{int}} = 2.4 \times 10^{12}/\text{cm}^2$. Here we assume $T = 30$ mK. Stage 1 data are shown in Fig. 30. There are stable ZBP clusters in G_{RR} and G_{LL} as well as accidental ZBPs present for some cutter settings which correspond to disorder-induced subgap states at the junction. Due to the larger level of disorder in SLG-β-R1 than in DLG-ε-R1, there are more such accidental sub-gap states than in Fig. 28. The joint ZBP map is shown in Fig. 30(c).

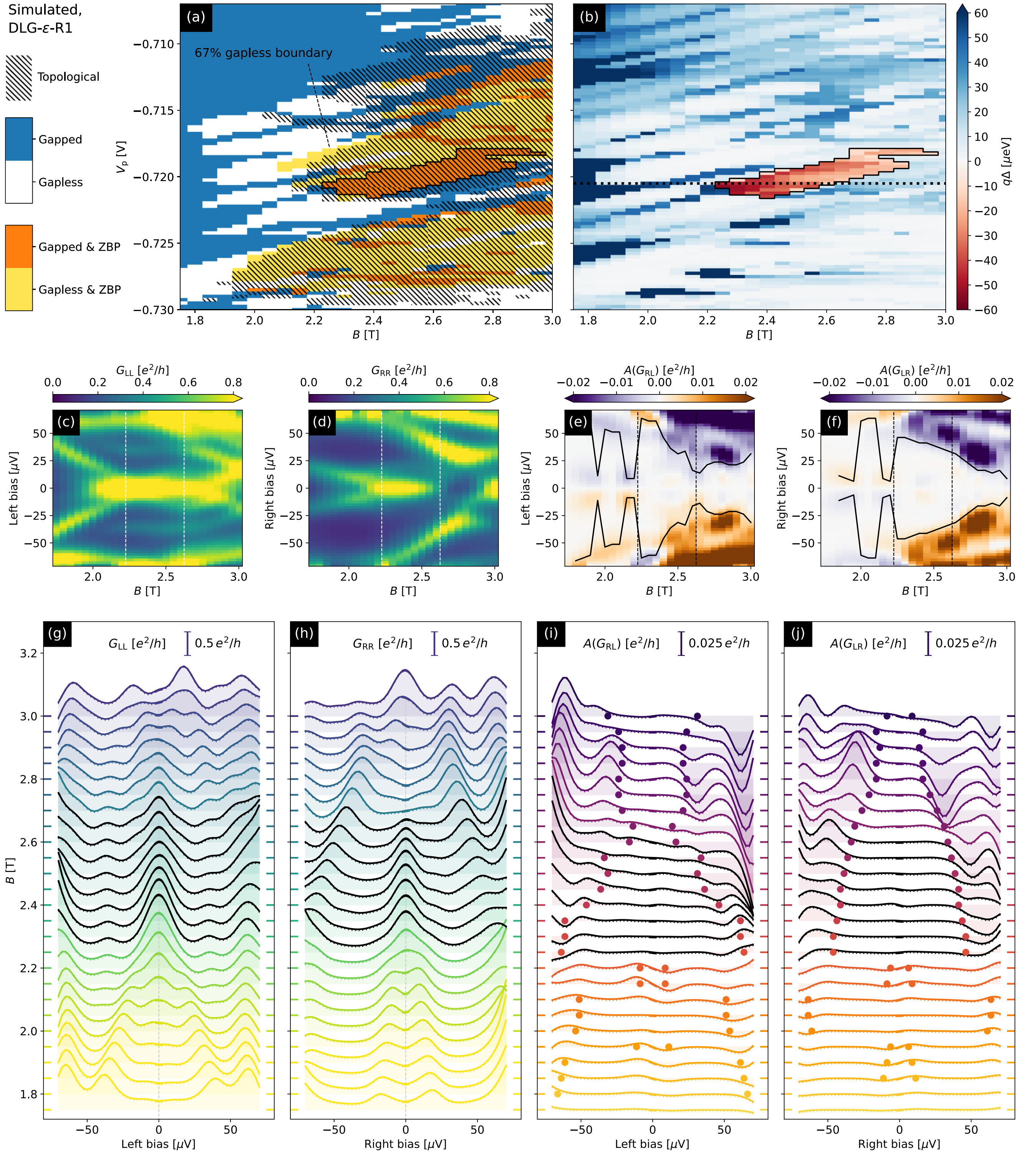

FIG. 29. (a) The simulated phase diagram for DLG, ε stack with $n_{\mathrm{2D,int}} = 10^{12}/\mathrm{cm}^2$ at $T = 40$ mK, combining the clusters of stable ZBPs at both junctions with the map of zero/nonzero gap. We identify gapped/gapless regions, with/without stable ZBPs, according to the color legend on the left. 67% of the boundary of the SOI_2 is gapless. The hatched regions are where the topological invariant is negative. (b) The simulated phase diagram, showing trivial and topological phases, as identified by the TGP. $q = \pm 1$ in the trivial/topological phase, so the color scale shows the size of the trivial (blue) or topological (red) gap. The protocol assigns a maximum topological gap (defined as the top quintile of measured gaps within the SOI_2) of $\Delta_{\mathrm{topo}}^{\mathrm{max}} = 41$ μeV. Simulated local and antisymmetrized nonlocal conductances at $V_p = -0.7205$ V: (c) G_{LL}, (d) G_{RR}, (e) $A(G_{\mathrm{RL}})$, (f) $A(G_{\mathrm{LR}})$. The field range between the vertical lines is in the SOI_2. Panels (g)–(j) are "waterfall" plots representing the same simulated data. The black curves in (e) and (f) and the dots in (i) and (j) are *not* guides to the eye; they indicate where the nonlocal signal drops below a threshold value, as described in the text. The details of these plots are disorder dependent, and any visible resemblance to measured data does *not* play a role in our analysis.

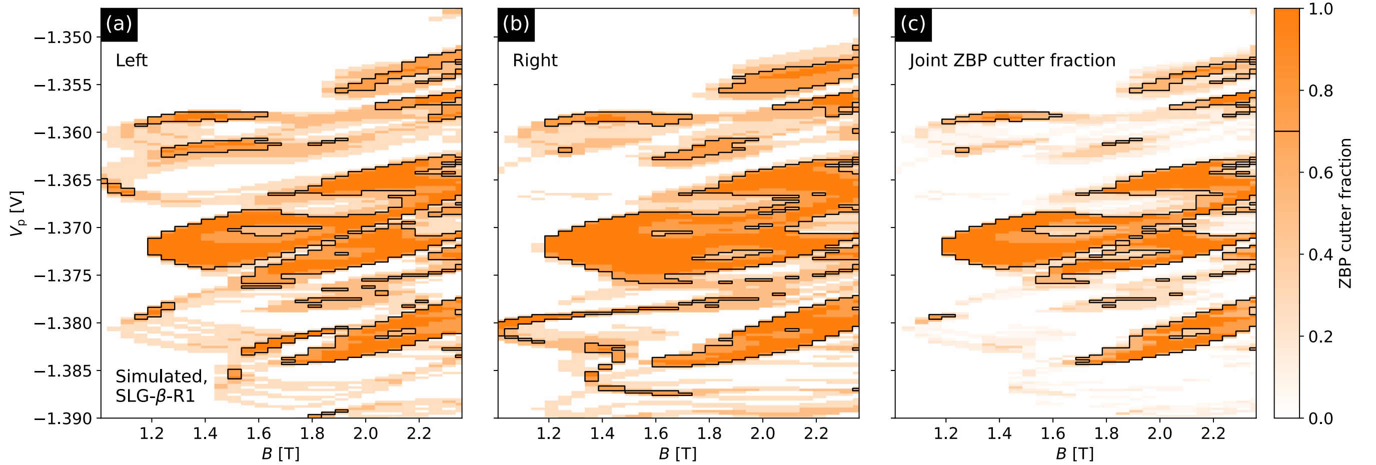

FIG. 30. The TGP applied to simulated transport data for a narrow 3 μm long wire with $n_{2D,int} = 2.4\times10^{12}/\text{cm}^2$, $\alpha \simeq 13$ meV nm at $T = 30$ mK, highlighting regions of phase space with stable ZBPs in (a) G_{LL} and (b) G_{RR}. (c) Regions of phase space with stable ZBPs in both G_{LL} and G_{RR}. Simulated transport data such as this are used to test the TGP. Here, we show one particular disorder realization for illustrative purposes. Any possible visible resemblance to measured data is dependent on the disorder realization and does *not* play a role in our analysis.

The Stage 2 analysis of simulated device SLG-β-R1 is presented in Fig. 31. Simulated device SLG-β-R1 has an SOI_2 around $(B, V_p) \approx (1.5\text{ T}, -1.372\,75\text{ V})$. 71% of the boundary of this SOI_2 is gapless; the maximum and median topological gaps are 30 and 25 μeV, respectively, for this cutter gate setting. Local and nonlocal conductances for $V_p = -1.372\,75$ V are shown in Figs. 31(c)–31(f). There are stable ZBPs at both junctions over a range of B fields of extent ≈1.3–1.7 T, and there is a clear gap closing and reopening as a function of B. Also, note the similarity between the hatched regions with negative SI in Fig. 31(a) and the bright orange regions in the simulated Stage 1 data in Fig. 30.

For the sake of comparison, we also present trivial ZBPs seen at a different value of $V_p = -1.365\,75$ V in Figs. 31(g)–31(j) [see upper dotted line in Fig. 31(b)]. However, the nonlocal conductance data in Figs. 31(i) and 31(j) clearly show that the system is gapless over the corresponding range of B field values.

In Fig. 32, we present Stage 2 of TGP for another disorder realization, which we call SLG-β-R2. This is one of the realizations that passed Stage 1 but failed Stage 2. There are stable ZBPs at both junctions around $V_p = -1.36$ V, as may be seen in Figs. 32(c) and 32(d). However, the nonlocal conductances in Figs. 32(e) and 32(f) yield zero gap. In fact, the, system is gapless over most of the scanned region, so this simulated transport data does not pass Stage 2 of the TGP. This example once again reinforces the fact that local measurements alone cannot reliably detect a topological phase.

APPENDIX F: COMPARISON OF SOI_2 FOR DIFFERENT CUTTER PAIRS

In this Appendix we compare the TGP Stage 2 outcome for different cutter pairs. Figure 11 demonstrates the results for cutter pair #0 (with $G_N \approx 0.3e^2/h$ for both sides) showing 78% gapless boundary and $\Delta_{\text{topo}}^{\text{max}} = 23$ μeV. Results for cutter pairs #1 ($G_N \approx 0.5e^2/h$) and #2 ($G_N \approx 0.7e^2/h$) are demonstrated in Figs. 33 and 34 showing 89% gapless boundary and $\Delta_{\text{topo}}^{\text{max}} = 26$ μeV for cutter pairs #1 and 74% gapless boundary and $\Delta_{\text{topo}}^{\text{max}} = 21$ μeV for cutter pairs #2. This comparison shows that SOI_2s corresponding to the different cutter pairs are similar. The vertical and horizontal dotted lines in panel (b) are the same in Figs. 11, 33, and 34; the intersection of these two lines is always inside the SOI_1 which clearly demonstrates that they overlap.

APPENDIX G: THREE-TERMINAL CONDUCTANCE MEASUREMENTS WITH SEVERAL HUNDRED HZ EXCITATIONS

The conductance matrix is measured with a standard lock-in technique, applying simultaneous voltage excitations with amplitudes $dV_L^0(f_L)$ and $dV_R^0(f_R)$ to the inputs of the left and right terminals, respectively. They are at frequencies f_L and f_R, respectively, and currents $dI_L^0(f_L)$ and $dI_L^0(f_R)$ are measured at the left terminal while $dI_R^0(f_L)$ and $dI_R^0(f_R)$ are measured at the right terminal. However, due to the finite impedance network between the signal input and the measured sample, the voltages applied and the currents measured deviate from those at the sample inputs. At lock-in frequencies of several hundred Hz, the capacitances of the cryostat lines and filters (on the order of several nF) combined with the line and filter resistances have a non-negligible contribution to the measured currents. Furthermore, a finite resistance at the drain contact imposes an effective voltage modulation of the opposing contact as a voltage divider effect. As a result, the sample experiences voltage modulations $dV_L(f_L)$ and $dV_L(f_R)$ at the left and $dV_R(f_L)$ and $dV_R(f_R)$ at the right input. The currents at the the left terminal are $dI_L(f_L)$ and $dI_L(f_R)$ while the currents at the right terminal are $dI_R(f_L)$ and $dI_R(f_R)$. Noting that $dI_I(f) = G_{IJ}dV_J(f)$ where $I, J = L, R$, the conductances

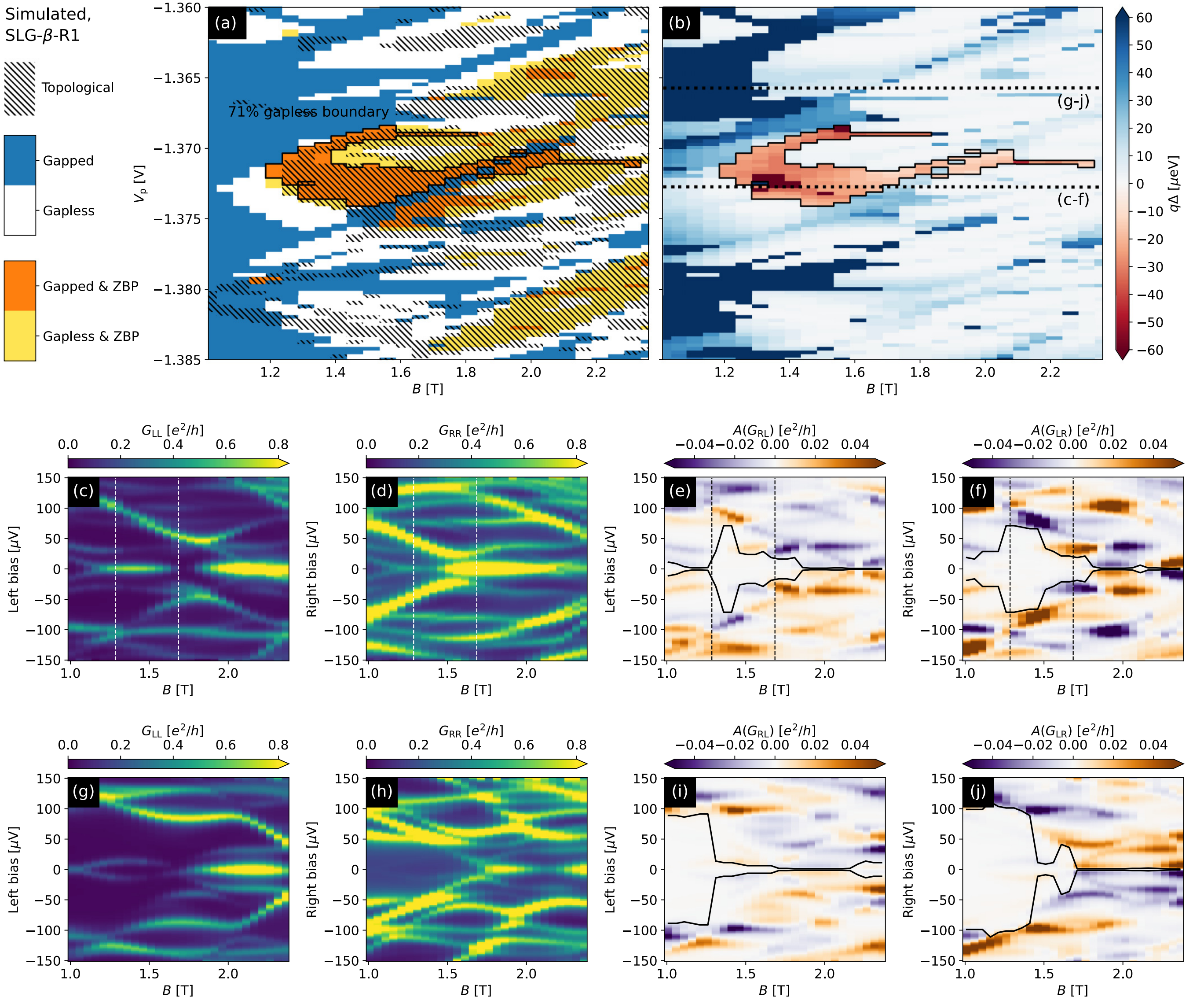

FIG. 31. (a) The simulated phase diagram for SLG device (disorder realization R1) with $n_{2D,\mathrm{int}} = 2.4\times10^{12}/\mathrm{cm}^2$, $\alpha \simeq 13$ meV nm at $T = 30$ mK, combining the clusters of stable ZBPs at both junctions with the map of zero/nonzero gap. We identify gapped/gapless regions, with/without stable ZBPs, according to the color legend on the left. 71% of the boundary of the SOI_2 is gapless. The hatched regions are where the topological invariant is negative. (b) The simulated phase diagram, showing trivial and topological phases, as identified by the TGP. $q = \pm1$ in the trivial/topological phase, so the color scale shows the size of the trivial (blue) or topological (red) gap. The protocol assigns a maximum topological gap (defined as the top quintile of measured gaps within the SOI_2) of $\Delta_{\mathrm{topo}}^{\mathrm{max}} = 30$ μeV. The lower and upper horizontal dotted lines correspond to the cuts shown, respectively, in (c)–(f) and (g)–(j). (c)–(f) Simulated local and antisymmetrized nonlocal conductances at $V_\mathrm{p} = -1.372\,75$ V: (c) G_{LL}, (d) G_{RR}, (e) $A(G_{\mathrm{RL}})$, (f) $A(G_{\mathrm{LR}})$. The field range between the vertical lines is in the SOI_2. (g)–(j) Conductances from the nontopological region ($V_\mathrm{p} = -1.365\,75$ V, outside of SOI_2). As may be seen by comparing (c) and (d) and (g) and (h), the local conductances are similar, but the nonlocal conductances in (i) and (j) lack a clear transport gap reopening, distinguishing them from (e) and (f).

are obtained from

$$\begin{pmatrix} G_{LL} & G_{LR} \\ G_{RL} & G_{RR} \end{pmatrix} = \begin{pmatrix} dI_\mathrm{L}(f_\mathrm{L}) & dI_\mathrm{L}(f_\mathrm{R}) \\ dI_\mathrm{R}(f_\mathrm{L}) & dI_\mathrm{R}(f_\mathrm{R}) \end{pmatrix} \begin{pmatrix} dV_\mathrm{L}(f_\mathrm{L}) & dV_\mathrm{L}(f_\mathrm{R}) \\ dV_\mathrm{R}(f_\mathrm{L}) & dV_\mathrm{R}(f_\mathrm{R}) \end{pmatrix}^{-1}. \tag{G1}$$

Note that we recover Eq. (2) if we take $dV_\mathrm{L}(f_\mathrm{R}){=}dV_\mathrm{R}(f_\mathrm{L}){=}0$. To proceed, we need a map

$$\mathbf{M} \equiv \begin{pmatrix} \mathbf{M}_{VV} & \mathbf{M}_{VI} \\ \mathbf{M}_{IV} & \mathbf{M}_{II} \end{pmatrix} \tag{G2}$$

between the voltages and currents at the sample, $\mathbf{V} = (dV_\mathrm{L}(f), dV_\mathrm{R}(f))^T$ and $\mathbf{I} = (dI_\mathrm{L}(f), dI_\mathrm{R}(f))^T$, and the voltages applied and the currents measured, $\mathbf{V}_0 = (dV^0_{L,0}(f),$

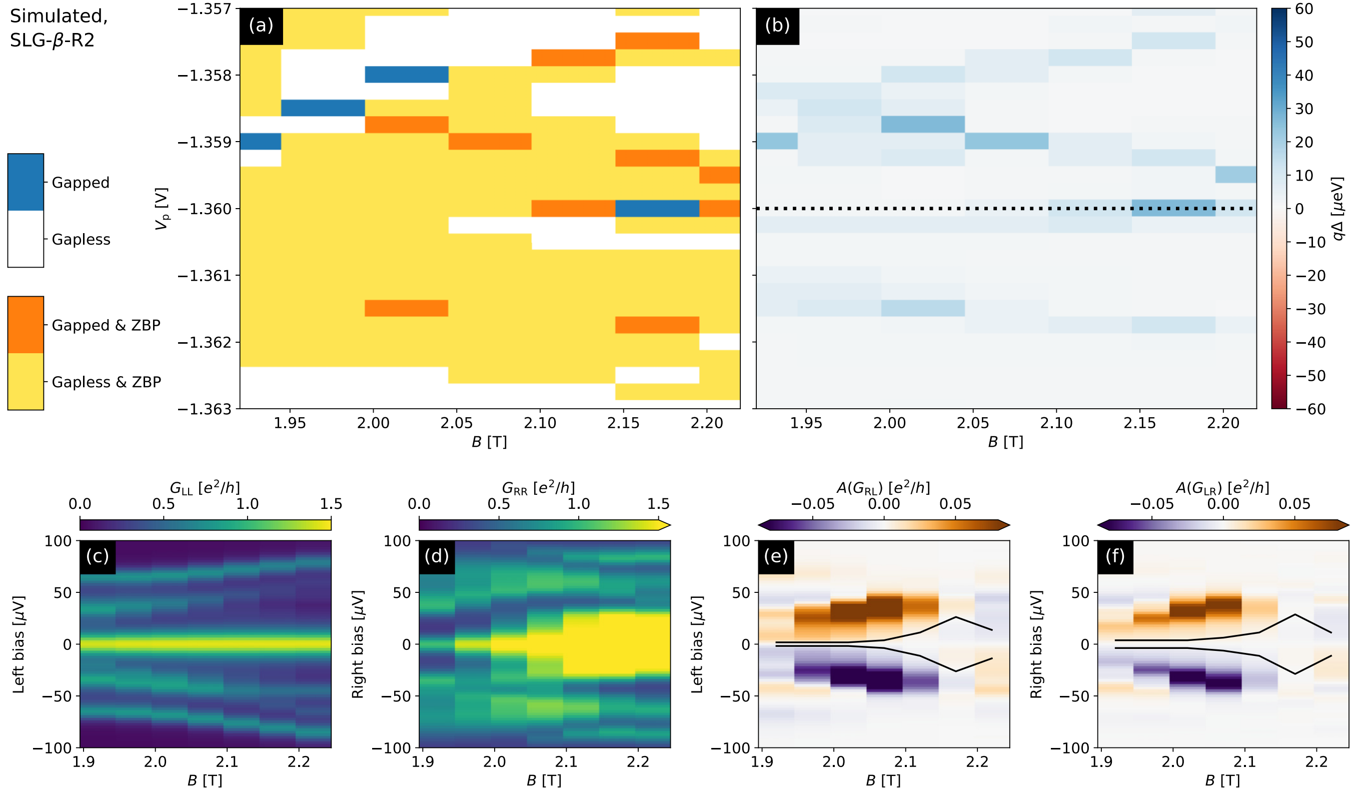

FIG. 32. Stage 2 analysis for realization SLG-β-R2 at $T = 30$ mK. (a) The regions with stable ZBPs at both junctions. (b) The gap as function of B and V_p. It vanishes in the region of interest, so this device fails the TGP. (c)–(f) Local and antisymmetrized nonlocal conductances at $V_p = -1.36$ V. The local conductances in (c) and (d) show ZBPs, but there is no gap reopening visible in the antisymmetrized nonlocal conductances in (e) and (f).

$dV^0_{R,0}(f)^T$ and $\mathbf{I}_0 = (dI^0_{L,0}(f), dI^0_{R,0}(f))^T$:

$$\begin{pmatrix} \mathbf{V} \\ \mathbf{I} \end{pmatrix} = \begin{pmatrix} \mathbf{M}_{VV} & \mathbf{M}_{VI} \\ \mathbf{M}_{IV} & \mathbf{M}_{II} \end{pmatrix} \begin{pmatrix} \mathbf{V}_0 \\ \mathbf{I}_0 \end{pmatrix}. \tag{G3}$$

The impedance network between the input ports and the measured sample consists of a sequence of stages, each of which has the general form illustrated in Fig. 35(a): every line has a capacitance to ground and to every other line in parallel and a resistance in series to the next stage. The drain of the measured device is also connected to ground at the input and is thus included in the circuit here and will be reduced from the final mapping later. By denoting the terminals as $k = \{L, R, D\}$ and $l = \{L, R, D, G\}$ (where G denotes ground), the output voltages dV_k and currents dI_k are determined by the input voltages dV'_k and currents dI'_k, as well as cross-currents dI_{kl} as

$$dI_k = dI'_k - \sum_{l\neq k} dI_{kl} = dI'_k - \sum_{l\neq k} Y_{kl}(dV'_k - dV'_l) = -\left(\sum_{l\neq k} Y_{kl}\right) dV'_k + \sum_{l\neq k} Y_{kl} dV'_l + dI'_k, \tag{G4}$$

$$dV_k = dV'_k - Z_k dI_k = \left[1 + Z_k \left(\sum_{l\neq k} Y_{kl}\right)\right] dV'_k - Z_k \sum_{l\neq k} Y_{kl} dV'_l - Z_k dI'_k, \tag{G5}$$

where Z_k are the impedances (resistances for sufficiently low frequencies) of the lines, $Y_{kl} = 2\pi i f C_{kl}$ are the parallel admittances via capacitors C_{kl} between k and l, and $V_G = 0$. Equations (G4) and (G5) can be expressed in matrix form as

$$\begin{pmatrix} V_L \\ V_R \\ V_D \\ I_L \\ I_R \\ I_D \end{pmatrix} = \begin{pmatrix} 1 + Z_L \sum_{k=R,D,G} Y_{Lk} & -Z_L Y_{LR} & -Z_L Y_{LD} & -Z_L & 0 & 0 \\ -Z_R Y_{LR} & 1 + Z_R \sum_{k=L,D,G} Y_{Rk} & -Z_R Y_{RD} & 0 & -Z_R & 0 \\ -Z_D Y_{LD} & -Z_D Y_{RD} & 1 + Z_D \sum_{k=L,R,G} Y_{Dk} & 0 & 0 & -Z_D \\ -\sum_{k=R,D,G} Y_{Lk} & Y_{LR} & Y_{LD} & 1 & 0 & 0 \\ Y_{LR} & -\sum_{k=L,D,G} Y_{Rk} & Y_{RD} & 0 & 1 & 0 \\ Y_{LD} & Y_{RD} & -\sum_{k=L,R,G} Y_{Dk} & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} V'_L \\ V'_R \\ V'_D \\ I'_L \\ I'_R \\ I'_D \end{pmatrix}. \tag{G6}$$

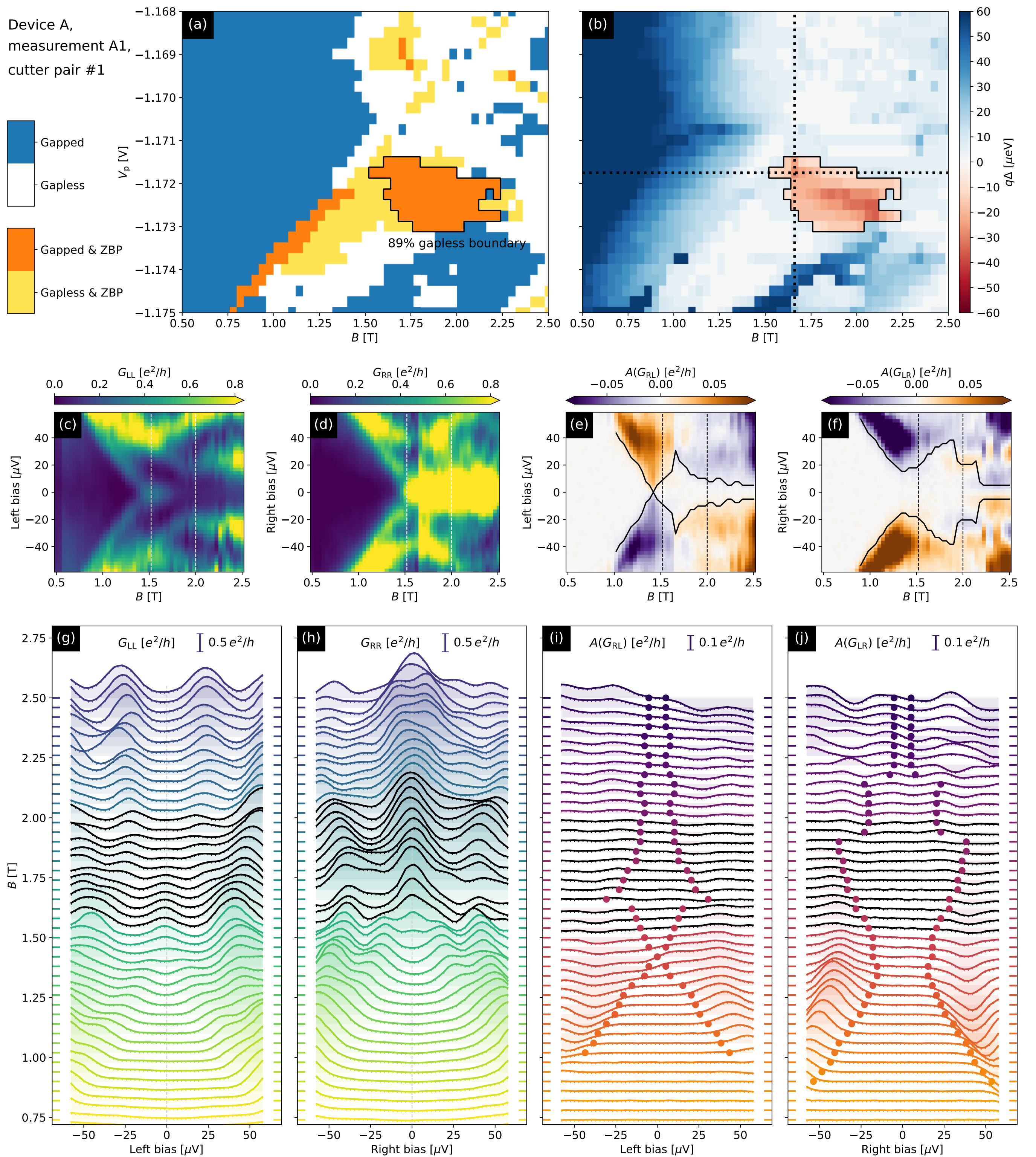

FIG. 33. TGP Stage 2 analysis of the device A (measurement A1). Figure shows the same as in Fig. 11 but for cutter pair #1 corresponding to $G_N \approx 0.5e^2/h$ for both sides. (a) The boundary of the SOI_2 is interpreted as a phase transition line, consistent with a visible gap closure along 89% of it. (b) The protocol assigns a maximum topological gap $\Delta_{topo}^{max} = 26$ μeV.

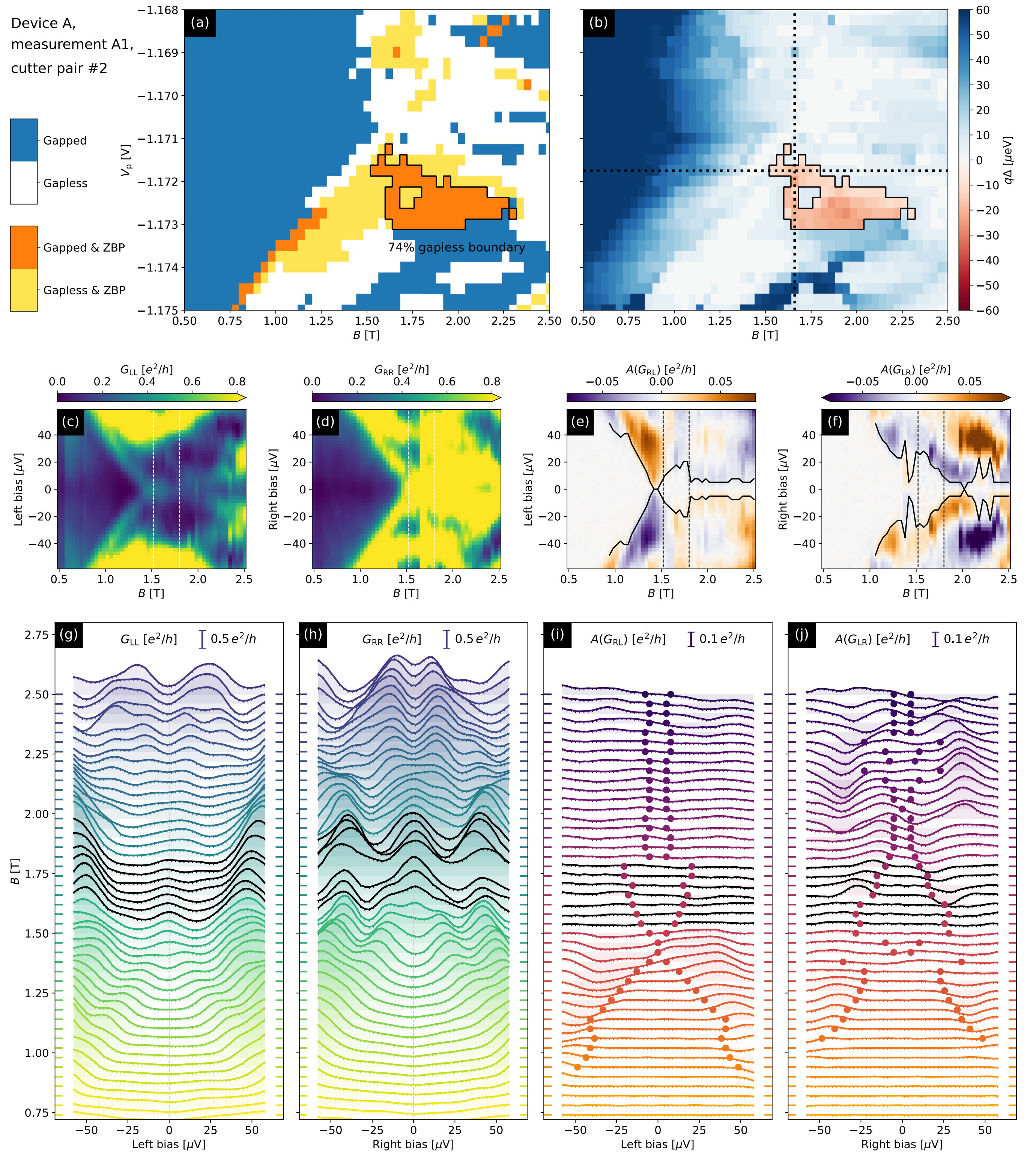

FIG. 34. TGP Stage 2 analysis of the device A (measurement A1). Figure shows the same as in Fig. 11 but for cutter pair #2 corresponding to $G_N \approx 0.7e^2/h$ for both sides. (a) The boundary of the SOI_2 is interpreted as a phase transition line, consistent with a visible gap closure along 74% of it. (b) The protocol assigns a maximum topological gap $\Delta_{topo}^{max} = 21$ µeV.

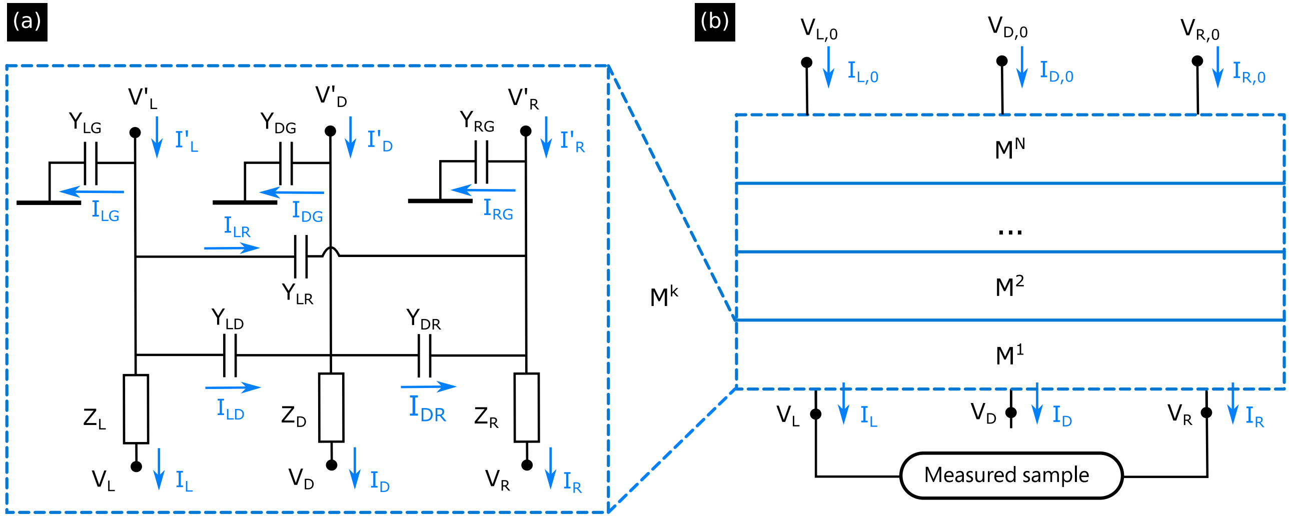

FIG. 35. (a) The stage of the impedance network that leads from the input ports to the measured sample. (b) The full network consists of multiple stages in series.

This has the general form

$$\begin{pmatrix}\mathbf{V}\\ \mathbf{I}\end{pmatrix} = \begin{pmatrix}\mathbf{M}^1_{VV} & \mathbf{M}^1_{VI}\\ \mathbf{M}^1_{IV} & \mathbf{M}^1_{II}\end{pmatrix}\begin{pmatrix}\mathbf{V}'\\ \mathbf{I}'\end{pmatrix} \equiv \mathbf{M}^1\begin{pmatrix}\mathbf{V}'\\ \mathbf{I}'\end{pmatrix}. \tag{G7}$$

With multiple stages in a sequence, the mapping from the input to the measured device

$$\begin{pmatrix}\mathbf{V}\\ \mathbf{I}\end{pmatrix} = \mathbf{M}^{\text{tot}}\begin{pmatrix}\mathbf{V}^0\\ \mathbf{I}^0\end{pmatrix} \tag{G8}$$

is given by matrix multiplication $\mathbf{M}^{\text{tot}} = \prod_k \mathbf{M}^k$ where the matrices $\mathbf{M}^k$ are given by Eq. (G6). The 6×6 map $\mathbf{M}^{\text{tot}}$ is further reduced to a more useful 4×4 form by the following steps:

(1) Imposing current conservation ($dI_D = -dI_L - dI_R$) at the sample, which then reduces the map to a 5×5 matrix with $k \in \{dV_L, dV_R, dV_D, dI_L, dI_R\}$ and $l \in \{dV_L^0, dV_R^0, dV_D^0, dI_L^0, dI_R^0\}$ which now takes the form

$$M^{\text{red}}_{kl} = M^{\text{tot}}_{kl} - \left(M^{\text{tot}}_{dI_L dI_D^0} + M^{\text{tot}}_{dI_R dI_D^0} + M^{\text{tot}}_{dI_D dI_D^0}\right)^{-1} \times \left(M^{\text{tot}}_{dI_L l} + M^{\text{tot}}_{dI_R l} + M^{\text{tot}}_{dI_D l}\right) M^{\text{tot}}_{k dI_D^0}. \tag{G9}$$

(2) Defining dV_L and dV_R as potentials with respect to dV_D at the sample, as well as $dV_D^0 = 0$, which leads to the final 4×4 matrix $\mathbf{M}$ with $k \in \{dV_L, dV_R, dI_L, dI_R\}$ and $l \in \{dV_L^0, dV_R^0, dI_L^0, dI_R^0\}$ that takes the form

$$M_{V_{L(R)}l} = M^{\text{red}}_{V_{L(R)}l} - M^{\text{red}}_{V_D l},$$
$$M_{I_{L(R)}l} = M^{\text{red}}_{I_{L(R)}l}. \tag{G10}$$

The effect on input voltages and measured currents of additional filtration from the measurement instruments should also be incorporated.

For our setup, the mapping $\mathbf{M}$ is comprised of four stages $\mathbf{M}^k$ where the resistances are determined by the installed filters and, for the final stage, are the sample lead resistances which are extracted independently from the linear I-V response in DC measurements. To calibrate the capacitances in the setup, we measure dI_L^0 and dI_R^0 as a function of the excitation frequency f_L of a voltage modulation first applied to the left port, then as a function of frequency f_R of the modulation applied to the right port when the device is fully pinched off (i.e., the zero conductance limit). We then use capacitances between the lines and the ground as fit parameters relating the measured dI_L^0 to f_L and dI_R^0 to f_R. Finally, the mutual capacitance between L and R is obtained as a fit parameter relating the measured dI_L^0 and dI_R^0 to f_R and f_L, respectively. In the experiments described in the main text, the extracted capacitances of the fridge lines and filters, together with known cutoff frequencies of the voltage sources and current preamplifier outputs, are then used to calculate the sample conductances based on the measured dI_L^0 and dI_R^0. Full details on this calibration routine, including all extracted parameters that were used to process measured data, can be found in the accompanying data repository [98].

Note that a further effect of finite resistances on the stages of the measurement circuit is to rescale the applied DC bias voltages. As described in [156], the DC voltages at the sample $\mathbf{V} = (V_L, V_R)^T$ are related to the applied DC voltages $\mathbf{V^0} = (V_L^0, V_R^0)^T$ and DC currents $\mathbf{I^0} = (I_L^0, I_R^0)^T$ through the relationship

$$\mathbf{V} = \mathbf{V^0} - R\,\mathbf{I^0}, \tag{G11}$$

where R is a matrix containing the total resistances on the left, right, and drain lines:

$$R = \begin{pmatrix}R_L + R_D & R_D\\ R_D & R_R + R_D\end{pmatrix}. \tag{G12}$$

For all the experimental data sets presented in this manuscript, the average magnitude of these corrections is 1%–6% of the applied bias voltages. For this reason, we do not apply these corrections and present the data as a function of the applied bias voltages, and not of the bias voltages at the sample.

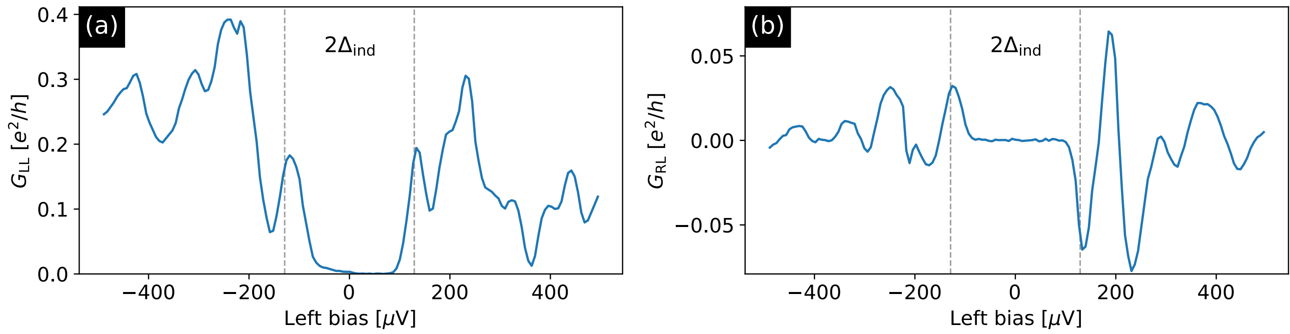

FIG. 36. Example cut of local (a) and nonlocal (b) conductance vs bias voltage for device A at $B = 0$. The zero-field bulk induced gap as extracted from this data set is $\Delta_{\rm ind} \sim 125$ μeV, as estimated from the locations of the lowest-lying peak in the nonlocal data. This number is consistent with $\Delta_{\rm ind} = 129 \pm 12$ μeV quoted in the main text (shown by vertical dashed lines), obtained by aggregating over several such bias traces from device A.

For the purposes of induced gap estimation as in Appendix H, full characterization of the measurement circuit is not required since the relevant features are the presence of conductance peaks and the DC voltage biases at the sample. In this case, we apply a simpler correction procedure for finite frequency effects consisting of rotation of the acquired signal in the complex plane (typically a few degrees), projection along the axis that maximizes signal to noise ratio, and subtraction of a small residual conductance offset (typically on the order of $10^{-3}e^2/h$).

APPENDIX H: SUBGAP DENSITY OF STATES AT ZERO FIELD

We now discuss the subgap density of states measured in device A at zero magnetic field. The presence of a finite subgap conductance can be attributed to coupling to the lead, temperature broadening, and/or the interfacial disorder, as discussed in Ref. [105]. Indeed, the first generation of proximitized nanowires [38] revealed a "soft" induced gap which was primarily associated with disorder at the superconductor-semiconductor interface. The local and nonlocal conductances as a function of bias voltage for device A are shown in Fig. 36. Note that in order to have large enough signal in the nonlocal conductance, one needs to keep the junctions sufficiently open. Data sets for both devices show well-defined coherence peaks at the edge of the induced gap and a strong suppression of the local conductance below the gap. The subgap nonlocal conductances are below the noise floor of the measurement and, thus, consistent with zero. The magnitude of the induced gap as determined from the coherence peak location in the local conductance agrees with the location of the lowest peak in the nonlocal conductance, indicating that, for these bias cuts, no subgap states were observed in the junction. In general, subgap states may appear in the local spectroscopy, which we interpret as localized bound states at the junction, likely originating from the defects residing close to junction.

In order to understand the residual subgap density of states observed in local spectroscopy, we can compare the measured subgap suppression to the theory model described in [159]. The subgap suppression is consistently below the single-channel limit, indicating that we have a "hard" proximitized gap with multiple conduction channels at the junction. Indeed, the above-gap conductance at the cutter and plunger values was approximately $0.18\,e^2/h$ whereas the zero-bias conductance was comparable to the noise floor, which is estimated to be $0.001\ e^2/h$. This is consistent with having two or more conduction channels in the lead.

Finally, we note that a better way to quantify the level of disorder in our devices is by measuring the localization length under the superconductor at finite B field, outlined in Appendix C. This measurement is more sensitive to disorder and is easier to interpret than the zero-field local conductance measurement. Nevertheless, the residual subgap conductance data are consistent with having ultraclean proximitized nanowires as discussed above.

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