Electrostatic modulation of the lateral carrier density profile in field effect devices with nonlinear dielectrics

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The properties of two-dimensional (2D) electronic systems are often effectively controlled using electrostatic gating. The geometry of such field effect devices influences the effectiveness of the gate and the carrier density profile in the 2D device. Here, we analyze the gate-induced spatial variations in the lateral carrier density in patterned $LaAlO_3/SrTiO_3$ devices. We model the electrostatics of the 2D interface using the Thomas-Fermi approximation and compute the gate-induced charge distribution at the interface. We show that the electric field lines generated by the gate are focused at the edges of the device, causing an increased depletion near its edges. This effect is accentuated in $LaAlO_3/SrTiO_3$ due to the large, nonlinear dielectric constant of the substrate, and the large distance between the gate electrode and the interface. We experimentally demonstrate one consequence of this effect by directly imaging current distributions in gated heterostructures, finding that insulating regions nucleate at the edges of the device due to the gate. Our results suggest that device geometry and choice of dielectric materials control the charge distribution in 2D systems.

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I. INTRODUCTION

Complex oxide interfaces often host electronic properties that are not present at the host compounds [1–4]. $LaAlO_3/SrTiO_3$ (LAO/STO) heterostructures are a well-studied example, where a conducting two-dimensional electron system (2DES) forms at the interface between LAO and STO [5]. The 2DES exhibits several exciting properties, including superconductivity [6] and Rashba spin-orbit coupling [7,8], which open the door to various applications [9]. These properties can be tuned by changing the carrier density of the 2DES. For example, a Lifshitz transition from single- to multiband transport [10], the Rashba spin-orbit coupling [7,8], a superconductor-to-insulator transition [11], and a metal-to-insulator transition [12,13] are all achieved through changing the carrier density.

The key tuning knob which enables effective and controllable changes to the carrier density is electrostatic gating. Field effect devices in oxide interfaces can be realized in several geometries. Top gates and side gates offer spatial control over the carrier density and typically require low voltages (a few volts), due to the small distance between the 2DES and the gate electrode [14–17]. Another possibility is using a back gate, where the substrate is used as the gate dielectric. While a thick substrate usually precludes effective control over the carrier density due to the small capacitance generated by this geometry, this problem is alleviated in STO-based systems, due to the large dielectric constant of STO at low temperatures [18]. Although this geometry requires larger voltages than the top and side gates, it is easy to fabricate and is more robust against electrostatic discharge. It has therefore been the most widely used route to gate STO-based 2D systems.

In addition to tuning the overall carrier density, the gate also changes the three-dimensional (3D) distribution of the carriers in the 2DES. The vertical charge distribution in STO-based systems has been studied experimentally and theoretically [14,19–23] because it affects the mobility and superconductivity in the 2DES. The lateral charge distribution across the device is also affected by electrostatic gating. The effect of gating on the lateral carrier density depends on the device geometry, and was shown to modify the resistance and capacitance of small devices [24]. However, a detailed study of the underlying carrier density profile that causes this effect is missing.

Here, we show that the charge density near the edges of the device is suppressed due to electrostatic gating. We demonstrate that the large dielectric constant of STO causes a significant enhancement of the electric fields generated by the gate at the edges of the 2D patterned device. We calculated the electric fields and carrier density distribution self-consistently using the Thomas-Fermi approximation, and showed that the enhanced fields reduce the carrier densities near the device edges. We experimentally observed this effect by imaging the current flow in patterned LAO/STO interfaces using scanning superconducting quantum interference device (SQUID) microscopy. Our results suggest that the gate-tunable properties of STO-based interfaces are spatially inhomogeneous due to the finite sample geometry.

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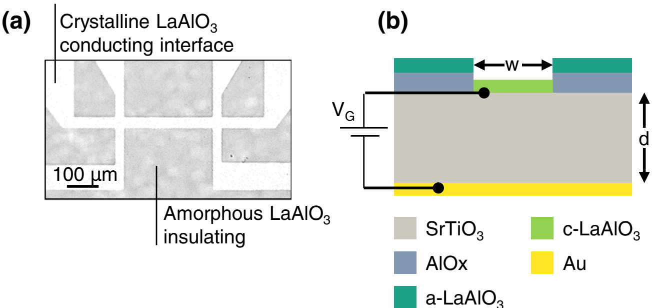

FIG. 1. (a) Optical microscope image of an LAO/STO device. White areas correspond to a crystalline LAO epitaxial film, beneath which a conducting interface forms, while the dark gray areas correspond to an amorphous layer, and insulating regions. (b) A schematic cross section (not to scale) of a patterned device. The conducting interface, of width w, is typically narrower than the thickness of the substrate, d. The gate voltage is applied between the interface and a metallic electrode at the bottom of the substrate.

II. THOMAS-FERMI MODEL

Figure 1 shows a typical LAO/STO device geometry. The details of the device fabrication can be found in Ref. [25]. In this case, a conducting Hall bar of width w was patterned lithographically on a 5 mm × 5 mm × 0.5 mm STO substrate. The back gate is a gold film deposited on the other side of the substrate, or a metallic surface onto which the sample is glued. For simplicity, we consider only a cross section of this device, assuming the Hall bar is long enough to ignore the geometry of the contacts.

To determine the electric potential $\phi(\mathbf{r})$, we used the Laplace equation

$$\nabla[\epsilon(\mathbf{r})\nabla\phi(\mathbf{r})] = 0, \tag{1}$$

where $\epsilon(\mathbf{r})$ is the dielectric constant. We treat the gate electrode as a perfect ground plane, and impose a voltage difference V_G between this electrode and the interface. The 2DES does not perfectly screen the electric field, resulting in changes to the charge density which can be described with the Thomas-Fermi approximation,

$$\delta n(\mathbf{r}) = e\nu[\mu - e\phi(\mathbf{r})], \tag{2}$$

where ν is the density of states, e is the electron charge, and $\mu = V_G/e$ is the chemical potential. For simplicity, we describe the 2DES with a single parabolic band of effective mass $m_{\text{eff}} = 3m_e$ [26], such that $\nu = m_{\text{eff}}/\pi\hbar^2$. By considering a single parabolic band, we effectively treat the system in a low carrier density regime, where the light d_{xz}, d_{yz} orbital bands are empty, and the effects of spin-orbit coupling, which are important primarily near the band-touching points [10], can be ignored. To accurately capture the electrostatics at higher carrier concentrations, one can introduce an energy-dependent density of states which captures the multiband and spin-orbit coupling effects present in the realistic 2DES. The electric potential due to this charge distribution satisfies Gauss's law, imposing the boundary condition

$$\epsilon\nabla\phi(\mathbf{r}) \cdot \hat{\mathbf{n}} = \delta n(\mathbf{r}), \tag{3}$$

where $\hat{\mathbf{n}}$ is a unit vector normal to the interface.

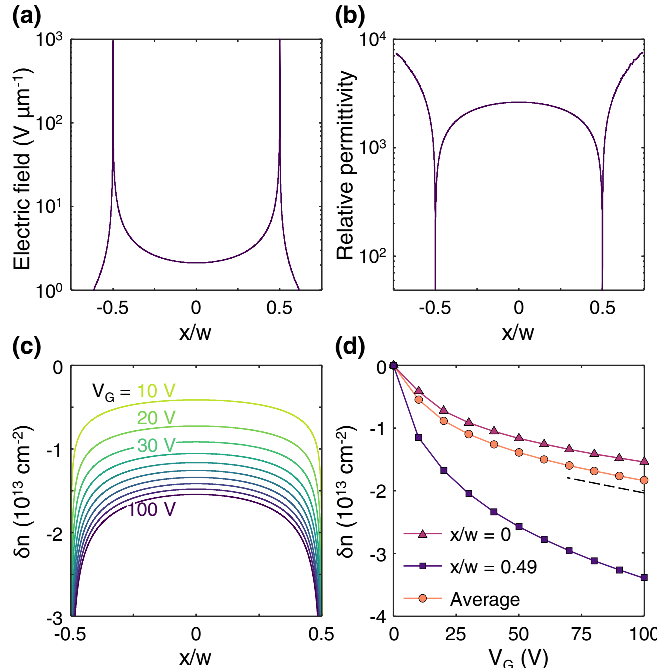

FIG. 2. (a), (b) Profiles of the electric field magnitude (a), and dielectric constant (b), computed along a 100-µm-wide device at $V_G = 100$ V. (c) Charge density profiles for a this device, for V_G between 0 and 100 V. (d) Changes in charge density as a function of V_G, at the center of the device (triangles), and near its edge (squares). The circles show the device-averaged change. The black dashed line is a guide to the eye, demonstrating how the carrier density changes linearly with V_G, once the substrate is polarized.

We used the multiphysics object oriented simulation environment (MOOSE) [27] to solve Eqs. (1)–(3) self-consistently. In our calculations, we take into account the large nonlinear dielectric constant of STO. At low temperatures, STO is highly polarizable [28,29], resulting in a field dependent relative permittivity [30],

$$\epsilon_{\text{STO}}(\mathbf{E}) = 1 + \frac{A}{[1 + (|\mathbf{E}|/E_0)^2]^{1/3}}, \tag{4}$$

where, at 4 K, $A = 23\,000$ and $E_0 = 82\,000$ V m^{-1} [15,31]. This field dependence leads to a substantial reduction of ϵ once the gate is used; for a 500-µm-thick substrate, a gate voltage of 100 V generates an average field of 2×10^5 V m^{-1}, reducing the dielectric constant by 1/2. As we show below, the dielectric constant is further suppressed near the 2DES.

We first consider a 100-µm-wide device. Figures 2(a) and 2(b) show the electric field and relative permittivity profiles at the interface, resulting from a gate voltage of $V_G =$ 100 V. The electric field distribution shows two pronounced peaks, at the two edges of the conducting interface. The peaks originate from focusing of electric field lines originating from the wider (5-mm) gate electrode, at the edges of the interface. To screen the enhanced field, the charge is redistributed such that a larger charge concentration is removed from the areas close to the edges, as shown in Fig. 2(c) for various gate voltages. The charge density at the center of this device,

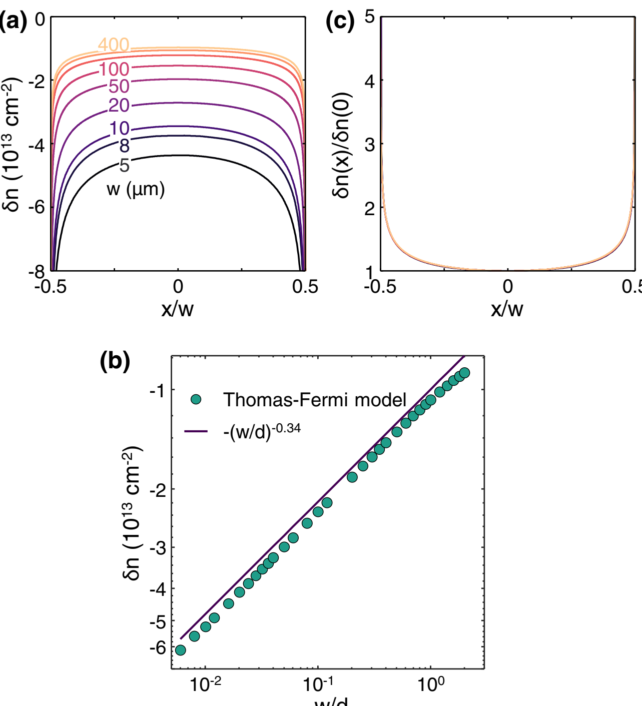

FIG. 3. (a) Charge density profiles along devices with various widths, ranging from 5 to 500 μm, at a constant gate voltage, $V_G = 100$ V. The substrate thickness was 500 μm. (b) Charge density at the center of the device, as a function of the device width, plotted on a log-log scale. The dashed line is $-(w/d)^{-0.34}$. (c) The profiles from (a), rescaled by the charge density at the center of each device. The data collapse onto a single curve.

$\delta n(x = 0)$, can be a factor of 4 larger than the density at its edge, $\delta n(x = w/2)$.

Experiments typically measure the average change in carrier density $\bar{\delta n}$ either using the Hall effect or by measuring the differential capacitance of the sample. To understand how the variations at the edge affect the averaged density, we calculated $\bar{\delta n}$ for various gate voltages [Fig. 2(d)]. Because the density sharply increases away from the edge, $\bar{\delta n}$ is close to the value at the center of the device. It is important to note, however, that the averaged density is lower by about 20% than the carrier density at the center.

Submicron LAO/STO devices may be patterned using electron beam lithography [15,32], and patterning with a conductive atomic force microscopy tip enables widths as low as 2 nm [33]. For narrow devices, the field focusing will be more significant and will result in further suppression of the carrier density. To study how the device geometry affects the gate dependence, we considered Hall bars with widths varying between 5 and 500 μm (w/d between 0.01 and 1). Figure 3(a) shows the resulting carrier density profiles for the various device widths, for $V_G = 100$ V. The overall carrier density change due to the gate is larger for smaller devices. This is a clear deviation from the charging of an ideal capacitor, where the charge density on the capacitor plates does not depend on the size of the plate. Figure 3(b) shows how the density at the center of the device $\delta n(x = 0)$ depends on the geometry. We find a power law dependence,

$$\delta n(x = 0) \sim w^{-\alpha}, \tag{5}$$

with $\alpha \approx 0.34$. This nonlinear behavior is a result of the strong suppression of the dielectric constant close to the interface.

Even though the overall carrier density depends on the device width, we find that the distribution of charges inside the device is insensitive to the geometry. When the density is rescaled by the concentration at the center of the device, $\delta n(x = 0, V_G)$, the profiles from different devices collapse onto a single curve [Fig. 3(c)]. Thus, even for devices as large as the plate separation, the averaged density is 20% smaller than the density at the center.

III. DIRECT IMAGING OF CURRENT FLOW PROFILES

Experimentally, the spatial variations to the carrier density profile can be studied through the current distribution in gated LAO/STO devices. The changes at the edges are comparable to the density of the ungated device. Thus, the electric field focusing could render the edges of the device insulating, confining the current density to the center of the device. We directly observed this effect by imaging the current distribution in a gated LAO/STO device using scanning SQUID microscopy. We applied an alternating current of 3–30 μA rms (frequency 1.6 kHz) to a 60-μm-wide device, and imaged the resulting magnetic field with the SQUID, using a lock-in amplifier. The measurements were performed at 4 K. Figure 4(a) shows the magnetic flux recorded by the SQUID for various gate voltages. As we increased V_G, carriers were removed from the system. Indeed, we find that the current, which was initially distributed along the entire cross section of the device, was gradually focused into the center of the device as we removed carriers from the system.

We tracked the width of the current flow by measuring the distance between the peaks of the magnetic field distribution, as shown in Figs. 4(b) and 4(c). Note that the effective width of the device at $V_G = 0$ V (53 μm) was smaller than the lithographically defined width because the initial application of gate voltage (forming process) led to trapping of some of the carriers at charged impurities [34,35]. We note that conductivity (and carrier density) maps cannot be extracted from measurements of the current density alone, if the current flow is inhomogeneous. Following Ohm's law, $\mathbf{J} = \sigma \mathbf{E}$, an additional measurement of the electric potential is needed in order to determine the conductivity map [36]. However, the changes to the device width require a large conductivity reduction at the edges of the device. Such a reduction is consistent with carrier depletion, and is difficult to explain by other mechanisms, such as changes to the mean free time or effective mass near the edges.

We used the charge density profiles calculated above to compare our model to the effective device width measured in the experiment. Assuming that the initial carrier density is 3×10^{13} cm^{-2}, and that the threshold density for conductivity is 1.2×10^{13} cm^{-2} [12], we defined the conducting and insulating regions of the device according to the carrier density profiles calculated from the simulations. The results, shown in Fig. 4(c), are in qualitative agreement with the data. The variations between the simulation and the experimental data,

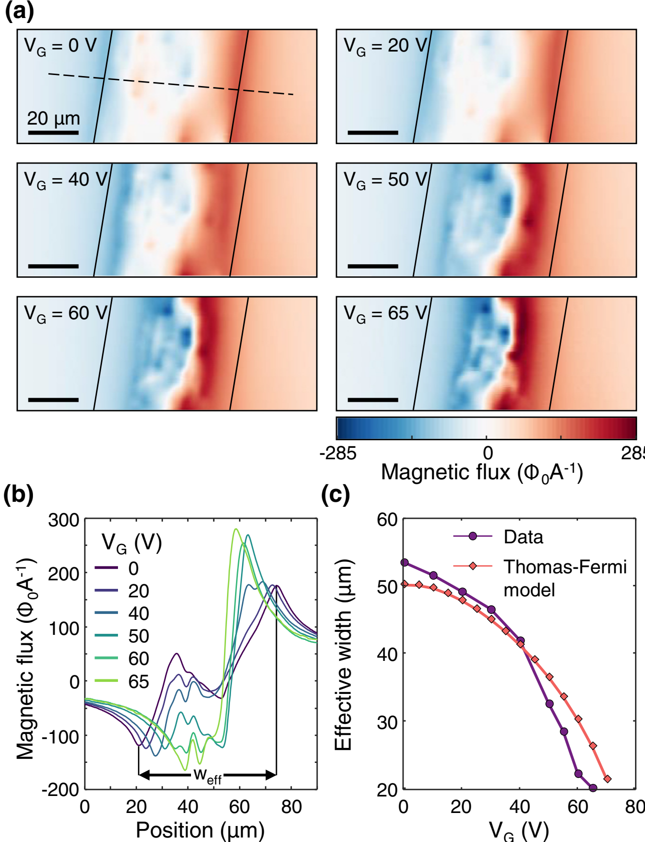

FIG. 4. (a) Magnetic flux images of current flow in a 60-µm-wide LAO/STO device, at various V_G. The black solid lines indicate the edges of the channel at $V_G = 0$ V. Note that the inhomogeneity inside the device is caused by disorder in the sample, and is enhanced at lower carrier densities. $\Phi_0 = h/2e$ is the magnetic flux quantum, and the measured flux is normalized by the applied current. (b) Line cuts of the magnetic flux taken along the dashed line in (a). The effective width of the sample is measured as the distance between the positive and negative peaks of the magnetic field (indicated on the figure for $V_G = 0$ V). (c) Effective width of the device as a function of V_G (purple circles), compared with a calculation for a 50-µm-wide homogeneous device (red diamonds). For the simulation, we assumed the initial carrier density was 3×10^{13} cm^{-2}, and that the threshold density required for conductivity was 1.2×10^{13} cm^{-2}.

at higher V_G, can be attributed to the presence of disorder in the sample.

IV. DISCUSSION

To conclude, we showed that electrostatic gating in STO-based interfaces results in a significantly reduced carrier density near the edges of the device. These effects are caused by electric field focusing at the edges of the device. We experimentally studied how the inhomogeneous carrier density affects the current flow in patterned LAO/STO devices and showed that insulating regions nucleate at the edges of the device, due to the carrier density suppression.

The field focusing effect is more dominant for smaller devices, making the back gate more effective for narrow Hall bar geometries. Indeed, even though the mobility and sheet resistance of ungated LAO/STO samples are typically independent of device width [37], their properties significantly vary once gated. Wider devices (100's of µm) typically require voltages in excess of 100 V in order to generate a change of 1×10^{13} cm^{-2} in the carrier density [7,10,11,25], while narrower devices (10's of µm) require a few dozen volts to generate the same change [12]. Devices narrower than 10 µm were shown to produce that change with a gate voltage of 2 V [24].

The lower working voltages come at the expense of the transport current inhomogeneities. In devices with narrow voltage leads, the field focusing may render the leads insulating, leading to high contact resistance while the device under study remains metallic. The reduced effective width should also be taken into account when interpreting sheet resistance and Hall effect measurements. Further experiments combining spatially resolved techniques and transport measurements are required to shed light on the influence of the finite-size effects reported here on the plethora of gate-tunable electronic phenomena at LAO/STO interfaces.

We note that our model neglects the effects of disorder on the carrier density profile; it is evident from the data that disorder plays an important role in determining the current patterns at low carrier densities. Current is diverted away from areas with locally reduced conductivity, appearing as dipolelike features in the magnetic flux maps. The appearance of such features at low carrier densities is consistent with previous reports of a percolationlike metal-insulator transition in LAO/STO [12,13]. An additional effect of disorder that has not been taken into account is the resulting diffusive motion of the electrons. Diffusive behavior will affect the electronic density profile by smearing fast variations. This can be taken into account using a Smoluchowski-type equation. However, given that we observe density modulations down to the resolution limit of our probe we conclude that diffusion does not play a crucial role in determining the density profile in Fig. 4. Furthermore, the Thomas-Fermi approximation limits the applicability of our model to devices wider than the Thomas-Fermi screening length. For the two-dimensional system, the Thomas-Fermi length is given by $r_{\mathrm{TF}} \approx 2\pi a_B^*$, where $a_B^* = \hbar^2\epsilon/m_{\mathrm{eff}}e^2$ is the effective Bohr radius. For LAO/STO, this translates to $r_{\mathrm{TF}} \approx 35$ nm. Devices of width comparable or lower than this can be generated in LAO/STO structures, either through top gates [15], or using conductive atomic force microscopy [33]. Back-gating these devices could significantly change the carrier density profile throughout the device, requiring a more detailed Schrödinger-Poisson modeling.

Finally, we discuss the applicability of our modeling to other two-dimensional systems, such as GaAs/AlGaAs quantum wells or van der Waals heterostructures. In these materials, the distance between the gate electrode and the 2D system is typically much smaller compared to LAO/STO, and the dielectric constant is small and linear. Thus, the carrier suppression would be small in large (several microns wide) devices. The edges of nanoscale devices, however, may be strongly affected.

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