# Building programmable integrated circuits through disordered Chern insulators

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We study the construction of programable integrated circuits with the help of disordered Chern insulators. Specifically, the schemes for low dissipation logic devices and connecting wires are proposed. We use the external-gate-induced step voltage to construct spatially adjustable channels, where these channels take the place of the conventional wires. Our numerical calculation manifests that the external gates can be adopted to program the arbitrary number of wires ($n$-to-$m$ connections). We find that their electron transport is dissipationless and robust against gate voltage fluctuation and disorder strength. Furthermore, seven basic logic gates distinct from the conventional structures are proposed. Our proposal has potential applications in low power-integrated circuits and enlightens the building of integrated circuits in topological materials.

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## I. INTRODUCTION

The integrated circuits made up of metallic wires and logic devices have significantly improved information processing efficiency and dramatically rebuilt our lifestyle [1–3]. However, the power dissipation for such devices is one of the most focused challenges, where lots of energy is wasted due to the existence of resistance. In conventional printed circuit boards [see Fig. 1(a)], the connections between electronic components are exclusively determined by conductor pattern (metallic wires), in which electron transport is inevitably dissipated [4–6]. Furthermore, the complicated structure of logic devices also suffers from heavy joule heat, which also induces overheating troubles [7,8]. To overcome those problems, topological insulators attracted great interest over the past decades [9–17]. These systems are predicted to possess the dissipationless topological edge states and are considered as candidates of ideal wires in integrated circuits [18,19]. Nevertheless, the edge state always sits at the boundary, and its shape is only determined by the geometry of the sample, which limits its applications.

Fortunately, the conducting channels also emerge at the interfaces between two topologically distinct materials [20–23]. Especially at the interfaces between quantum anomalous Hall phases with different Chern numbers, the one-dimensional chiral states with dissipationless transport are available [24,25]. Compared to the topological edge states, the interface states exhibit higher tunability, engineered spatially. Recently, we proposed the existence of a chiral interface state with quantized transport in disordered CIs [26]. Generally, the Hall conductivity $\sigma_{xy}$ for a disordered CI is $e^2/h$ inside the mobility gap, while it sharply jumps to 0 at two mobility edges since all the bulk states are localized by Anderson disorder [26–32]. When a step potential is adopted by an external gate, the Chern number of two adjacent areas (separated by external gates) can be 0 and 1, respectively. Hence, the dissipationless chiral channels, which are spatially adjustable by external gates, emerge at the interface [26].

In this paper, we show that the interface channels with arbitrary trajectories can be constructed by controlling the external gates in disordered CIs, and its robustness against backscattering is also preserved. Utilizing such perfect transport properties, we propose a programable circuit board. As shown in Fig. 1(b), the central region of the sample is divided into several blocks, among which appropriate gate voltage arrangements are considered to program the required wires to connect the corresponding devices. Our numerical results manifest that the partition of the current can also be realized in this programable circuit, and the number of branch wires can be adjusted by external gate voltage manipulation. Significantly, the programable chiral interface channels can also be adopted to construct all seven basic logic gates [33–36]. These structure-simplified logic gates are compatible with wires, which take full advantage of disordered Chern insulators' (CIs) topological nature. Our proposal of dissipationless wires and basic logic gates provide a route to build integrated circuits in topological systems.

## II. MODEL AND METHOD

Our investigation is based on Qi-Wu-Zhang CI model [37], and the Hamiltonian in the square lattice reads

$$H=\sum_i\left[c_i^\dagger\left(\frac{t\sigma_z}{2}-iv\sigma_y\right)c_{i+\hat{x}}+c_i^\dagger\left(\frac{t\sigma_z}{2}-iv\sigma_x\right)c_{i+\hat{y}}+\text{H.c.}\right]$$
$$+\sum_i[c_i^\dagger(m-2t)\sigma_z c_i+c_i^\dagger(V_i+W_i)\sigma_z c_i], \quad (1)$$

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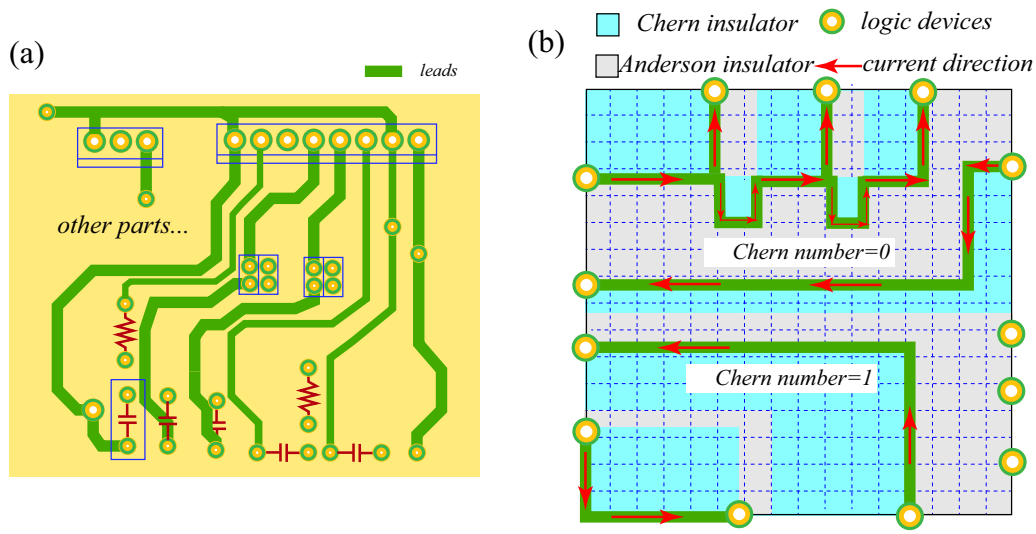



FIG. 1. (a) Schematic plot of a conventional printed circuit board. The orange areas are the background. The solid green lines are the wires and the logic devices are marked in yellow circles. (b) Schematic plot of a programmable integrated circuit based on disordered CIs. The central region is divided into several cyan and gray blocks. The red arrows denote the current directions.

where $c_i^\dagger$ ($c_i$) is the creation (annihilation) operator on site $i$. $\sigma_{x,y,z}$ are Pauli matrices and $\sigma_0$ is the $2 \times 2$ identity matrix. The parameters are fixed at $v = 0.5t$, $m = t$, where $v$, $m$ and $t$ are Fermi velocity, mass, and hopping energy, respectively. $V_i$ shows the profile of the gate-induced potential, and $W_i$ is the Anderson disorder uniformly distributed within $[-\frac{W}{2}, \frac{W}{2}]$. $W$ is the disorder strength.

The nonequilibrium Green's function method [38,39] is adopted to simulate the transport properties with $G_{pq} = \frac{e^2}{h} Tr[\Gamma_p G^r \Gamma_q G^a]$ the conductance between terminals $p$ and $q$. $G^{r/a} = [E_F \pm i0^+ - H - \sum_p \Sigma_p]^{-1}$ are the retarded/advanced Green's function, and $\Gamma_p = i[\Sigma_p - \Sigma_p^\dagger]$ is a linewidth function with $\Sigma_p$ the self-energy of terminal $p$. The local current flow vector is calculated by

$$\mathbf{J}_{i\to j} = \frac{2e^2 V}{h} Im[H_{i,j}(G^r \Gamma_L G^a)_{j,i}]. \tag{2}$$

$H_{i,j}$ is the coupling matrix between $i$ and $j$ sites. The local current flow vector for site $i$ is $\mathbf{J}_i = [\mathbf{J}_{i\to i+\hat{x}} + \mathbf{J}_{i\to i+\hat{y}}]$.

## III. PROGRAMMABLE CIRCUIT WIRES

The wires and the logic gates are basic building blocks for conventional integrated circuits. We first propose the realization of programable "wires" with the help of disordered CIs. The transport properties of a typical device are studied as illustrated in Fig. 2(a). The central region is divided into $6 \times 6$ little blocks, where each block is attached with an external gate. The blocks' potential can be manipulated by the corresponding gates independently. To simulate the typical cases in printed circuits's boards, the gate voltage takes two discrete standard values $V_a$ and $V_b$ for white and blue blocks, respectively. Furthermore, 12 logic devices are considered, which are labeled as $(U_1, U_2, U_3)$, $(D_1, D_2, D_3)$, $(L_1, L_2, L_3)$, and $(R_1, R_2, R_3)$ connecting the up, down, left, and right boundaries, respectively.

Three cases are investigated to illuminate the highly programable wires based on the dissipationless chiral-interface states. For simplicity, the standard gate voltage for the white (blue) blocks are chosen as $V_a = -2.8t$ ($V_b = 0$, if exists) with the Chern number $C = 0$ ($C = 1$) [26]. In the first case, all gate voltages in blocks are set as $V_a$ [see Fig. 2(b)]. The entire sample belongs to the Anderson insulator with $C = 0$. One can see from the typical local current density distribution [Fig. 2(b)] and the conductance $G = 0$ [Fig. 2(c)], all logic devices in the circuit board are completely disconnected due to Anderson localization. In the second and the third cases, the gate voltages of blocks are programed as configurations in Figs. 2(d) and 2(g). The Chern number is $C = 1$ in the blue blocks with $V_b = 0$, and their difference between blue and white blocks guarantees the emergence of chiral interface channels labeled by the solid red lines with arrows. As shown in Figs. 2(d) and 2(g), channel connecting device $L3$ ($L2$) and $R2$ ($D2$) is obtained. Therefore, it is appropriate to summarize that any two devices of a circuit can be switched into "on" and "off" by properly arranging the gate voltage $V_a$, $V_b$.

In realistic samples, the disorder strength $W$ and gate voltage $V_a/V_b$ may deviate from the standard values because of the immature fabricating processes. To examine the robustness of wires in the programable circuit boards, we investigate the differential conductance $G$ versus $W$ for different $V_a/V_b$. As shown in Fig. 2(c), the localization behaviors for states in Fig. 2(b) are insensitive to the variation of $V_a$ and $W$. The plots in Figs. 2(e) and 2(f) and Figs. 2(h) and 2(i) correspond to the configurations in Figs. 2(d) and 2(g), respectively. The quantized $G = e^2/h$ plateau exists for different gate voltages and a wide range of disorder strength, indicating the transport of these interface channels are robust against the variation of gate voltages and disorder strength. To be specific, when $V_a$ ($V_b$) takes the standard value $-2.8t$ ($0t$), the $G = e^2/h$ plateau holds within a wide disorder strength range $W \in [2.4t, 4.4t]$. When the gate voltages on blue and white blocks deviate from the standard value, the plateau width shrinks slightly. Nevertheless, it is worth noting that as long as $V_a \in [-3t, -2.6t]$

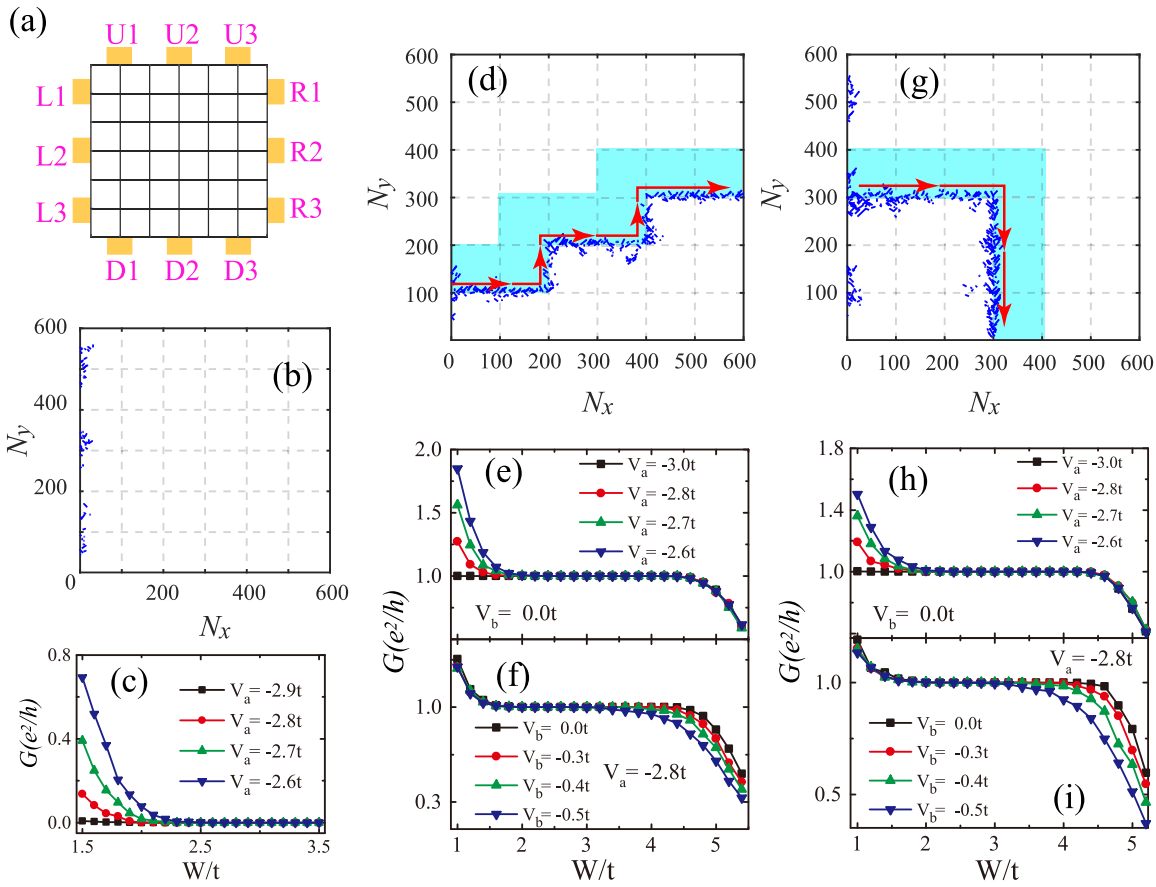



FIG. 2. (a) Schematic of programable circuit device. The central region is divided into $6 \times 6$ blocks with size $100a \times 100a$, where $a$ is lattice constant. (b), (d), (g) Local current density distribution corresponding to (a) with disorder strength $W = 3.5t$ under different gate voltage configuration. Here, the gate voltage on white and blue blocks are $V_a$ and $V_b$, which take the standard values $V_a = -2.8t$, $V_b = 0$ if not specified. The red arrows denote the chiral interface channels. (c) Differential conductances $G$ of case (b) versus $W$ under different $V_a$. [(e),(f)] and [(h),(i)] are similar to those in (c), except $G$ for cases (d) and (g), respectively.

and $V_b \in [-0.4t, 0]$, one can always achieve the quantized $G = e^2/h$ plateau with disorder strength $W \in [2.4t, 3.6t]$. This phenomenon indicates that the dissipationless programable circuit "wires" have a high fault tolerance feature for both gate voltage and disorder.

Furthermore, we also study the gate voltage configurations shown in Figs. 3(a) and 3(e). These two gate voltage configurations enable the simultaneous connection of two and three sets of devices [i.e., ($L1$-$R2$/$L2$-$R3$) in Fig. 3(b) and ($L1$-$R1$/$L2$-$R2$/$L3$-$R3$) in Fig. 3(f)]. Figures 3(c) and 3(d) and Figs. 3(g) and 3(h) manifest that the quantized $G$ capture the double ($G = 2e^2/h$) and triple ($G = 3e^2/h$) disspationless channels, respectively. Compared to those in Fig. 2, the parameter regions of $W$ and $V_a/V_b$ for quantized plateaus $2e^2/h$ ($3e^2/h$) are nearly unchanged. It means that the parameter's optimization is not needed when the single wire is replaced by the multiple wire. Hence, such disordered-CIs-based programable wires possess fantastic potential applications due to their flexibility for device connection ($V$-tunable) and the robustness against parameter variation.

One can also program the chiral interface channels as current splitters, leading to a one-to-many connection between devices. Such a connection requires a more careful arrangement of gate voltages. For example, as shown in Figs. 4(a) and 4(d), one-to-two and one-to-three connections are obtained. The corresponding local current density distributions [see Figs. 4(b) and 4(e)] agree with the current flowing in the directions marked by red arrows.

To quantitatively study one-to-many wire connections, we pay more attention to the dependence of the current partition on the gate voltage $V_b$ [see Figs. 4(c) and 4(f)]. The differential conductance between different devices are studied, where $G_{Ri,L2}$ signals the currents partitioned into device $Ri$ from device $L2$. And the summation $G = \sum_{i\in[1,2,3]} G_{Ri,L2}$ gives the total conductance. From Figs. 4(c) and 4(f), one finds that $G$ still holds the quantized value $e^2/h$ with $G_{Ri,L2}$ unquantized for $V_b \in [-0.4t, 0.4t]$. Specifically, when $V_b$ takes the standard gate voltage ($V_b = 0t$), all $G_{Ri,L2}$ take the large values. It means that each branch wire is well connected. Furthermore, the conductance $G_{Ri,L2}$ varies with $V_b$, which provides a possible way to manipulate the current partition relations between branches.

We close this section by discussing the voltage and energy loss for such a configuration. As shown in Fig. 4(b), the incident electrons are scattered at the bifurcation point. The backscattering is forbidden at the bifurcation point due to the spatial separation of the backscattering channels [38].

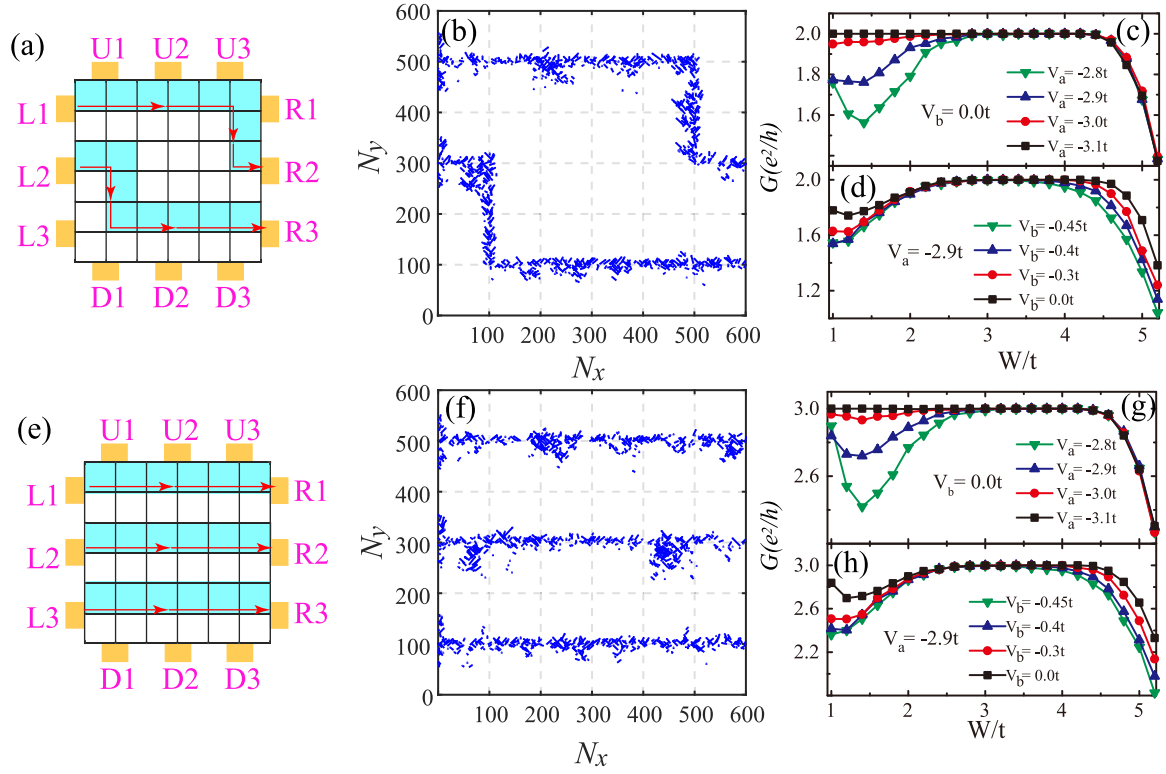



FIG. 3. [(a),(e)] Schematic of programable circuit devices, which have two and three chiral interface channels, respectively. [(b),(f)] Local current density distribution corresponding to cases [(a),(e)] with gate voltage $V_a = -2.8t$, $V_b = 0$ and disorder strength $W = 3.5t$. [(c),(d)] and [(g),(h)] Conductances $G$ *vs* $W$ for different $V_a$ and $V_b$, respectively.

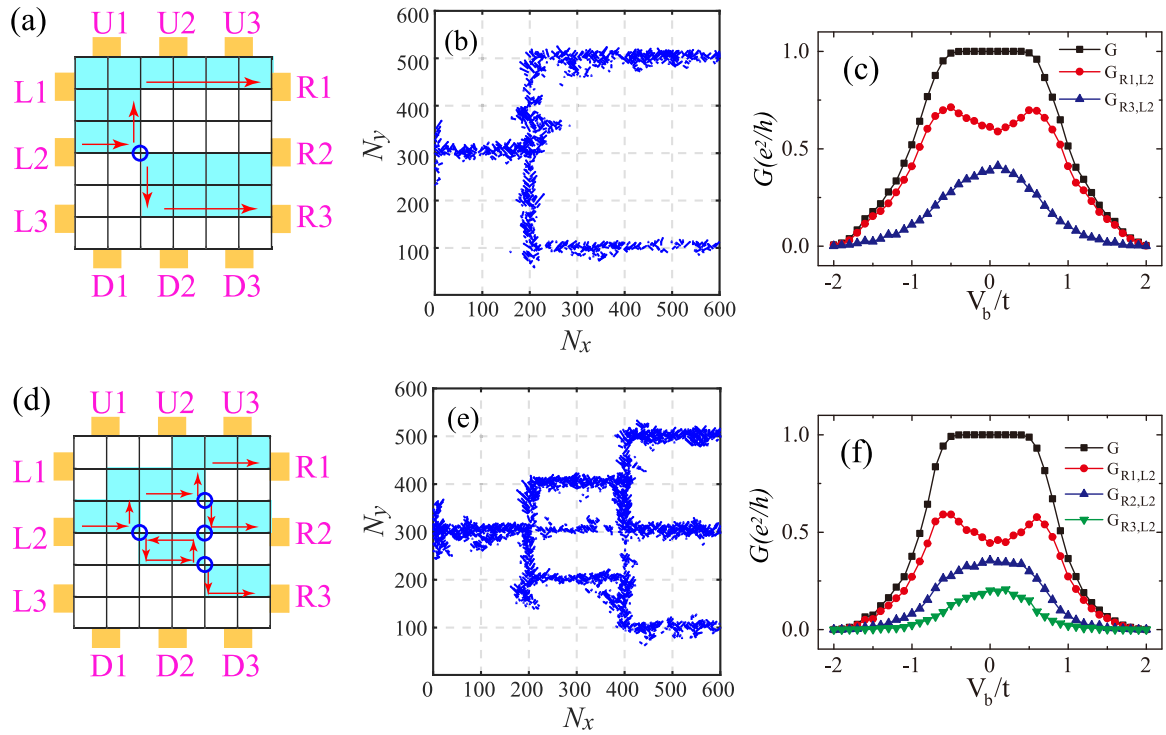
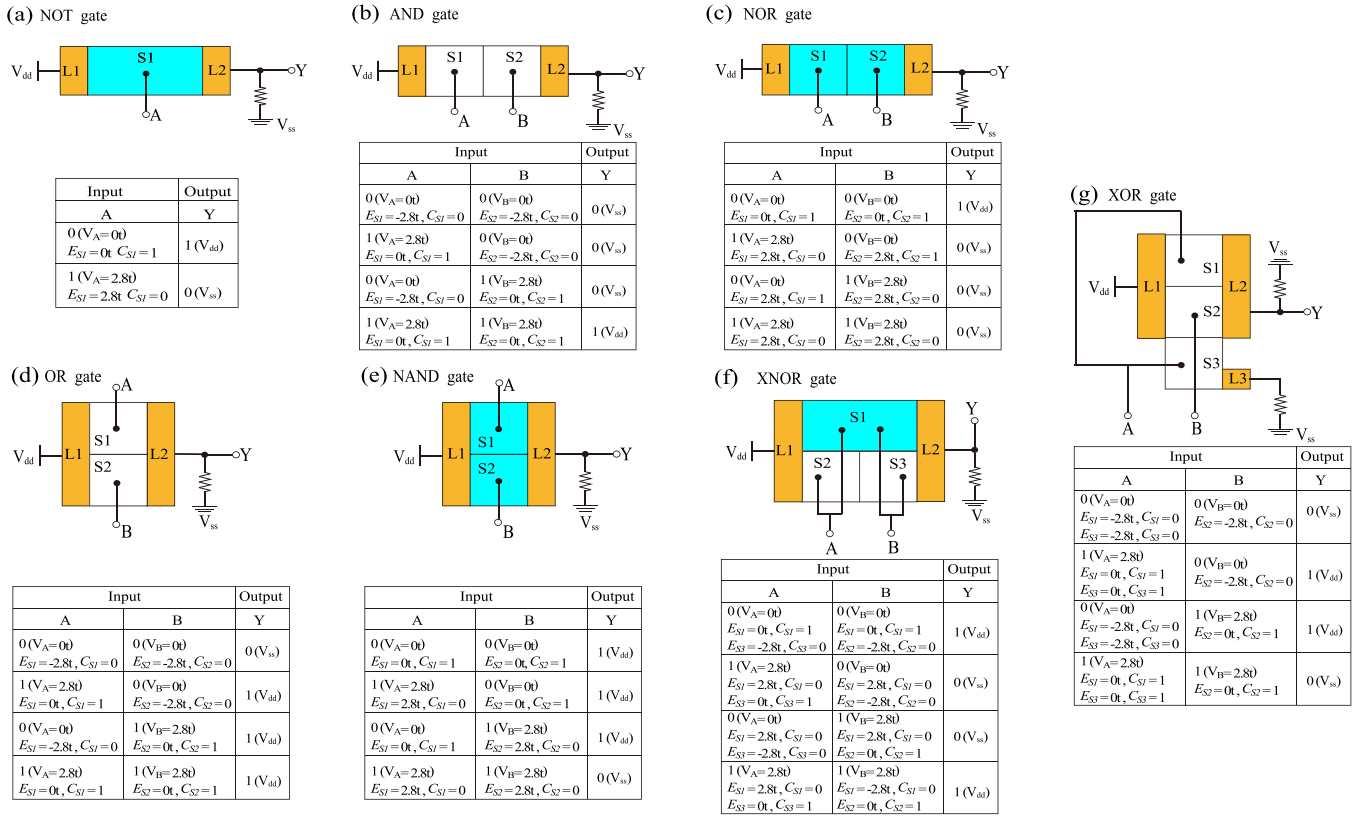



FIG. 4. [(a),(d)] The schematic diagram of gate voltage configuration to realize two and three branches of current in integrated circuits devices, respectively. The blue circles denote bifurcation points of current. [(b),(e)] Local current density distribution corresponding to [(a),(d)], respectively, with $V_a = 0$, $V_b = -2.8t$ and disorder strength $W = 3.5t$. [(c),(f)] The branch conductance $G_{R1,L2}$, $G_{R2,L2}$, $G_{R3,L2}$, and the total conductance $G$ vs $V_b$ with $V_a = 0$ and $W = 3.5t$.




| Input | Output |
|---|---|
| A | Y |
| 0 ($V_A$=0t) $E_{S1}$=0t $C_{S1}$=1 | 1 ($V_{dd}$) |
| 1 ($V_A$=2.8t) $E_{S1}$=2.8t $C_{S1}$=0 | 0 ($V_{ss}$) |

| Input | | Output |
|---|---|---|
| A | B | Y |
| 0 ($V_A$=0t) $E_{S1}$=-2.8t, $C_{S1}$=0 | 0 ($V_B$=0t) $E_{S2}$=-2.8t, $C_{S2}$=0 | 0 ($V_{ss}$) |
| 1 ($V_A$=2.8t) $E_{S1}$=0t, $C_{S1}$=1 | 0 ($V_B$=0t) $E_{S2}$=-2.8t, $C_{S2}$=0 | 0 ($V_{ss}$) |
| 0 ($V_A$=0t) $E_{S1}$=-2.8t, $C_{S1}$=0 | 1 ($V_B$=2.8t) $E_{S2}$=0t, $C_{S2}$=1 | 0 ($V_{ss}$) |
| 1 ($V_A$=2.8t) $E_{S1}$=0t, $C_{S1}$=1 | 1 ($V_B$=2.8t) $E_{S2}$=0t, $C_{S2}$=1 | 1 ($V_{dd}$) |

| Input | | Output |
|---|---|---|
| A | B | Y |
| 0 ($V_A$=0t) $E_{S1}$=0t, $C_{S1}$=1 | 0 ($V_B$=0t) $E_{S2}$=0t, $C_{S2}$=1 | 1 ($V_{dd}$) |
| 1 ($V_A$=2.8t) $E_{S1}$=2.8t, $C_{S1}$=0 | 0 ($V_B$=0t) $E_{S2}$=2.8t, $C_{S2}$=1 | 0 ($V_{ss}$) |
| 0 ($V_A$=0t) $E_{S1}$=2.8t, $C_{S1}$=1 | 1 ($V_B$=2.8t) $E_{S2}$=2.8t, $C_{S2}$=0 | 0 ($V_{ss}$) |
| 1 ($V_A$=2.8t) $E_{S1}$=2.8t, $C_{S1}$=0 | 1 ($V_B$=2.8t) $E_{S2}$=2.8t, $C_{S2}$=0 | 0 ($V_{ss}$) |

| Input | | Output |
|---|---|---|
| A | B | Y |
| 0 ($V_A$=0t) $E_{S1}$=-2.8t, $C_{S1}$=0 | 0 ($V_B$=0t) $E_{S2}$=-2.8t, $C_{S2}$=0 | 0 ($V_{ss}$) |
| 1 ($V_A$=2.8t) $E_{S1}$=0t, $C_{S1}$=1 | 0 ($V_B$=0t) $E_{S2}$=-2.8t, $C_{S2}$=0 | 1 ($V_{dd}$) |
| 0 ($V_A$=0t) $E_{S1}$=-2.8t, $C_{S1}$=0 | 1 ($V_B$=2.8t) $E_{S2}$=0t, $C_{S2}$=1 | 1 ($V_{dd}$) |
| 1 ($V_A$=2.8t) $E_{S1}$=0t, $C_{S1}$=1 | 1 ($V_B$=2.8t) $E_{S2}$=0t, $C_{S2}$=1 | 0 ($V_{ss}$) |

| Input | | Output |
|---|---|---|
| A | B | Y |
| 0 ($V_A$=0t) $E_{S1}$=0t, $C_{S1}$=1 | 0 ($V_B$=0t) $E_{S2}$=0t, $C_{S2}$=1 | 1 ($V_{dd}$) |
| 1 ($V_A$=2.8t) $E_{S1}$=2.8t, $C_{S1}$=0 | 0 ($V_B$=0t) $E_{S2}$=0t, $C_{S2}$=1 | 1 ($V_{dd}$) |
| 0 ($V_A$=0t) $E_{S1}$=0t, $C_{S1}$=1 | 1 ($V_B$=2.8t) $E_{S2}$=2.8t, $C_{S2}$=0 | 1 ($V_{dd}$) |
| 1 ($V_A$=2.8t) $E_{S1}$=2.8t, $C_{S1}$=0 | 1 ($V_B$=2.8t) $E_{S2}$=2.8t, $C_{S2}$=0 | 0 ($V_{ss}$) |

| Input | | Output |
|---|---|---|
| A | B | Y |
| 0 ($V_A$=0t) $E_{S1}$=0t, $C_{S1}$=1 $E_{S3}$=-2.8t, $C_{S3}$=0 | 0 ($V_B$=0t) $E_{S2}$=0t, $C_{S2}$=1 | 1 ($V_{dd}$) |
| 1 ($V_A$=2.8t) $E_{S1}$=2.8t, $C_{S1}$=0 $E_{S3}$=0t, $C_{S3}$=1 | 0 ($V_B$=0t) $E_{S2}$=-2.8t, $C_{S2}$=0 | 0 ($V_{ss}$) |
| 0 ($V_A$=0t) $E_{S1}$=2.8t, $C_{S1}$=0 $E_{S3}$=-2.8t, $C_{S3}$=0 | 1 ($V_B$=2.8t) $E_{S2}$=0t, $C_{S2}$=1 | 0 ($V_{ss}$) |
| 1 ($V_A$=2.8t) $E_{S1}$=2.8t, $C_{S1}$=0 $E_{S3}$=0t, $C_{S3}$=1 | 1 ($V_B$=2.8t) $E_{S2}$=-2.8t, $C_{S2}$=0 | 1 ($V_{dd}$) |

| Input | | Output |
|---|---|---|
| A | B | Y |
| 0 ($V_A$=0t) $E_{S1}$=-2.8t, $C_{S1}$=0 $E_{S3}$=-2.8t, $C_{S3}$=0 | 0 ($V_B$=0t) $E_{S2}$=-2.8t, $C_{S2}$=0 | 0 ($V_{ss}$) |
| 1 ($V_A$=2.8t) $E_{S1}$=0t, $C_{S1}$=1 $E_{S3}$=0t, $C_{S3}$=1 | 0 ($V_B$=0t) $E_{S2}$=-2.8t, $C_{S2}$=0 | 1 ($V_{dd}$) |
| 0 ($V_A$=0t) $E_{S1}$=-2.8t, $C_{S1}$=0 $E_{S3}$=-2.8t, $C_{S3}$=0 | 1 ($V_B$=2.8t) $E_{S2}$=0t, $C_{S2}$=1 | 1 ($V_{dd}$) |
| 1 ($V_A$=2.8t) $E_{S1}$=0t, $C_{S1}$=1 $E_{S3}$=0t, $C_{S3}$=1 | 1 ($V_B$=2.8t) $E_{S2}$=0t, $C_{S2}$=1 | 0 ($V_{ss}$) |

FIG. 5. (a)–(g) The schematic diagram of seven basic logic gates and the corresponding truth tables. The central region is divided into one, two, or three blocks labeled by $S1$, $S2$, or $S3$, respectively. $A$ and $B$ denote voltage input terminals, connected to the gate on the corresponding block $S1$, $S2$, or $S3$. $Y$ denotes voltage output terminal. $V_{dd}$ and $V_{ss}$ represent supply and source voltage. $L1$ and $L2$ or $L3$ represent the left and right terminals connected to the central region. When the voltage signal $V_A = V_B = 0$, the initial Fermi energy in the blue block is $E_f = 0$ (i.e., the CI with Chern number $C = 1$), and in the white block is $E_f = -2.8t$ (i.e., the Anderson insulator with $C = 0$).

Since we only focus on the elastic scattering rather than inelastic scattering in our numerical calculations, the resistance is only determined by the backscattering. Therefore, the absence of backscattering results in a vanishing resistance at the bifurcation point, and consequently the voltage drop at the bifurcation point is zero [38]. Also, there is no energy loss at the bifurcation point, and the dissipationless properties of the circuit boards are consistent with the quantized total conductance $G = e^2/h$ [see Fig. 4(c)]. According to all studied configurations, one concludes that the external gates can be adopted to program the wires with arbitrary ($n$-to-$m$) connections in disordered CIs.

## IV. DISORDERED-CIS-BASED NEW LOGIC GATE

Apart from being used as programable dissipationless wire, disordered CIs also have a promising application in designing logic devices. Generally, the logic devices are constructed by seven basic logic gates. At present, the conventional logic gates have relatively complicated structures. Taking the CMOS-based logic gate AND gate as an example, it is constructed by the combination of NAND gate and NOT gate. The NAND gate requires two pairs of PMOS and NMOS, while the NOT gate requires one pair of PMOS and NMOS. Comparing with the conventional logic gates, the structures of disordered-CIs-based logic gates are greatly simplified by taking advantage of gate-voltage-programable chiral edge and interface states.

Figures 5(a) to 5(g) illustrate the construction schemes of seven basic logic gates and the corresponding truth tables. Each of these seven logic gates has a central region, divided into several blocks. $A$ and $B$ denote two input terminals with voltage signals $V_A$ and $V_B$. $V_{dd}$ and $V_{ss}$ are supply and source voltages, respectively. The initial Fermi energy in the blue block is $E_f = 0$ (i.e., the Chern number $C = 1$) and in the white block is $E_f = -2.8t$ (i.e., the Anderson insulator with $C = 0$). For clarity, the Fermi energy $E_{S1}$ ($E_{S2}$ and $E_{S3}$) and Chern number $C_{S1}$ ($C_{S2}$ and $C_{S3}$) for block $S1$ ($S2$ and $S3$) are shown in the truth table. The corresponding logic gate for different cases of voltage input are $V_A$, $V_B$. Importantly, we set $V_{A/B} = V_{dd} = 2.8t$ as the rated high level (i.e., logical "1") and $V_{A/B} = V_{ss} = 0t$ as the rated low level (i.e., logical "0").

Here, we take two of these seven logic gates as examples for a detailed analysis. Figure 5(d) illustrates how the OR gate works. When $V_A = V_B = 0t$, $S1$ and $S2$ have the Fermi energy $E_{S1} = E_{S2} = -2.8t$, and the corresponding Chern number is $C_{S1} = C_{S2} = 0$. Thus, there is no current flowing into $L2$, and one has $V_Y = V_{ss}$ (i.e., the logical operation: $0 + 0 = 0$). When $V_A = 2.8t$, $V_B = 0t$, the Chern number of $S1$ becomes $C_{S1} = 1$ ($C_{S2}$ remains 0). The chiral interface channel emerges between $S1$ and $S2$. The current input from $L1$ will flow into $L2$ along this channel, and thus $V_Y = V_{dd}$ (i.e., $1 + 0 = 1$). For

the last two cases $V_A = 0t$, $V_B = 2.8t$ (i.e., $C_{S1} = 0$, $C_{S2} = 1$) or $V_A = V_B = 2.8t$ (i.e., $C_{S1} = C_{S2} = 1$), the current will flow into $L2$ along the lower edge of $S1$, and thus $V_Y = V_{dd}$ (i.e., $0 + 1 = 1$ and $1 + 1 = 1$).

Similarly, Fig. 5(g) illustrates how the XOR gate works. The central region is divided into three blocks $S1$, $S2$, and $S3$. Signal input terminal $A$ is connected to the gates on both $S1$ and $S3$, $B$ is connected to the gate on $S2$. In the case of $V_A = V_B = 0t$, the entire central region is an Anderson insulator ($C_{S1} = C_{S2} = C_{S3} = 0$) with no current flowing through it (i.e., $\bar{0} \cdot 0 + 0 \cdot \bar{0} = 0$). When $V_A = V_B = 2.8t$, the Chern number of the entire central region is 1 ($C_{S1} = C_{S2} = C_{S3} = 1$), the current will flow into $L3$ along the lower edge of region $S3$, rather than $L2$. Thus, $L2$ is always switched off for both cases with $V_Y = V_{ss}$ (i.e., $\bar{1} \cdot 1 + 1 \cdot \bar{1} = 0$). However, when $V_A = 2.8t$, $V_B = 0t$ ($V_A = 0t$, $V_B = 2.8t$), the Chern number for $S2$ always differs by 1 compared to those for $S1$ and $S3$. The chiral interface channel emerges between $S1$ and $S2$ ($S2$ and $S3$). Generally, the current will flow into $L2$ along the interface channel between $S1$ and $S2$ or between $S2$ and $S3$ with $V_Y = V_{dd}$ (i.e., $\bar{1} \cdot 0 + 1 \cdot \bar{0} = 1$ or $\bar{0} \cdot 1 + 0 \cdot \bar{1} = 1$). The rest of the other logic gates can be analyzed in a similar manner.

Here, the feasibility of our logic gates proposal also originates from the spatial programable of chiral interface states. Compared to the conventional logic gates, the dissipationless transport features of chiral interface states can, in principle, significantly lower the power of logic gates in our cases. Specifically, we also analyze the logical operation of OR gate by investigating the conductance versus disorder strength in the Appendix. The numerical results show that the logical operation is dissipationless and immune to disorder. Finally, the wires are compatible with the logic gates because they can be built based on one disordered CI sample. It will greatly simplify the integrated circuits fabricating process.

## V. CONCLUSION AND DISCUSSION

In summary, we study the realization of a programable integrated circuit based on disordered CIs. Due to the localization features, we propose the chiral interface channels as ideal wires. Significantly, dissipationless wires, which connect the arbitrary required devices, can be obtained by programming samples' gate voltage arrays. In addition to the wires, the disordered CIs can be utilized to construct the basic logic gates. Compared to the conventional counterparts, the simplified logic gates' structures will greatly promote the compaction of integrated circuits. Moreover, combined with the dissipationless characteristics of the wires as well as the logic devices, our proposal will enable circuits with lower power consumption, higher integration, and reliability.

Notably, since the Anderson phase transition is basic and only determined by the system's dimension and symmetry ensemble, our results apply to all two-dimensional CIs that exhibit a direct transition from the CI to the normal insulator. Furthermore, to construct such a programable integrated circuit, one only needs two discrete standard gate voltages ($V_a$ and $V_b$) corresponding to the topologically nontrivial insulator and the normal insulator, respectively. The proposal is still available if $V$ can drive the transition from CI to a band insulator in some systems [40,41]. This also means that it does not matter if there exists a metallic phase during the Anderson transition since one can skip the voltage windows corresponding to the metallic phase [42]. Therefore the CIs can be further broadened to other topological nontrivial systems such as the quantum spin Hall effect, and so on [43–45]. Finally, we discuss the scaling of the integrated circuits, which is limited by the size of gate blocks. For a typical quantum anomalous Hall effect system with Fermi velocity $v_F \approx 5 \times 10^5$ m/s and energy gap $\Delta \approx 20$ meV, the decay length is $\lambda \approx \frac{\hbar v_F}{\Delta} \sim 50$ nm. The limited scaling can be smaller than 0.5 $\mu$m since the gate block will work well if the size is one order of magnitude larger than $\lambda$. Experimentally, our proposal only depends on the size scale for the Anderson transition in CIs. Fortunately, the Anderson localization has been recently observed in $MnBi_2Te_4$ samples of 20 $\mu$ m $\times$ 20 $\mu$m [15,46], indicating the proposed integrated circuits are feasible under the state-of-the-art experimental techniques.

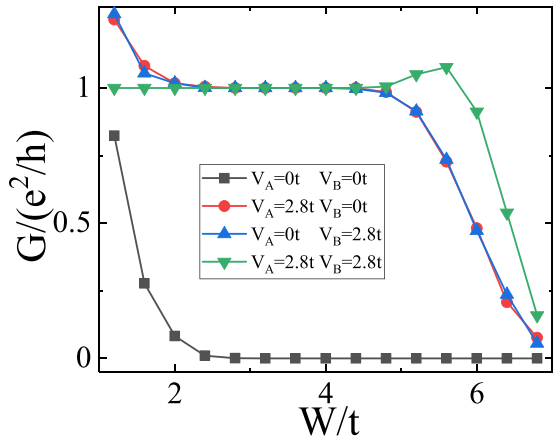



FIG. 6. Differential conductances $G$ versus disorder strength $W$ for *OR gate*.

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## APPENDIX: LOGICAL OPERATION OF *OR GATE*

We take the *OR gate* as an example and calculate the conductance $G$ versus disorder strength $W$ for four cases of voltage input ($V_A$, $V_B$), as shown in Fig. 6. When the output level is logical "1" [i.e., (i) $V_A = 2.8t$, $V_B = 0t$; (ii) $V_A = 0t$, $V_B = 2.8t$; (iii) $V_A = 2.8t$, $V_B = 2.8t$], the quantized $G = e^2/h$ plateau exists within a wide range of disorder strength $W \in [2.4t, 4.4t]$. When the output level is logical "0" (i.e., $V_A = 0t$, $V_B = 0t$), $G = 0$ for the same disorder region. It means that the logical operations of the *OR gate* are dissipationless and robust against disorder.

[1] B. Razavi, *Design of Analog CMOS Integrated Circuits*, (Irwin Electronics & Computer Engineering), 2nd ed., (McGraw-Hill, New York, 2016).

[2] G. E. Moore, Cramming more components onto integrated circuits, Proc. IEEE **86**, 82 (2002).

[3] H. Wang, L. Yu, Y. H. Lee, Y. Shi, and A. Hsu, Integrated circuits based on bilayer mos2 transistors, Nano Lett. **12**, 4674 (2012).

[4] A. C. Marques, J. M. Cabrera, and C. de F. Malfatti, Printed circuit boards: A review on the perspective of sustainability, J. Environ. Manag. **131**, 298 (2013).

[5] A. C. Siegel, S. T. Phillips, M. D. Dickey, N. Lu, Z. Suo, and G. M. Whitesides, Foldable Printed Circuit Boards on Paper Substrates, Adv. Funct. Mater. **20**, 28 (2010).

[6] E. P. Li, X. C. Wei, A. C. Cangellaris, E. X. Liu, Y. J. Zhang, M. D'Amore, J. Kim, and T. Sudo, Progress Review of Electromagnetic Compatibility Analysis Technologies for Packages, Printed Circuit Boards, and Novel Interconnects, IEEE Trans. Electromag. Compat. **52**, 248 (2010).

[7] S. Subrina, D. Kotchetkov, and A. A. Balandin, Heat removal in silicon-on-insulator integrated circuits with graphene lateral heat spreaders, IEEE Electr Device Lett. **30**, 1281 (2009).

[8] J. Koh and R. Colony, Heat transfer of microstructure for integrated circuits, Int. Commun. Heat Mass **13**, 89 (1986).

[9] M. Z. Hasan, and C. L. Kane, Colloquium: Topological insulators, Rev. Mod. Phys. **82**, 3045 (2010).

[10] A. Bansil, H. Lin, and T. Das, Colloquium: Topological band theory, Rev. Mod. Phys. **88**, 021004 (2016).

[11] H. Weng, R. Yu, X. Hu, X. Dai, and Z. Fang, Quantum anomalous Hall effect and related topological electronic states, Adv. Phys. **64**, 227 (2015).

[12] C. Liu, S. C. Zhang, and X. L. Qi, The Quantum Anomalous Hall Effect: Theory and Experiment, Annu. Rev. Condens. Matter. Phys. **7**, 301 (2017).

[13] C. Z. Chang, W. Zhao, D. Y. Kim, H. Zhang, B. A. Assaf, D. Heiman, and J. S. Moodera, High-precision realization of robust quantum anomalous Hall state in a hard ferromagnetic topological insulator, Nat. Mater. **14**, 473 (2015).

[14] X. Kou, S. T. Guo, Y. Fan, L. Pan, M. Lang, Y. Jiang, and J. Tang, Scale-Invariant Quantum Anomalous Hall Effect in Magnetic Topological Insulators Beyond the Two-Dimensional Limit, Phys. Rev. Lett. **113**, 137201 (2014).

[15] Y. Deng, Y. Yu, M. Z. Shi, Z. Guo, Z. Xu, J. Wang, and Y. Zhang, Quantum anomalous Hall effect in intrinsic magnetic topological insulator $MnBi_2Te_4$, Science **367**, 895 (2020).

[16] M. M. Otrokov, I. P. Rusinov, M. Blanco-Rey, M. Hoffmann, A. Y. Vyazovskaya, S. V. Eremeev, and E. V. Chulkov, Unique Thickness-Dependent Properties of the van der Waals Interlayer Antiferromagnet $MnBi_2Te_4$ Films, Phys. Rev. Lett. **122**, 107202 (2019).

[17] A. Rivas, O. Viyuela, and M. A. Martin-Delgado, Density-matrix Chern insulators: Finite-temperature generalization of topological insulators, Phys. Rev. B **88**, 155141 (2013).

[18] Y. Hatsugai, Chern Number and Edge States in the Integer Quantum Hall Effect, Phys. Rev. Lett. **71**, 3697 (1993).

[19] G. M. Graf and M. Porta, Bulk-Edge Correspondence for Two-Dimensional Topological Insulators, Commun. Math. Phys. **324**, 851 (2013).

[20] H. Pan, X. Li, Z. F. Li, and S. A. Yang, Perfect valley filter in a topological domain wall, Phys. Rev. B **92**, 041404(R) (2015).

[21] L. Ju, Z. Shi, N. Nair, Y. Lv, C. Jin, J. Velasco, and A. Zettl, Topological valley transport at bilayer graphene domain walls, Nature (London) **520**, 650 (2015).

[22] J. Li, K. Wang, K. J. McFaul, Z. Zern, Y. F. Ren, K. Watanabe, and J. Zhu, Gate-controlled topological conducting channels in bilayer graphene, Nat. Nanotechnol. **11**, 1060 (2016).

[23] L. J. Yin, H. Jiang, J. B. Qiao, and L. He, Direct imaging of topological edge states at a bilayer graphene domain wall, Nat. Commun. **7**, 11760 (2016).

[24] Y. Ren, J. Zeng, K. Wang, F. Xu, and Z. Qiao, Tunable current partition at zero-line intersection of quantum anomalous Hall topologies, Phys. Rev. B **96**, 155445 (2017).

[25] K. Wang, Y. Ren, X. Deng, S. A. Yang, J. Jung, and Z. Qiao, Gate tunable current partition in graphene based topological zero lines, Phys. Rev. B **95**, 245420 (2017).

[26] Z. Q. Zhang, C. Z. Chen, Y. Wu, H. Jiang, J. Liu, Q. Sun, and X. C. Xie, Chiral Interface States and Related Quantized Transport in Disordered Chern Insulators, Phys. Rev. B **103**, 075434 (2021).

[27] B. Huckestein, Scaling theory of the integer quantum Hall effect, Rev. Mod. Phys. **67**, 357 (1995).

[28] A. Yamakage, K. Nomura, K. I. Imura, and Y. Kuramoto, Criticality of the metal-topological insulator transition driven by disorder, Phys. Rev. B **87**, 205141 (2013).

[29] F. Evers, and A. D. Mirlin, Anderson Transitions, Rev. Mod. Phys. **80**, 1355 (2008).

[30] A. M. M. Pruisken, Universal Singularities in the Integral Quantum Hall Effect, Phys. Rev. Lett. **61**, 1297 (1988).

[31] M. Onoda and N. Nagaosa, Quantized Anomalous Hall Effect in Two-Dimensional Ferromagnets: Quantum Hall Effect in Metals, Phys. Rev. Lett. **90**, 206601 (2003).

[32] C. W. J. Beenakker, Random-matrix theory of quantum transport, Rev. Mod. Phys. **69**, 731 (1997).

[33] D. Gentili, P. Sonar, F. Liscio, T. Cramer, L. Ferlauto, F. Leonardi, and M. Cavallini, Logic-gate devices based on printed polymer semiconducting nanostripes, Nano Lett. **13**, 3643 (2013).

[34] A. P. Chandrakasan and S. Sheng, Low-Power CMOS Digital Design, IEICE J. Solid-St. Circ. **27**, 473 (1992).

[35] Y. Huang, X. Duan, Y. Cui, L. J. Lauhon, K. H. Kim, and C. M. Lieber, Logic gates and computation from assembled nanowire building blocks, Science **294**, 1313 (2001).

[36] B. Radisavljevic, M. B. Whitwick, and A. Kis, Integrated Circuits and Logic Operations Based on Single-Layer $MoS_2$, ACS Nano **5**, 9934 (2011).

[37] X. L. Qi, Y. S. Wu, and S. C. Zhang, Topological quantization of the spin Hall effect in two-dimensional paramagnetic semiconductors, Phys. Rev. B **74**, 085308 (2006).

[38] S. Datta, *Electronic Transport in Mesoscopic Systems*, 2nd ed. (Cambridge University Press, Cambridge, England, 1995).

[39] J. Wang, and H. Guo, Relation between nonequilibrium Green's function and Lippmann-Schwinger formalism in the first-principles quantum transport theory, Phys. Rev. B **79**, 045119 (2009).

[40] M. Ezawa, Valley-Polarized Metals and Quantum Anomalous Hall Effect in Silicene, Phys. Rev. Lett. **109**, 055502 (2012).

[41] W. K. Tse, Z. Qiao, Y. Yao, A. H. MacDonald, and Q. Niu, Quantum anomalous Hall effect in single-layer and bilayer graphene, Phys. Rev. B **83**, 155447 (2011).

[42] M. Onoda, Y. Avishai, and N. Nagaosa, Localization in a Quantum Spin Hall System, Phys. Rev. Lett. **98**, 076802 (2007).

[43] X. Qian, J. Liu, L. Fu, and J. Li, Quantum Spin Hall Effect in Two-Dimensional Transition Metal Dichalcogenides, Science **346**, 1344 (2014).

[44] X. L. Qi and S. C. Zhang, Topological insulators and superconductors, Rev. Mod. Phys. **83**, 1057 (2011).

[45] F. Schindler, A. M. Cook, M. G. Vergniory, Z. Wang, S. S. P. Parkin, B. A. Bernevig, and T. Neupert, Higher-order topological insulators, Sci. Adv. **4**, 0346 (2018).

[46] H. Li, C. Z. Chen, H. Jiang, and X. C. Xie, arXiv:2107.04752 [Phys. Rev. Lett. (to be published)].