Electronic transport in submicrometric channels at the $LaAlO_3/SrTiO_3$ interface

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Nanoscale channels realized at the conducting interface between $LaAlO_3$ and $SrTiO_3$ provide a perfect playground to explore the effect of dimensionality on the electronic properties of complex oxides. Here we compare the electric transport properties of devices realized using the atomic force microscope-writing technique and conventional photolithography. We find that the lateral size of the conducting paths has a strong effect on their transport behavior at low temperature. We observe a crossover from a metallic to an insulating regime occurring at about 50 K for channels narrower than 100 nm. The insulating upturn can be suppressed by the application of a positive backgate. We compare the behavior of nanometric constrictions in lithographically patterned channels with the result of model calculations, and we conclude that the experimental observations are compatible with the physics of a quantum point contact.

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I. INTRODUCTION

At oxide interfaces, the interplay between confinement effects and the physical properties emerging from the junction of the constituent materials gives rise to a plethora of phenomena unattainable in III–V semiconductor heterostructures. One of the most studied systems is the conducting two-dimensional electron system (2DES) appearing at the interface between $LaAlO_3$ and $SrTiO_3$ [1]. It exhibits a series of interesting properties including gate-tunable superconductivity and spin-orbit coupling [2–4]. Moreover, recent spin-to-charge conversion experiments, performed both in $LaAlO_3/SrTiO_3$ heterostructures and at the reduced surface of $SrTiO_3$, evidence the potential of this interface for spintronics and topology studies [5–9]. Fundamental to several studies and applications is the capability to reduce the lateral dimension of the conducting channels.

Among the different methods used to nanostructure the 2DES, which include photolithography [10] and electron-beam lithography [11–13], the so-called atomic force microscope "(AFM)-writing" technique offers a versatile way to sketch conducting nanodevices in $LaAlO_3/SrTiO_3$ heterostructures [14,15]. It relies on the application of a positive voltage to the tip of an AFM, while scanning the $LaAlO_3$ surface to realize conducting patterns at the otherwise insulating interface between $SrTiO_3$ and 3 unit cells (u.c.s) of $LaAlO_3$.

These nanolithographic techniques give access to the study of interesting phenomena including universal conductance fluctuations [10,11], the Josephson effect in planar junctions [13,16–18], superconductivity in AFM-written nanowires [19], and conductance quantization in quantum-point contacts (QPCs) [20–24]. Among the different phenomena recorded in these nanodevices, there are a few effects that deserve further investigation, for instance: in AFM-written nanowires the presence of electron pairs without superconductivity has been suggested [25], and a surprisingly long ballistic length has been observed in the normal state of nanochannels [20,21]. Furthermore, the role of the lithography technique on the channel properties has to be clarified since nanowires realized via electron-beam lithography often display an insulating state at low temperature [12,26].

We report here on a comparative study of electric transport in (sub-)micrometric conducting channels realized at the $LaAlO_3/SrTiO_3$ interface using two methods: the AFM-writing technique and conventional photolithography. The lateral size of AFM-written wires ranges from 50 to 200 nm [27] and is comparable with the characteristic electronic length scales of the 2DES at low temperature. Indeed, the inelastic-scattering length is ~200 nm at 1 K [10,11], the elastic mean-free path ranges from 10 to 100 nm at 1.5 K [28], and the superconducting coherence length ranges from 10 to 70 nm [2,29]. The temperature behavior of the channel resistance displays a clear size dependence: wires narrower than ~100 nm have a crossover from a metallic to an insulating behavior at approximately 50 K, whereas wider wires stay metallic down to 1.5 K.

To shed light on this effect, we also investigate devices realized by conventional photolithography. These paths have a minimal width of ~1 μm, i.e., larger than those realized via AFM writing, but their conductance is more stable in time, and their properties have been extensively studied in the past. One of these devices is found to have a few ~50 nm-wide bottleneck constrictions giving rise to a crossover from a metallic to an insulating behavior at ~45 K, analogous to that observed in AFM-written wires. Moreover, at 50 mK, field effect experiments revealed that the electronic transport is characterized by conductance quantization through these constrictions.

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By comparing these experimental results with calculations for a QPC with a saddle-point potential, we show that the conductance quantization originates from the lateral confinement of the electrons at the interface; such lateral confinement can also explain the transport properties below 50 K. We conclude that constrictions acting as QPCs, similar to those reported in lithographic devices, could also be at the origin of the insulating behavior observed in AFM-written nanowires.

The paper is structured as follows: The experimental methods are described in Sec. II, and Sec. III presents the experimental results. Section IV describes the theoretical model developed to interpret the data, and finally we will discuss our findings in Sec. V.

II. EXPERIMENTAL DETAILS

The $LaAlO_3$ thin films have been grown by pulsed laser deposition (PLD) on commercial TiO_2-terminated $SrTiO_3$ substrates provided by Crystec GmbH using a laser fluence of 0.6 J/cm^2 and a repetition rate of 1 Hz. During the deposition, the substrates are kept at 800 °C in an O_2 pressure of 10^{-4} mbars. After the deposition, the samples are annealed *in situ* in an O_2 pressure of 200 mbars at 550 °C for 1 h and later cooled down to room temperature in the same atmosphere. The $LaAlO_3$ thickness, the control of which is crucial for the AFM-writing technique, is monitored *in situ* using the reflection high-energy electron diffraction technique. The quality of the samples realized with this procedure is well documented in a previous publication of our group [30].

After the growth, AFM-written channels are prepared (see for details Ref. [27]) at room temperature by scanning the AFM tip between conducting electrodes in contact with the interface. The channel width is controlled by the voltage applied to the AFM tip (5–9 V), by the number of consecutive scans, and estimated at room temperature using the so-called cutting method. They are typically 10-μm long and 50–200-nm wide. All the transport measurements are performed using a four-point configuration as shown in Fig. 1(a).

Devices realized with photolithography were prepared using the following procedure: First a layer of photoresist, lithographically patterned with the shape of the conducting device, covers a bare substrate, then amorphous $SrTiO_3$ is deposited by PLD at room temperature in an O_2 pressure of 10^{-4} mbars, finally the photoresist is removed to expose the selected areas of the substrate to the deposition of crystalline $LaAlO_3$ [11]. The structures realized with this technique are Hall bars ~1-μm wide and up to 300-μm long [see Fig. 1(d)]. Although their lateral size is, in general, larger than the characteristic electronic length scales of the 2DES, their length/width ratio is chosen to mimic that of AFM-written wires.

For field effect tuning, we sputter a few micrometers of gold on the backside of the $SrTiO_3$ substrate to create a gate electrode.

III. RESULTS

Figure 1 shows the temperature dependence of the sheet resistance of four devices fabricated using the AFM-writing technique (b) and (c) or patterns of amorphous $SrTiO_3$ (e) and (f). The behavior of the AFM-written wires depends on their channel width. Wires wider than ~100 nm have an overall metallic behavior [see panel 1(b)], whereas narrow channels have a crossover to an insulating behavior occurring at approximately 50 K [see panel 1(c)]. This transition can be suppressed (metallicity kept down to 1.5 K) by the application of a positive voltage to the backgate [see Fig. 1(c)]. All the devices realized with patterns of amorphous $SrTiO_3$ are metallic with a finite resistance at low temperature [see Fig. 1(e)], except for one: A device nominally 1.5-μm wide and 150-μm long has a crossover from a metallic to an insulating behavior at ~50 K. A positive gate voltage restores the metallicity [see Fig. 1(f)].

To understand this surprising behavior in a lithographically defined channel, similar to that of narrow AFM-written wires, we investigated the topography of this device and revealed the presence of two consecutive oval structures located close to one end of the path [see Fig. 2(a)]. These regions have exactly the same height as the regions covered by the amorphous $SrTiO_3$ used to prevent the formation of the 2DES at the interface [inset of Fig. 2(a)]. We believe that these islands are insulating regions, creating a series of conducting constrictions 0.5–1.5-μm long and from 50 to 500-nm wide in the otherwise wider conducting channel. The origin of these amorphous $SrTiO_3$ regions is probably due to our attempt to push the limits of the photolithography procedure to realize devices a few micrometers wide. Consequently, the photoresist did not develop well along the entire length of the channels, and some amorphous $SrTiO_3$ was deposited in regions that were supposed to be protected, giving rise to the islands observed in topography.

The 2DES conductivity in proximity to these features has been investigated using the scattering-type scanning near-field optical microscopy (s-SNOM) technique [31]. Figures 2(b) and 2(c) show two local maps, measured at 5 K, of the phase component of the s-SNOM signal. In the energy range probed here (laser wavelength of 10.7 μm), the phase component of the optical response is a reliable measure of the interface local conductivity [31]. This analysis shows that the conductivity of the constrictions cooled down with the gate grounded is much smaller than that of the larger area of the channel. Indeed, the s-SNOM phase difference between the center of the bottleneck and the insulating regions around the channel ~0.14 rad is low compared to the difference referred to the wide conducting channel ~0.32 rad. By increasing the backgate voltage to 5 V, the phase difference between the constrictions and the insulating regions increases to ~0.2 rad, (cf. intensity of the peaks in the horizontal cuts at the bottom of Fig. 2 at $V_g = 0$ and $V_g = 5$ V), whereas the same quantity estimated at the center of the large channel rises to ~0.38 rad, indicating that the constrictions become more metallic. These observations suggest that the insulating behavior of this device originates from the regions where the channel width is reduced.

Taking advantage of the nanosize channels created by the bottleneck structures of amorphous $SrTiO_3$, we measured the electronic transport below 1 K in a dilution cryostat. The sample was cooled down to 50 mK with 14 V applied to the backgate, and all the measurements were performed with a constant current of 8 nA applied between the drain and the

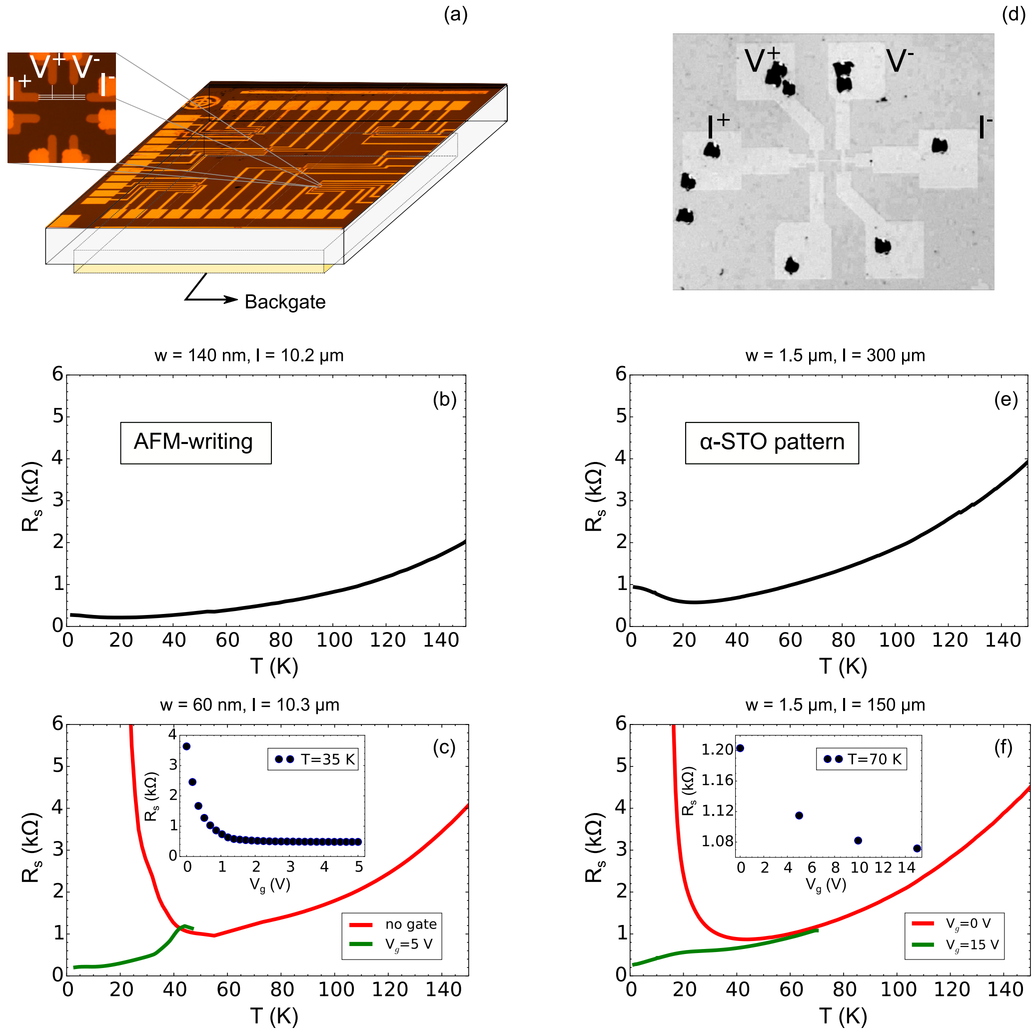

FIG. 1. (a) Sketch of an AFM-written device. A closeup of the writing area surrounded by metallic electrodes is shown in the inset. The sheet resistance as a function of temperature between 150 and 1.5 K for AFM-written wires of different widths is shown in panels (b) and (c). (b) Two parallel AFM-written wires 10.2-μm long, 140-nm wide, and 1 μm apart from each other. (c) Three parallel AFM-written wires 10.3 μm long, 60 nm wide, and 1 μm apart from each other with (green curve) and without (red curve) an applied gate voltage. The inset shows the evolution of the sheet resistance upon backgate voltage at 35 K. We note that the sheet resistance at 35 K and $V_g = 0$ is $\sim$4 kΩ, hence, higher than R_s at 35 K extracted from the red curve. This discrepancy is related to the thermal history of the device: First it was cooled down to 20 K (red curve) and then warmed up again to 35 K where R_s was found to be higher than at the beginning of the process. (d) Optical image of a Hall bar realized with a pattern of amorphous $SrTiO_3$. The channel is nominally 1.5-μm wide and 150-μm long. Panels (e) and (f) show the sheet resistance as a function of temperature between 150 and 1.5 K of two lithographically patterned devices with different sizes. (e) $R_s(T)$ of a channel 300-μm long and 1.5-μm wide. (f) $R_s(T)$ of a device 150-μm long, 1.5-μm wide, and containing some constrictions formed by insulating islands in the middle of the conducting region (see Fig. 2). The evolution of the sheet resistance as a function of the gate voltage at 70 K is shown in the inset.

source. We note that this sample does not display any sign of superconductivity in the setup used for the measurements. This may be related to the setup (i.e., lack of appropriate filters or very low critical current) or to an intrinsic reason such as doping, low transition temperature, or one-dimensional behavior. Figure 3(a) shows the resistance as a function of gate voltage at 50 mK while decreasing V_g from 17 to 13.6 V. The resistance increases from 38 to 340 kΩ and, between $V_g = 15$ and $V_g = 13.6$ V, it is characterized by some steplike features, which are not present in wider $LaAlO_3/SrTiO_3$ paths [3]. Such a large resistance increase (by one order of magnitude) upon a gate change of a few volts is due to the strong focusing of the electric field applied between the large gate electrode and the narrow (1.5-μm wide) channel [32]. We assume that the channel resistance results from the sum of two contributions. One comes from the resistance of the 1.5-μm wide and almost 150-μm long channel, and the other comes from the small constrictions in series with it. We attribute the continuous increase in the resistance to the charge depletion in the full channel and the steplike features to the constrictions. This behavior is reproducible upon several gate voltage sweeps and resembles that of the conductance of a QPC upon gate tuning [33]. For a more detailed analysis, we convert the resistance data in units of the quantum of

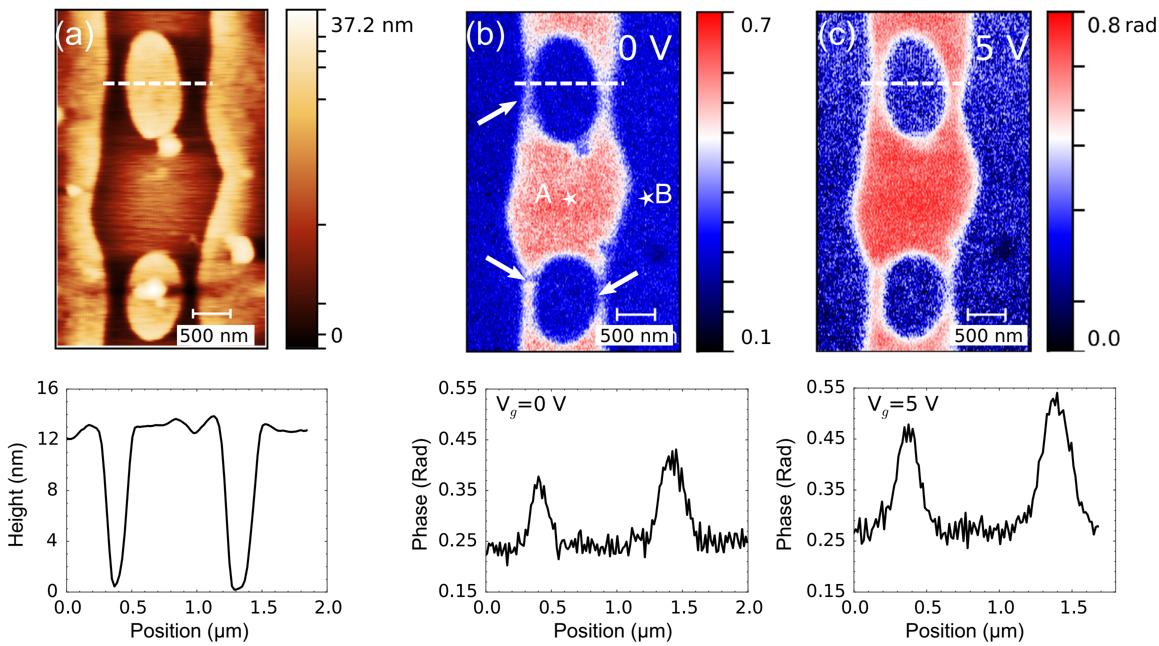

FIG. 2. (a) AFM topography of the conducting channel realized with a pattern of amorphous $SrTiO_3$ in correspondence to the constrictions. (b) Phase component of the near-field optical signal measured using a cryo-SNOM at 5 K with an incident light wavelength of 10.7 μm and the backgate grounded. The insulating regions at the center of the constrictions are labeled by white arrows. The symbols labeled A and B indicate the positions considered to evaluate the phase difference between the wide conducting channel and the insulating region. (c) Phase component of the near-field optical signal with 5 V applied to the backgate. The plots below panels (a)–(c) show a line cut of the topography and the phase component of the near-field signal at $V_g = 0$ and 5 V, respectively. The dashed white lines in the main figures indicate the position of the cuts.

conductance G $(2e^2/h)$ [see Fig. 3(b)]. G shows three steps approximately $0.02(2e^2/h)$ high and separated by roughly $\Delta V_g = 350$ mV. The height of the steps is much smaller than $2e^2/h$, and this discrepancy is attributed to the contribution of the full channel to the total conductance (the 1.5-μm wide and almost 150-μm-long conduction path in series with the constrictions). Therefore, a quantitative comparison with theory requires further analysis as presented in the next section.

Figure 4(a) shows the constriction conductance as a function of the gate voltage at different temperatures where four steps in $G(V_g)$ are visible. These datasets have been acquired a few days after the one shown in Fig. 3(b), and the measurements are characterized by lower noise levels and a slightly different step shape. The conductance steps survive up to 1 K, they are smeared out at higher temperature, and eventually vanish at 4 K. The suppression of the conductance quantization in temperature is expected for a QPC [34,35], but, interestingly, our device is particularly robust to the effect of temperature. The application of a magnetic field (oriented out of the interface plane) induces a similar effect: The conductance steps are smeared out at 8 T as shown in Fig. 4(b).

IV. NUMERICAL MODEL

We interpret the behavior of the structural constrictions below 1 K in the framework of the saddle-point model for

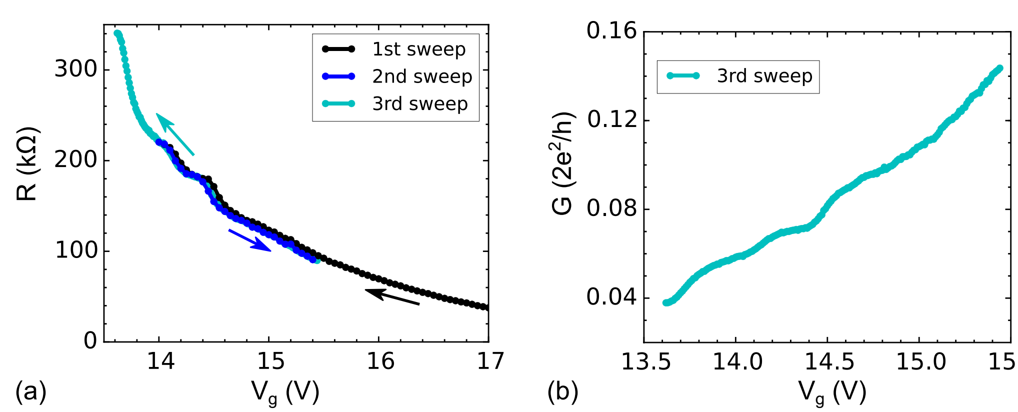

FIG. 3. (a) Backgate dependence of the total resistance at 50 mK for the device realized with a pattern of $SrTiO_3$. Three datasets have been acquired successively by sweeping the backgate voltage up and down (the arrows indicate the sweeping direction). (b) Gate dependence of the total conductance (for the third sweep only), normalized to the quantum of conductance $2e^2/h$.

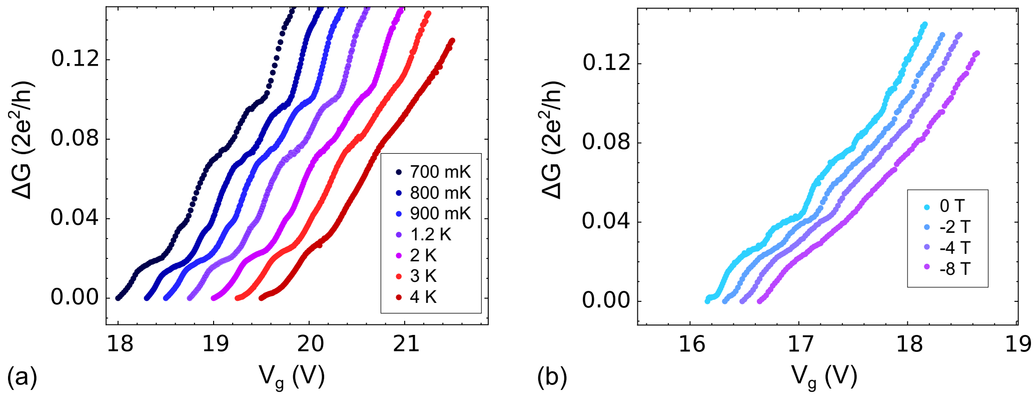

FIG. 4. Backgate dependence of the conductance increase $\Delta G = G(V_g) - G(V_g^{\mathrm{min}})$ normalized to $2e^2/h$ acquired at increasing temperatures (a) and increasing magnetic fields at 400 mK (b). The curves have been shifted along the x axis for clarity.

a QPC [36]. The confining potential used in this approach provides a good approximation of a bottleneck constriction as found in our lithographically patterned device [see Fig. 2(a)]. It is a smooth function of the interface plane coordinates x and y (x is the current direction and y is the transverse one), written as

$$V(x, y) = V_0 - \tfrac{1}{2}m\omega_x^2 x^2 + \tfrac{1}{2}m\omega_y^2 y^2, \qquad (1)$$

where V_0 is the electrostatic potential at the saddle point, ω_x and ω_y are two frequencies related to the size of the constriction, and m is the electron mass. $V(x, y)$ is the potential of a 2D harmonic oscillator along the y axis and a potential barrier with a parabolic shape along the x axis, and $\omega_{x,y}$ can be expressed in terms of length l_x and width l_y of the constriction: $\omega_{x,y} = \frac{\hbar}{m l_{x,y}^2}$. By solving the eigenvalue problem relative to Eq. (1), one can compute the total conductance at finite temperature of a QPC using the Landauer formula [37],

$$G = \frac{2e^2}{h} \sum_n \int d\epsilon \frac{\partial f_\mu(\epsilon)}{\partial \epsilon} t_n(\epsilon), \qquad (2)$$

where $f_\mu(\epsilon) = (e^{\beta(\epsilon-\mu)} + 1)^{-1}$ is the Fermi distribution in the reservoirs, $t_n(\epsilon)$ is the transmission coefficient of the nth channel at energy ϵ (one should note that channel intermixing does not occur in this case as the confining potential is quadratic), μ is the chemical potential, and $\beta = 1/k_B T$.

We model the experimental behavior of our device by making the assumption that the conductance jumps visible in Fig. 3(b) originate from a single constriction. Equation (2) has been computed numerically by fixing a finite number of channels entering in the sum,[1] using an electron effective mass of $2.2m$ [38], and setting the chemical potential μ to zero. The position of μ is arbitrary as it is compensated by the value of the electrostatic potential V_0. We set the values of l_y and l_x to 35 and 350 nm, respectively. Despite the lack of a precise control over the geometry of our device, these values are compatible with the s-SNOM and topographic images shown in Fig. 2. The V_0 dependence of the calculated conductance at 50 mK is shown in Fig. 5. The energy difference ΔV_0 between the conductance plateaus reflects the energy spacing between the transverse states $\hbar\omega_y \propto l_y^{-2}$, the sharpness of the steps is controlled by the temperature and $\hbar\omega_x \propto l_x^{-2}$, and their height corresponds to a quantum of conductance $2e^2/h$.

Considering the complex geometry of our device [see Fig. 2(a)], extracting a precise value for the conductance jumps from the experimental data is challenging as we need to estimate and remove the contribution of the full channel (the long conducting path in series with the constriction) from the total conductance [Fig. 3(b)]. A quite good approximation is provided by the following method. First, we compute the resistance of the constriction R_{QPC} by subtracting from the total

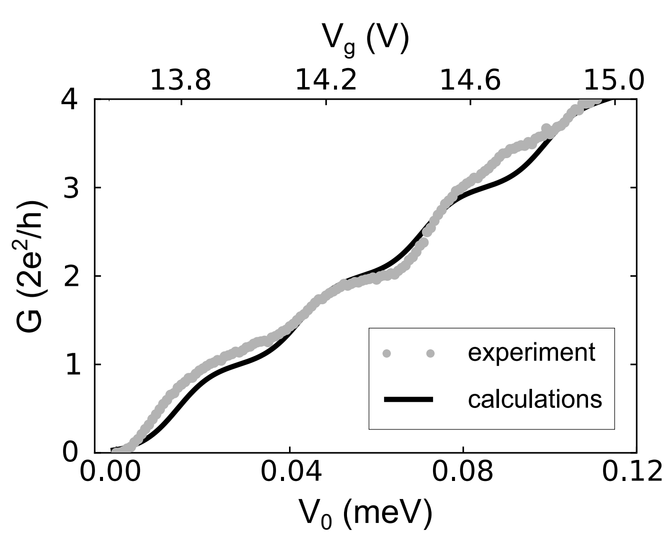

FIG. 5. Calculated and experimental values of the conductance of the QPC (in units of $2e^2/h$) as a function of V_0 at 50 mK. The numerical calculations were carried out using the saddle-point model for a QPC with $l_x = 350$ and $l_y = 35$ nm. The experimental conductance has been analyzed as explained in the main text. The gate voltage applied to the device is reported on the top abscissa axis for comparison.

[1]We fixed the number of channels to 100. This value is large enough to describe the conductance steps observed experimentally [Fig. 3(b)], involving the conduction channels at low energy. Considering a larger number of channels would imply making strong assumptions on the high-energy structure of the constriction, which clearly goes beyond the regime of validity of our simple description.

resistance the component of the full channel (the reservoirs), computed by rescaling the total resistance to the reservoir length l_{channel}, i.e.,

$$R_{\mathrm{QPC}} = R_{\mathrm{tot}}(1 - l_{\mathrm{channel}}/l_{\mathrm{tot}}), \tag{3}$$

where R_{tot} is the total resistance of the device and l_{tot} is the total length of the channel (full path and constriction region). We fixed l_{channel} and l_{tot} to 147.5 and 150 μm, respectively. The value of l_{tot} is the nominal length of the pattern of our device, whereas l_{channel} was chosen under the assumption that the insulating islands occupy approximately 2.5 μm of the total channel length. Finally, from R_{QPC}, we computed the conductance of the constriction, obtaining a value that matches steps of magnitude $2e^2/h$.

In order to compare the experimental data with the calculations we need to estimate the scaling factor between the backgate V_g and the electrostatic potential V_0. Indeed, these two quantities are not equivalent: whereas V_g is the voltage applied to the backelectrode, V_0 is the electrostatic potential related to the gate-induced Fermi energy shift. In order to convert the gate voltage into the electrostatic potential at the interface, we analyzed the effect of ΔV_0 on a simple parabolic conduction band with an electron effective mass of $2.2m$ [38]. For a variation $\Delta V_0 = 0.12$ meV we computed a carrier density variation $\Delta n_{2\mathrm{D}}$ of 1.1×10^{11} cm^{-2}. Since such $\Delta n_{2\mathrm{D}}$ is obtained in our devices by ΔV_g of ~ 1.4 V [39],[2] we estimate a scaling factor $\Delta V_g/\Delta V_0$ of 1.2×10^4. As a result of this analysis, we find good agreement between the experimental and the calculated curves (cf. Fig. 5). We note that the deviations of the experimental points from the calculated curves might have multiple origins. First of all, the real geometry of the constriction might deviate from the perfectly parabolic model in Eq. (1), and an anharmonic potential would account for changes in the form of the steps when the voltage is increased. Second, there might be spurious effects stemming from other constrictions present in our device (see Fig. 2).

If we extend our model to higher temperatures, we find that the calculated conductance steps are smeared out at 100 mK. Experimentally, the quantization seems to persist up to 1 K as visible in Fig. 4(a). This could be due to a larger energy separation $\hbar\omega_y$ between the conductance levels due to a smaller channel size. For example, if we consider a QPC with $l_x = 8$ and $l_y = 6$ nm, we find conductance steps similar to the experimental ones at 50 mK that remain essentially unchanged up to 1 K. Therefore, the real dimension of the constriction giving rise to this effect remains elusive.

Although the QPC model ultimately gives reason for the insulating behavior observed in Fig. 1(f), it cannot reproduce the complete behavior of the resistance in temperature since it completely neglects a plethora of phenomena occurring at higher temperatures, such as electron-phonon and electron-electron interaction, that are expected to be the dominant contributions to the resistance in this temperature range.

[2]We note that this value has been extracted from analysis performed on wider devices (later size above 100 μm), nevertheless the field focusing occurring in narrow ones enables the same $\Delta n_{2\mathrm{D}}$ to be achieved using a lower backgate voltage [32].

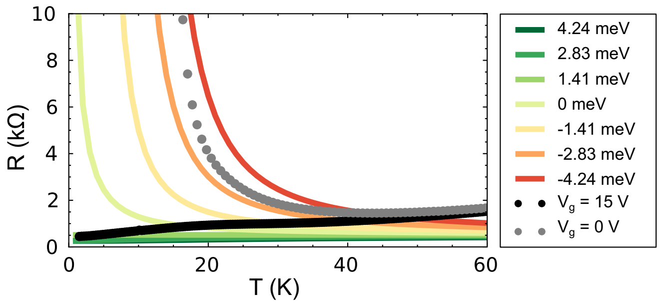

FIG. 6. Calculated (solid lines) and experimental values (points) of the constriction resistance as a function of temperature. The calculations have been performed using the model and the parameters detailed in Sec. IV with $l_x = 350$ nm and $l_y = 35$ nm. The values of the electrostatic potential V_0 used in the calculations are reported in the legend.

V. DISCUSSION

The analysis presented in the previous section shows that the conductance jumps observed in our device as a function of the backgate result from the quantization of the transverse electronic states in a QPC. We also followed experimentally the evolution of these plateaus in temperature and magnetic field. Although the temperature dependence of the conductance quantization corresponds to what is expected for a QPC [34,35], the behavior in the magnetic field is less trivial to understand. The saddle-point model predicts a modification of the plateaus when a magnetic field is applied to the system as a result of the interplay between the quantization of the energy levels induced by the confinement $\omega_{x,y}$ and by the magnetic field ($\omega_c = |eB|/m$, where e is the electron charge, m is its mass, and B is the magnetic field) [36]. The inclusion of orbital effects in our model would lead to sharper conductance steps as the magnetic field is increased [36].

In our experiments, by increasing the field to 8 T, we observe an opposite effect since the magnetic field suppresses the conductance plateaus [see Fig. 4(b)].

A recent report by Jouan *et al.* [23] on transport measurements in the magnetic field, realized in a gate-controlled QPC at the $LaAlO_3/SrTiO_3$ interface, revealed the emergence of half-integer quantum conductance steps $0.5(2e^2/h)$ at 6 T. They attribute this effect to the Zeeman splitting of the spin-degenerate QPC levels. In our system we could not observe the emergence of such additional steps. The behavior of our device might originate from additional effects of the magnetic field on the electronic reservoirs, characterized by the interplay among spin-orbit coupling, Zeeman splitting, and lateral confinement provided by the lithographically defined channel, whose description goes well beyond the simplistic saddle-point model for the QPC.

The presence of quantum tunneling barriers in conducting channels is a good candidate to explain the crossover between metallic and insulating behavior observed in our devices. In order to analyze this scenario, we used the model presented in Sec. IV to compute the temperature behavior of the QPC resistance for different values of the electrostatic potential (see Fig. 6). Despite the limit of this calculation that neglects any effect occurring at high temperature, such as electron-phonon and electron-electron coupling, we observe that, for $V_0 \leqslant 0$, the resistance of the system diverges below $\sim$30 K (Fig. 6). The metallic behavior is restored only at positive values of the electrostatic potential, similar to what we observed experimentally (see for comparison the experimental points in Fig. 6).

As discussed in the experimental section, Fig. 1 shows that AFM-written wires become insulating at temperatures that are comparable to the ones observed in the device patterned with amorphous $SrTiO_3$ ($\sim$40 K). One may argue that this analogy is due to the presence of local constrictions in these electrically defined channels whose precise charge profile remains unknown. It is worth noting that, in this case, other phenomena could be equally responsible for the insulating behavior at low temperatures: The presence of multiple constrictions could act as an effective disordered potential leading to Anderson localization [40–42], a phenomenon which is robust to the presence of repulsive Coulomb interactions among electrons [43]. Alternatively, the formation of consecutive barriers could lead to the formation of well-isolated charge puddles acting as quantum dots responsible for Coulomb blockade effects [44]. Further efforts in controlling the shape of thin and homogeneous wires would be important to clarify this issue.

In conclusion, this paper, aiming at exploring the electric transport properties of nanoscale devices realized at the $LaAlO_3/SrTiO_3$ interface, shows that the lateral size of a conducting path has a striking effect on the resistance behavior as a function of temperature. Studying devices realized using the AFM-writing technique or with conventional photolithography, both with a lateral confinement of the 2DES lower than $\sim$100 nm, we witnessed a crossover from a metallic to an insulating behavior at $\sim$50 K. The comparison between experiments and model calculations reveals that this behavior could be understood by considering the presence of tunnel barriers acting as QPCs along the conducting path. These findings will be useful for the interpretation of past and future experiments performed on such oxide 2D nanoscale devices, and it will be of high interest to study the confinement effects in future devices where superconductivity is present.

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