Analysis of the thermally stimulated capacitor-discharge method for characterizing localized states in amorphous semiconductors*†

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A detailed analysis of the method of thermally stimulated capacitor discharge (TSCD) is presented. Distinction is made between the dielectric relaxation currents and the trap-limited currents. The position, shape, and number of the depolarization peaks caused by the dielectric relaxation currents are shown to depend (i) on the conductivity of the sample as a function of temperature and electric field and (ii) on the geometry of the sample. It is pointed out that the behavior of the dielectric-relaxation-current peaks is quite similar to the trap-limited-current peaks, and an analysis of the peaks may lead to false conclusions, if done without distinguishing them from one another. We assert that no new information about the trap parameters can be obtained from TSCD, unless the structure of the polarization and depolarization curves are different. No such difference was found in the chalcogenide glass studied by us, and the observed TSCD could be explained in terms of dielectric relaxation currents only. We also point out that a low drift mobility, a short screening length, and possibly a large density of localized states near the Fermi level, make the observation of trap-limited TSCD in multicomponent chalcogenides unlikely.

I. INTRODUCTION

The understanding of many physical properties of amorphous semiconductors requires the knowledge of the distribution and capture cross section of localized states within the mobility gap of the particular material. The method of thermally stimulated capacitor depolarization (TSCD) has been widely used for investigating trapping levels in crystalline as well as amorphous semiconductors.[1-20] Experimentally, the TSCD method consists of first filling the traps at some high temperature T_1 (usually chosen to be room temperature) by the application of an electric field to the semiconductor. The sample is then cooled down to a temperature T_0 with the field applied. The field is then removed, and upon heating, the trapped charges are liberated, giving rise to a current called the thermally stimulated capacitor discharge or depolarization current. This is similar to the method of thermally stimulated currents (TSC).[21] Here a nonequilibrium carrier distribution is produced by light, frozen in by cooling, and its relaxation to equilibrium observed by the excess current which flows as a result of a small field applied as the sample is heated at a constant rate. Thus, in order to analyze the TSCD curves, one uses the techniques and formulas[21] similar to the ones used to analyze the TSC curves. The TSCD method is considered to be a more convenient tool in cases where the dark current is of the same magnitude or larger than the TSC excess current which is to be measured. A disadvantage of the TSCD method may be the fact that one does not probe the bulk of the sample but rather a contact or interface region. In the case of amorphous semiconductors, where the dark current is usually quite large, the TSCD method is particularly recommended.[8]

The depolarization current observed in a TSCD experiment consists of two parts: (i) the dielectric relaxation current and (ii) a trap-limited current due to carriers excited into the conduction (or valence) band as the carrier distribution returns to equilibrium as the sample is heated. The dielectric relaxation currents simply depend on the variation of conductivity σ of the material with temperature, and does not yield new information if $\sigma(T)$ is known. Thus, in order to learn something new about the trap parameters, one has to extract the trap-limited current (ii) from the total TSCD current by subtracting the relaxation current (i).

It is evident that the TSCD method will be most efficient, when one of the contacts to the semiconductor is blocking and the other ohmic. In the case of amorphous semiconductors, however, it is difficult to make a truly blocking contact because the resistance of the metal-semiconductor contact, for most metals, is rarely found to be much larger than the bulk resistance of the semiconductor film.[22] Using an insulator as a barrier between the semiconductor and one of the electrodes we obtained TSCD curves on a typical chalcogenide glass. These were found to contain one or more peaks, whose positions and strengths depended on the sizes and the relative geometrical arrangement of the electrodes with respect to one another. All the structure in the TSCD could be explained in terms of dielectric relaxation currents.[23]

The TSCD structures observed by us are quite similar to the ones obtained by the other authors.

These authors, however, make no attempt to distinguish their results from dielectric relaxation. In Sec. II we show that the sample geometry plays an important role, and that the structure of the TSCD curves and peak positions change upon changing the geometrical arrangement of the contacting electrode with respect to the blocking electrode. In Sec. I we show that for most of the common geometries one expects to see two peaks, and depending on the geometry employed one may see some extra structure in the form of shoulders near the peak. These may easily be misinterpreted as representing trap centers. Further, our calculations show that under certain conditions the initial rise of the TSCD current resulting from the dielectric relaxation plotted as $1/T$ may yield a slope smaller than the activation energy of the semiconductor, and may easily mislead one into taking this to be a proof of the existence of traps at that depth. We also suggest in Sec. I an easy experimental method for determining *a priori* whether a given TSCD curve contains any trap-limited currents. If it does, the polarization and depolarization curves must differ.

Section III discusses our experimental results for different electrode geometries. We show that our TSCD curves can be explained, provided the field dependence is included in the conductivity. In Sec. IV we analyze previously published results in the light of these arguments, summarize our findings, and discuss the conditions necessary to observe trap limited TSCD currents.

II. TSCD METHOD AND ANALYSIS

A. Depolarization experiment

For the TSCD experiment, the samples are prepared in the form of a metal-insulator-semiconductor-metal (MISM) arrangement or MSM arrangement with one of the metal-semiconductor contacts blocking. A voltage V_d is applied to the device at "high" temperature[24] (T_1) by connecting terminals 1 and 2 in Fig. 1. The sample is then cooled to a "low" temperature (T_0) in this condition. This charges up the capacitor formed by the semiconductor insulator and lower electrode to the potential V_d. At T_0 the terminals 1 and 3 are connected and the depolarization current is measured as the temperature is increased at a constant rate. This current may arise (i) from the discharge of the capacitor through the temperature and field-dependent resistance of the semiconductor (i.e., dielectric relaxation), or (ii) from the liberation of electrons out of trap levels (i.e., trap limited), or both.

The analysis of the trap-limited TSCD currents has been described quite extensively in the literature[1–20] and therefore will not be presented here. The dielectric relaxation currents, on the other hand, have not been discussed previously because they do not give any more information than the conductivity as a function of temperature for low and high fields. It is, however, important to distinguish the dielectric relaxation currents from the trap-limited TSCD currents in order to interpret the results correctly. We have found that the structure in the dielectric relaxation curves depends crucially on the geometry of the sample. In the following we shall discuss dielectric relaxation currents for several electrode geometries.

Although many different and complicated geometries are possible, they can basically be divided into three categories for our purpose. These are shown in Fig. 2. Let us assume that the temperature-dependent conductivity of the semiconductor $\sigma(T)$ follows the common form

$$\sigma(T) = \sigma_0 e^{-E/kT} , \tag{1}$$

where E is the activation energy.

a. Case I: Geometry (a). The equivalent circuit of the semiconductor is a capacitor C_s in parallel with a resistor, whose resistance $R(T)$ depends on T in accordance with Eq. (1). The insulator in Fig. 2(a) is represented by a capacitor C_I in series with the semiconductor. Upon applying the voltage V_d at $T = T_1$, the capacitor C_I gets charged, whereas C_s remains uncharged. Upon cooling to T_0 the value of $R(T)$ increases, but C_s continues to be uncharged. At T_0 terminals 1 and 3 are connected (see Fig. 1) and the charge on C_I gets distributed between C_s and C_I in proportion to their magnitudes. With a constant heating rate β, the relaxation current measured is given by (see Appendix A)

$$I(T) = \frac{C_I^2 V_d}{C^2 R_0} \exp\left[-x + \frac{E}{k\beta C R_0} \times \left(\frac{e^{-x_0}}{x_0} - \frac{e^{-x}}{x} + \int_x^{x_0} \frac{e^{-x}}{x} dx\right)\right], \tag{2}$$

where

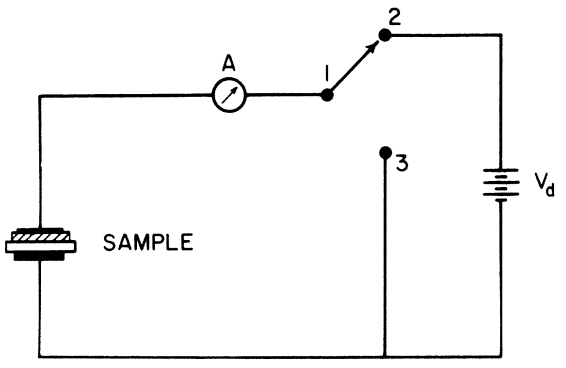

FIG. 1. Circuit for measuring TSCD.

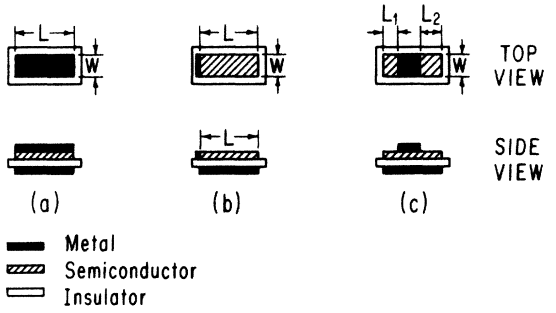

FIG. 2. Three electrode geometries for MISM samples.

$$C = C_s + C_I\,, \quad x = E/kT\,, \quad x_0 = E/kT_0\,,$$

and R_0 is related to σ_0 of Eq. (1) by the geometry factors,

$$R_0 = t_s/\sigma_0 WL\,.$$

W and L are defined in Fig. 2(a) and t_s is the thickness of the semiconductor. The maximum in $I(T)$ occurs at $T = T^*$, which is determined by

$$(E/k\beta CR_0)e^{-E/kT^*} = (E/kT^*)^2\,. \tag{3}$$

The graphical solution to the transcendental Eq. (3) is shown in Fig. 3 for different values of the coefficient

$$\alpha \equiv E/k\beta CR_0\,.$$

The integral in Eq. (2) can be evaluated numerically, and I can then be obtained as a function of temperature. The numerical results are shown in Figs. 4 and 5. We see that the peak is sharper and at lower temperatures for smaller values of E. Figure 5 shows that an increase in β causes an increase in peak height and a shift to higher temperatures. This behavior of the dielectric relaxation current is similar to the trap-limited current. Therefore on the basis of this behavior alone it is difficult to distinguish the two currents which have very different origins.

b. Case II: Geometry (b). At temperature T_1 the semiconductor is quite conducting. Therefore, when V_d is applied at T_1 the whole area of the semiconductor acts like the upper electrode, and the capacitor C_1 formed by the semiconductor-insulator-metal structure charges. As the sample is cooled, the semiconductor becomes highly resistive, [see Fig. 2(b)] and the upper electrode effectively shrinks back to the size of the metal electrode. As shown in Appendix B, the dielectric relaxation current, in this case, is given by

$$I(T) = \left(\frac{2V_d}{Lr_0}\right)e^{-E/kT}\sum_{n=0}^{\infty}\exp\left(-\frac{(2n+1)^2\pi^2}{4\beta r_0 C_I L^2}\int_0^T dT\, e^{-E/kT}\right), \tag{4}$$

with

$$r_0 = 1/(\sigma_0 W t_s)\,,$$

where L and W are defined in Fig. 2(b). The condition for maximum can be found by setting $dI/dT|_{T=T^*} = 0$. Keeping only the first term ($n = 0$) in the summation in Eq. (4), the condition can be written

$$(\pi^2 E/4\beta r_0 C_I Lk)\, e^{-E/kT^*} = (E/kT^*)^2\,. \tag{5}$$

This is justified because near the maximum, the value of the integral in the exponent is large, and only one term is needed to yield a fairly accurate value of the current at the maximum. Equation (5) can be solved graphically, again by using Fig. 3, but with α determined by

$$\alpha \equiv \pi^2 E/4\beta r_0 C_I Lk\,.$$

The solutions to Eq. (4) are shown in Figs. 6, 7 and 8 for different values of E, β, and L, respectively. It is clear that large values of E and L result in a larger and broader peak at higher temperatures.

c. Case III: Geometry (c). This is clearly a superposition of Cases I and II [see Fig. 2(c)] and the total TSCD current is given by the sum of Eqs. (2) and (4). It is obvious that this will result in two peaks provided either the upper electrode is symmetrical with respect to the semiconductor, i.e., $L_1 = L_2$, or is touching the edge of the semiconductor on one side, i.e., $L_1 = 0$. In case $L_1 \neq L_2$ one may see an additional shoulder on the dielectric relaxation curve.

The height of the peak in Case I is proportional to the square of the ratio of capacitances C_I and C,

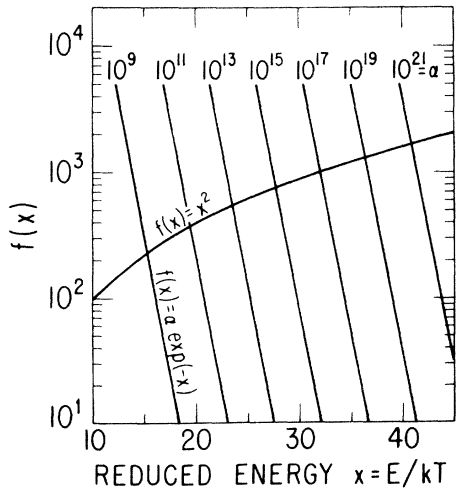

FIG. 3. Graphical solution to Eqs. (3) and (5) of text to determine the position of the dielectric-relaxation-current maximum. The parameter α defined in text depends on the sample geometry.

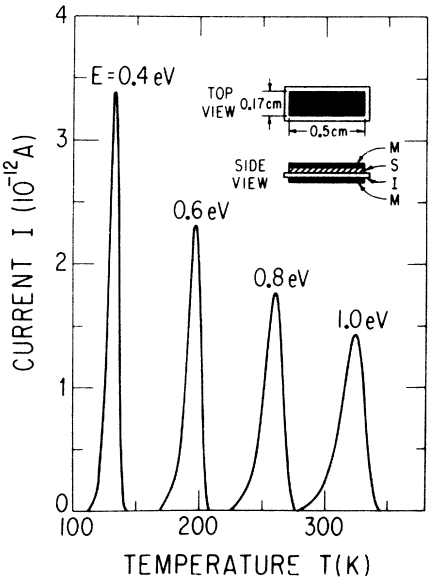

FIG. 4. Calculated dielectric relaxation currents for sample geometry (*a*) for different values of activation energy E. Other parameters are $\sigma_0 = 10^2$ $(\Omega\ \text{cm})^{-1}$, $V_d = 1$ V, $t_S = 0.5$ μm, and $t_I = 1$ μm, $\beta = 0.15$ K/sec.

whereas in Case II it is independent of this ratio. Therefore, the ratio t_s/t_I determines whether or not both the peaks are observable. Figures 9 and 10 illustrate this point, where we have plotted the calculated dielectric relaxation current for a sample with $L_1 = L_2 = 0.5$ cm and $W = 0.15$ cm. The other parameters chosen in this calculation are $E = 0.5$ eV, $\beta = 0.15$ K/sec, $V_d = 150$ V, and $\sigma_0 = 9.2 \times 10^2$ $(\Omega\ \text{cm})^{-1}$.

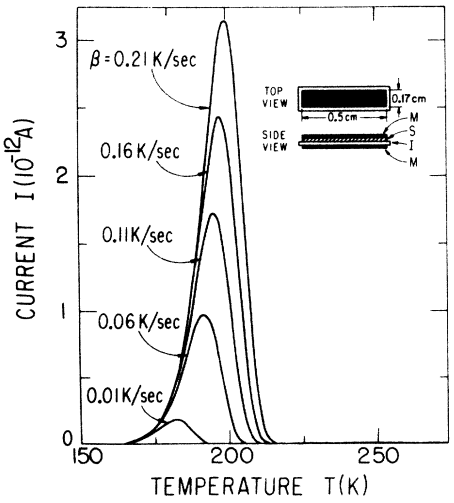

FIG. 5. Calculated dielectric relaxation currents for sample geometry (*a*) for different heating rates β. Activation energy was chosen to be $E = 0.6$ eV. Other parameters are the same as in Fig. 4.

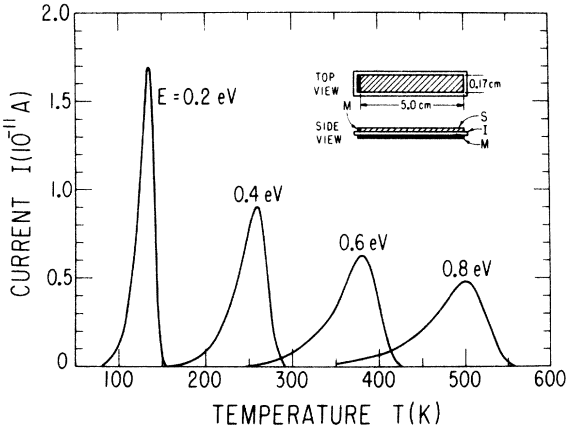

FIG. 6. Calculated dielectric relaxation currents for sample geometry (*b*), for different values of activation energy E. Other parameters are the same as in Fig. 4.

The insulator thickness t_I was varied from 1 to 10^3 μm, whereas the semiconductor thickness was kept constant at $t_s = 1$ μm. The total TSCD current resulting from such a geometry is obtained by adding the two peaks for the appropriate set of parameters. At $t_I \leq 10$ μm we see two peaks, but with $t_I > 10$ μm the lower temperature peak is too small to be observed.

Figure 11 shows the effect of changing the semiconductor thickness t_s and Fig. 12 illustrates the behavior of the two peaks as σ_0 is varied.

It is evident that the position, size, shape, and even the number of peaks depend strongly on the geometry of the sample. It is important to note that these relaxation-current peaks can easily be mistaken for trap-limited currents if only one geometry is studied with different heating rates. Thus, the usual methods[25] of obtaining trap depth by using the positions of TSCD peaks and their half-widths may lead to erroneous conclusions if applied to the TSCD curves without ascertaining their origin.

In order to evaluate data published previously in

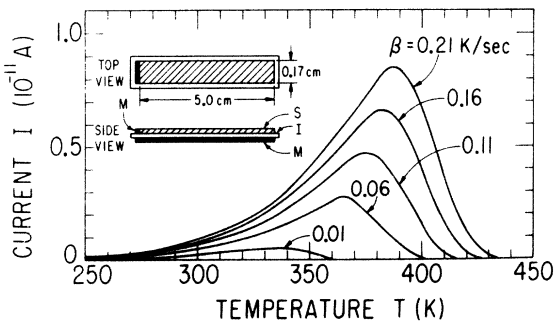

FIG. 7. Calculated dielectric relaxation currents for sample geometry (*b*) for different heating rates β. $E = 0.6$ eV. Other parameters are the same as in Fig. 4.

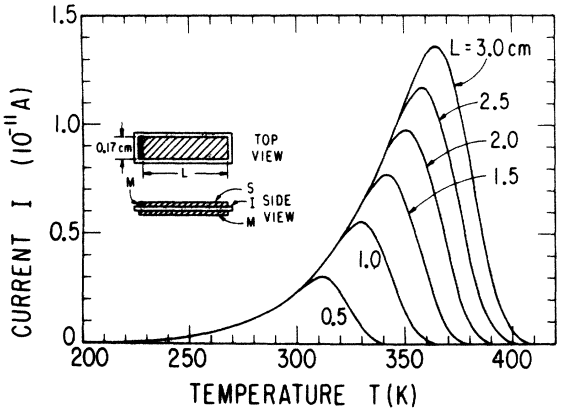

FIG. 8. Calculated dielectric relaxation currents for sample geometry (*b*) for different lengths of the edge L of the semiconductor. Other parameters are $E = 0.6$ eV, $\sigma_0 = 10^2$ $(\Omega\text{cm})^{-1}$, $V_d = 3$ V, $t_S = 0.5$ μm, $t_I = 1$ μm, and $\beta = 0.15$ K/sec.

this field it is interesting to apply the commonly used TSCD analysis to the relaxation currents calculated in Sec. II. The trapping parameter thus obtained will, of course, have no physical meaning since the relaxation currents are determined by Eq. (1).

A technique commonly known as the initial-rise

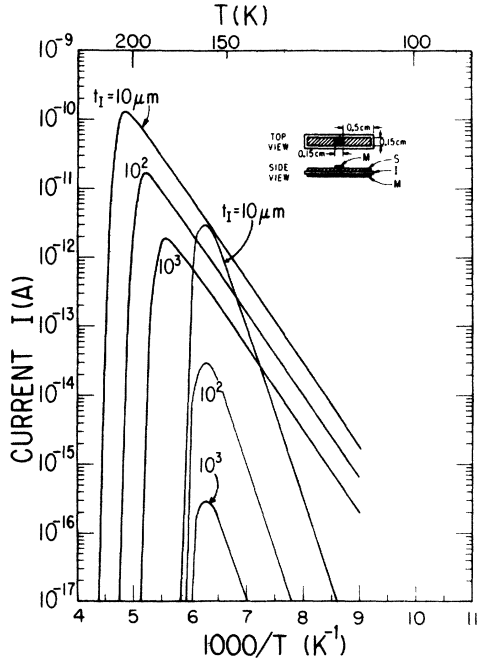

FIG. 9. Calculated dielectric relaxation currents for sample geometry (*c*) for various insulator thicknesses t_I. Net current is obtained by adding the two peaks for a given t_I. Other parameters chosen were $E = 0.5$ eV, $\sigma_0 = 9.2 \times 10^2$ $(\Omega\text{cm})^{-1}$, $V_d = 150$ V, $t_S = 1$ μm, and $\beta = 0.15$ K/sec.

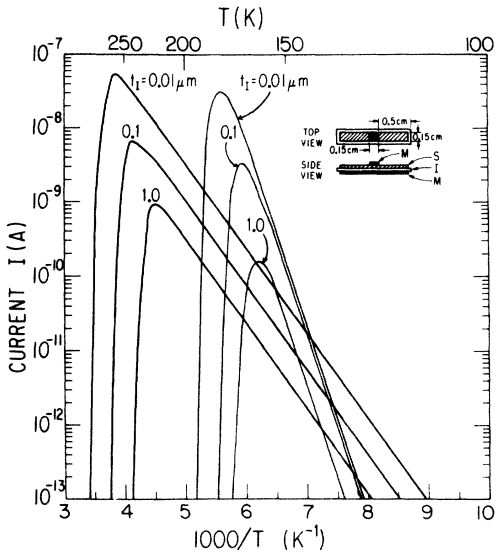

FIG. 10. Same as Fig. 9 for larger insulator thicknesses $t_I > 10$ μm, only the high-temperature peak can be observed.

method or the leading-edge analysis is frequently used in the case of trap-limited TSCD currents to obtain the trap depth.[21] In this method the slope of initial rise of TSCD plotted logarithmically against $1/T$ yields the trap depth. The main advantage of obtaining trap depth by this procedure, advocated initially by Garlick and Gibson[26] for glow curves, is that the procedure does not require the

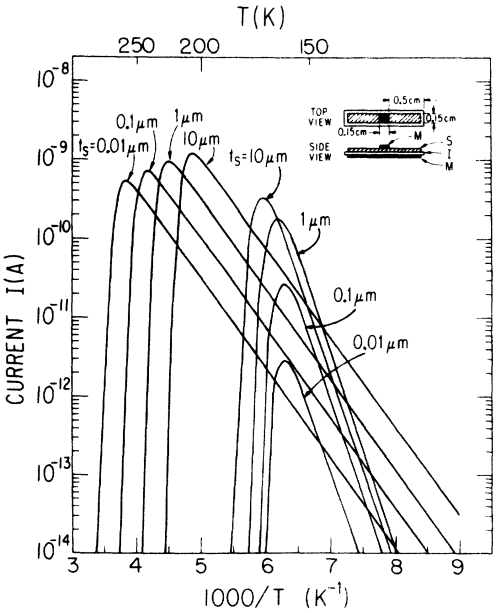

FIG. 11. Calculated dielectric relaxation currents for sample geometry (*c*) for various semiconductor thicknesses t_S; $t_I = 1$ μm. Other parameters are the same as Fig. 9.

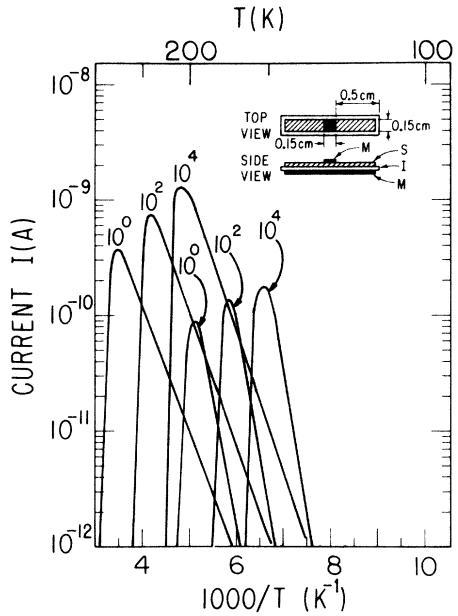

FIG. 12. Calculated dielectric relaxation currents for sample geometry (*c*) for various values of σ_0. $t_I = 1\ \mu$m. Other parameters are the same as Fig. 9.

knowledge of the recombination kinetics. If one plots such a graph for the dielectric relaxation currents, one would obtain a slope which is equal to the activation energy E for geometry (*a*) and smaller than E for geometry (*b*). For geometry (*c*) the low temperature slope depends on the electrode geometry because the current is a geometry-dependent superposition of two parts (as explained above). This leads one to the false conclusion that there are traps at a depth which corresponds to the initial-rise slope.

Another technique used to analyze trap-limited TSCD involves plotting $\ln(T^{*2}/\beta)$ as a function of $1/T^*$. The slope of the straight line thus obtained is interpreted as the trap depth.[21] It is clear, however, from Eqs. (3) and (5), that in the case of dielectric relaxation currents, such a plot would also yield a straight line. The magnitude of the slope is E. Thus the result of this analysis seems to verify within errors the "trap depth" obtained by the initial-rise method, but the interpretation is, of course, erroneous.

So, for the same reasons, another method called step heating,[21] which consists of annealing the sample to successively higher temperatures to obtain the trap depth of successively deeper traps by the initial-rise method, may be applied in the case of TSCD only after making sure that the observed TSCD are indeed trap limited.

B. Polarization experiment

One way of ascertaining the origin of the TSCD current as relaxation currents is to perform the calculation for the given geometry and $\sigma(T)$. A much faster method is, however, to measure both the polarization and depolarization current. The polarization current is obtained by cooling the sample with terminals 1 and 3 connected (see Fig. 1), and measuring the current while heating with V_d applied. If the polarization and depolarization currents are identical and opposite in sign, then one is dealing only with the dielectric relaxation currents.

III. EXPERIMENTAL RESULTS

A chalcogenide alloy of composition $Ge_{16}As_{35}Te_{28}S_{21}$ was chosen for the TSCD experiments. Thin films of this material were prepared by rf sputtering in an argon atmosphere onto glass, mica, or quartz substrates. The film thicknesses ranged from 1 to 5 μm, and the insulator thicknesses from 0.1 to 10^{-3} cm. Gold evaporated in a vacuum of better than 10^{-6} Torr was used as the electrode material to obtain a MISM structure. In order to correctly measure the temperature of the sample during heating, we replaced it with another test sample with MSM structure and measured its conductivity at various fixed temperatures. These values were then matched with the corresponding temperatures obtained on the temperature ramp by suitably adjusting the position of the thermocouple. This enabled us to read the temperature of the sample to within one degree while it was being heated. In our experiment, T_0 was chosen to be 77 K and T_1 was 300 K.

The solid curve in Fig. 14 shows the TSCD obtained with a sample having the electrode geometry of Fig. 2(b). The substrate used was a 1 in. $\times \frac{1}{2}$ in. 7059 Corning glass slide of thickness 0.13 cm. The thickness of the semiconductor was 1.2 μm. The heat rate used was $\beta = 0.15$ K/sec, and the activation energy measured by another experiment was found to be $E = 0.6$ eV. The area of the semiconductor was 1.8 cm $\times$ 0.3 cm. The relaxation current calculated from Eq. (4) using these values is shown by the dashed curve in Fig. 13. The fit is quite good. The peak height was found to scale linearly with the polarization voltage V_d in the range tested [with V_d(maximum) = 1.5 kV], and the measured current was identical with the opposite sign upon reversing V_d. In some cases a voltage V_i was applied during heating. $V_i = -V_d$ resulted in doubling the height of the peak and $V_i = V_d$ gave zero TSCD current as required by the dielectric relaxation model described above. Further, the polarization and depolarization curves were found to be identical in structure (and opposite in sign), which is an experimental proof that the phenomena observed are indeed dielectric-relaxation limited rather than trap limited.

Next, we performed the following experiment,

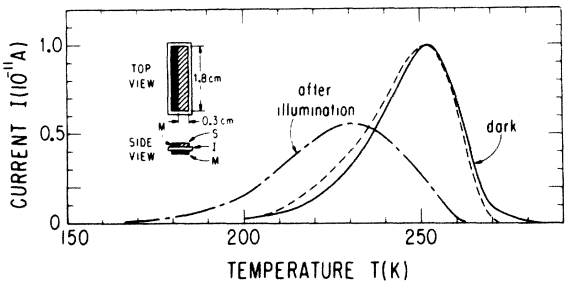

FIG. 13. Experimental TSCD obtained for a sample with geometry (*b*). The dashed curve is the dielectric relaxation current calculated by using the known sample parameters. The dotted dashed curve is the result of the depolarization experiment using light as well as electric field.

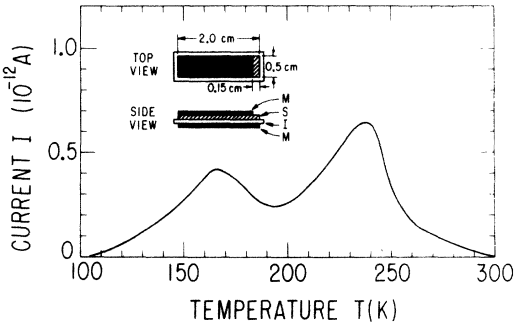

FIG. 15. Experimental TSCD obtained for the chalcogenide alloy of Figs. 13 and 14, but with geometry (*c*).

which is referred to in the literature as depolarization of the photoelectric state.[9-16] The sample was illuminated with white light from a 75 W tungsten halogen lamp and the voltage V_d was applied. The sample was then cooled to 77 K. The light was switched off and V_d removed at 77 K. The sample was then heated. The resulting depolarization curve is shown as the dotted-dashed line in Fig. 13. This curve is different from that obtained in the dark and one might argue that this may yield some information about trap parameters. However, a polarization experiment, (i.e., cooling the sample with $V_d = 0$ under illumination and then at 77 K applying the voltage V_d in the dark and measuring the charging current as the sample is heated) yielded an equal and opposite curve which indicates

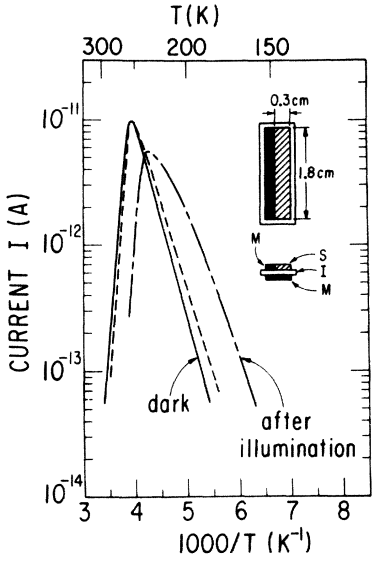

FIG. 14. Curves of Fig. 13 plotted on log I vs $1/T$ scale. The initial slope of the TSCD obtained in the dark is about 0.3 eV. The activation energy of the semiconductor is $E = 0.6$ eV.

that we are simply studying the relaxation phenomena in a material whose dark conductivity $\sigma(T)$ was charged by prior illumination. It is well known[27] that the dark conductivity of these materials is increased after exposure to light. This excess conductivity called "frozen-in photoconductivity" takes several hours to decay after the light is switched off. The reason for this behavior is not yet fully understood.[28] It may be caused by electrons getting trapped in the localized states by light and then coming to equilibrium slowly in the dark or, alternatively, it may be caused by photostructural changes.[29] Whatever the reason, the photodepolarization curve does not give any new information about this phenomenon, since the difference in the photodepolarization and the dark depolarization curve is simply explained as the difference in relaxation currents resulting from different conductivities of the exposed and the unexposed sample.

It may be interesting to note that the slope of the dark TSCD curve in Fig. 14 is about 0.3 eV, which agrees with that of the calculated relaxation curve which was obtained without reference to any particular trap level.

As pointed out in Sec. II the number, position, and height of the TSCD peaks depend on the sample geometry. The curve shown in Fig. 15, for example, was obtained with the same chalcogenide material used for Figs. 13 and 14, but in the geometry of Fig. 2(c). The dimensions are given in the figure inset. The same curve was obtained in a polarization and depolarization experiment. Therefore, an attempt to ascribe[30] the peaks to different trap levels is unwarranted.

A. High-field regime

The sample of Fig. 2(c) geometry having a mica insulator was subjected to successively increasing polarization voltages V_d. Figure 16 illustrates the experimental curves where the current on the Y axis has been normalized by dividing by V_d. The heights of the peaks were found to scale linearly with V_d until a field of approximately 5×10^4 V/cm

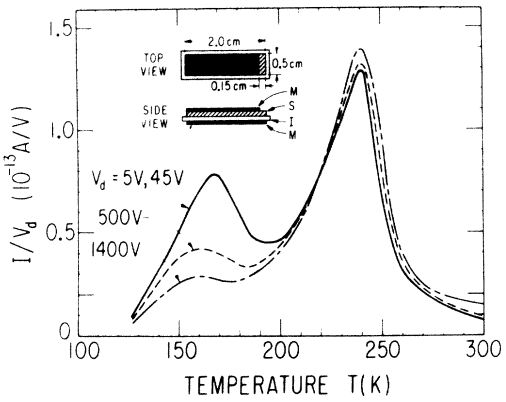

FIG. 16. Experimental TSCD for the sample of Fig. 15 as a function of polarizing voltage V_d. The ordinate shows the ratio I/V_d.

across the mica was reached. For V_d corresponding to a field higher than 5×10^4 V/cm a decrease in the normalized height of the low-T peak and a shift to lower temperatures is observed.

This observation can be explained in terms of the previous calculations of the relaxation current by taking account of the field dependence of the conductivity of the chalcogenide glass. In Fig. 17 calculated relaxation currents are presented for the sandwich geometry of Fig. 2(a) which gives rise to the low-T peak of Fig. 16. A field dependence of the form

$$\sigma = \sigma_0 e^{-E/kT} e^{V_d/V_0}$$

was chosen because it describes the field dependence of σ in a large class of amorphous semiconductors.[31] Figure 17 shows calculated relaxation curves for some typical values of V_0. The same trend as that shown by the low T peak of Fig. 16 is observed. The high-T peak of Fig. 16 is essentially unaffected by the large values of V_d because the potential drop in the edge piece of the semiconductor is distributed over a much larger distance so that the fields remain low.

This demonstrates that a description of the relaxation currents requires the dependence of the conductivity on both field F and temperature. In the case of the transverse geometry of Fig. 2(b) one has to consider not only the bulk conductivity $\sigma(T,F)$ but also the conductivity in the space-charge region modified by the (transverse) field effect. This can be obtained directly by measuring the field effect. Once $\sigma(T,F)$ is obtained by a conductivity measurement the relaxation data yield no further information.

IV. REVIEW OF LITERATURE AND CONCLUSIONS

Among the first authors to use the TSCD method for studying the trap levels in semiconductors were Driver and Wright,[1] who measured the thermal release of trapped space charge in CdS crystals. Subsequently several other groups[2–8] applied this method to CdS and other crystals in preference to the more commonly used TSC method because of the difficulty of subtracting dark current in the latter.

Following the success in crystals, the TSCD method is now being used to study the trap parameters in amorphous semiconductors.[17,18] Kolomiets *et al.*[12,13,15,16] and others[9–11,14] have studied TSCD using both light and electric field to disturb the equilibrium-carrier distribution in crystalline as well as amorphous semiconductors.

All these authors interpret their results in terms of trap-limited currents and derive various trap parameters. Our results, on the other hand, show that the TSCD in our material are relaxation currents, and a multitude of structure which is strikingly similar to that expected for trap-limited currents is produced by relaxation currents for commonly used geometries. Since most of the published results have neglected to mention all the parameters needed to calculate the dielectric relaxation currents, it is impossible for us to judge the validity of their interpretation in this way. We can, however, look at the requirements that the material under study must meet in order to give trap-limited TSCD. This may enable us to speculate upon the correctness of the published work.

The success of the TSCD experiments depends on (i) the extent to which the *shallow traps* in the space-charge region near the insulator interface

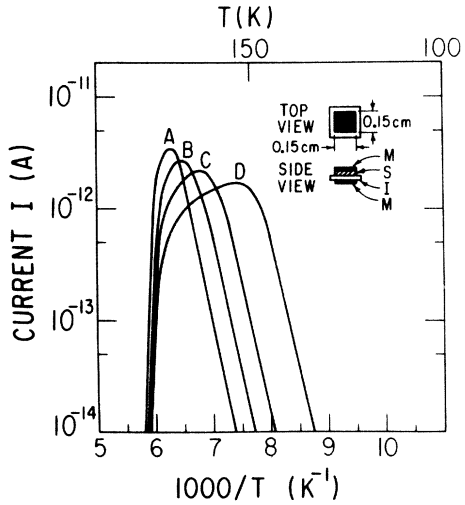

FIG. 17. Calculated dielectric relaxation curves for a semiconductor in geometry (*b*) obeying $\sigma = \sigma_0 e^{-E/kT} e^{V/V_0}$ at high fields. Parameters are $E = 0.5$ eV, $\sigma_0 = 9.2\times10^2$ $(\Omega\ \text{cm})^{-1}$, $V_d = 5$ V, $t_s = t_I = 1$ μm, and $\beta = 0.15$ K/sec. Curve (A): $V_0 = \infty$; (B): $V_0 = 1$ V; (C): $V_0 = 0.5$ V; (D) $V_0 = 0.25$ V.

can be filled and (ii) the ability of the released charges to reach the electrode. In condition (i) we refer to shallow traps between the Fermi level and the appropriate mobility edge because one cannot distinguish charges released from traps near the Fermi level and charge carriers excited in thermal equilibrium which give rise to the relaxation current. Condition (ii) is simply the statement of the fact that the released charges should have a sufficiently large drift range (Schubweg) in order to be detected. These conditions imply that the material under study must have a small number of localized states near the Fermi level and a large drift mobility. For the sandwich geometry of Fig. 2(a) the first condition requires a large enough mobility in the bulk of the material and for the parallel film geometry of Fig. 2(b) it means that the carrier mobility along the space charge region be large. For the geometry (*a*) we must further require that the screening length be large. This is to ensure that during depolarization the carriers can leave the space-charge region with an activation energy which is significantly less than that of the equilibrium carriers in the bulk. If any of the above requirements are not satisfied, one cannot hope to observe the trap-limited TSCD currents. In the case of multicomponent glasses, the drift mobility is very small. In particular, the drift-mobility measurements in our chalcogenide glass have proved unsuccessful,[32] probably due to strong retrapping by the recombination centers. Furthermore, capacitance and contact photovoltage measurements on this glass have shown that the screening length is quite small (≈ 200 Å).[22] These reasons make it almost impossible to detect the trap-limited currents in these multicomponent cross-linked chalcogenide glasses. However, other categories[33] of amorphous semiconductors do seem to satisfy these requirements. The twofold coordinated and two dimensionally bonded materials, e.g., Se, As_2Se_3, etc., and dielectric films, e.g., SiO_x, Al_2O_3, etc. have large enough band gaps and measurable mobilities to qualify as materials where trap-limited TSCD may be observable. Similarly, most of the crystals on which TSCD has been performed also satisfy the conditions mentioned above. So, the interpretations regarding these materials are quite possibly correct, although a proper analysis of the relaxation currents using the full field and temperature dependence of the conductivity and, in case of illumination, the frozen-in dark conductivity is still necessary. On the other hand, the interpretation of TSCD in terms of trap-limited currents in multicomponent chalcogenide glasses[12,13,16,18] is open to question. Further, it is evident that the dielectric relaxation peaks always occur at temperatures higher than trap-limited peaks. This fact may, in some cases, be useful in identifying dielectric relaxation peaks from the trap-limited peaks.

Although the relaxation currents yield no further information which is not already contained in $\sigma(T,F)$, they might be useful to obtain $\sigma(T,F)$ in cases where one blocking contact can for some reason not be avoided.

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APPENDIX A

The expression for the relaxation current in Eq. (2) can be simply derived as follows. Using the equivalent circuit of Fig. 18, one obtains

$$i = I + i_s = -(C_I + C_s)\frac{dV}{dt}\,, \tag{A1}$$

where $V = R(T)i$ is the voltage across C_s or C_I at time t.

Taking

$$R(T) = R_0 e^{E/kT}$$

and

$$T = T_0 + \beta t\,,$$

where β is the heating rate, we obtain

$$di/i = [E/kT^2 - (1/\beta R_0 C)\, e^{-E/kT}]\, dT\,. \tag{A2}$$

Upon integration and using the initial condition at

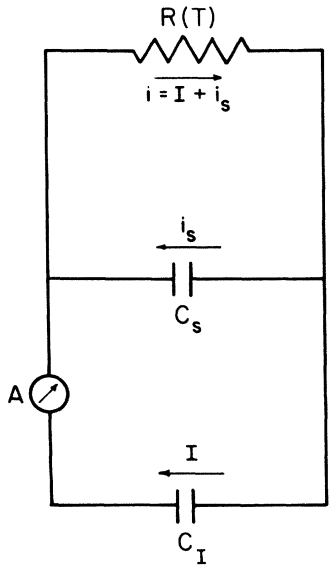

FIG. 18. Equivalent circuit for geometry (*a*) during depolarization.

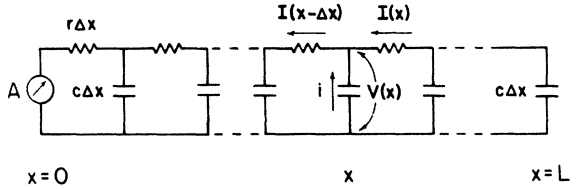

FIG. 19. Equivalent circuit for geometry (*b*) during depolarization.

$T = T_0$, $i = C_I V_d R(T_0)/(C_I + C_s)$, this gives

$$i(T) = \frac{C_I V_d}{C_I + C_s} \frac{1}{R_0} \exp\left[-x + \frac{1}{\beta(C_I + C_s)} \frac{E}{k} \times \left(\frac{e^{-x_0}}{x_0} - \frac{e^{-x}}{x} + \int_x^{x_0} \frac{e^{-x}}{x} dx\right)\right] , \quad \text{(A3)}$$

where

$$x = E/kT , \quad x_0 = E/kT_0 .$$

The current through the current meter (A) is then

$$I(T) = i(T) C_I/(C_I + C_s) . \quad \text{(A4)}$$

APPENDIX B

In this Appendix Eq. (4) of the text is derived. The equivalent circuit for the geometry of Fig. 2(b) is shown in Fig. 19. The total length L of the semiconductor is divided into infinitesimally small strips of width Δx. Each strip represents a capacitor of value $c\Delta x$ and a resistor of value $r\Delta x$; c and r being the resistance per unit length of semiconductor and capacitance per unit length of insulator, respectively. More explicitly,

$$r = 1/(\sigma W t_s) = r_0 e^{E/kT} , \quad c = C_I/L .$$

If $V(x, t)$ is the voltage across the capacitor at x, at time t, then in the limit $\Delta x \to 0$, we obtain

$$\frac{\partial I}{\partial x} = c \frac{\partial V}{\partial t} \quad \text{(B1)}$$

and

$$\frac{\partial V}{\partial x} = rI . \quad \text{(B2)}$$

If the heating rate is β, Eqs. (B1) and (B2) can be combined to give

$$\frac{\partial^2 V}{\partial x^2} = \beta r_0 c\, e^{E/kT} \frac{\partial V}{\partial T} . \quad \text{(B3)}$$

Equation (B3) is the familiar equation of heat conduction in one dimension.[34] The initial conditions are

(i) $V(0, T) = 0$, all T

(ii) $I(L, T) = 0$, all T

(iii) $V(x, 0) = V_d$, $0 \le x \le L$, taking $T_0 = 0$.

One obtains the following solution,

$$V(x, T) = \sum_{n=0}^{\infty} \frac{4V_d}{(2n+1)\pi} \sin\left((2n+1)\frac{\pi}{2}\frac{x}{L}\right) \times \left\{\exp\left[-\frac{(2n+1)^2\pi^2}{4\beta r_0 c L^2} \int_0^T e^{-E/kT} dT\right]\right\} . \quad \text{(B4)}$$

Using Eq. (B2), we finally obtain for the current,

$$I(0, T) = \frac{2V_d}{L r_0 e^{E/kT}} \times \sum_{n=0}^{\infty} \exp\left(-\frac{(2n+1)^2\pi^2}{4\beta r_0 c L^2} \int_0^T e^{-E/kT} dT\right) . \quad \text{(B5)}$$

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