Editors' Suggestion

Low-Latency Digital Signal Processing for Feedback and Feedforward in Quantum Computing and Communication

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Quantum computing architectures rely on classical electronics for control and readout. Employing classical electronics in a feedback loop with the quantum system allows us to stabilize states, correct errors, and realize specific feedforward-based quantum computing and communication schemes such as deterministic quantum teleportation. These feedback and feedforward operations are required to be fast compared to the coherence time of the quantum system to minimize the probability of errors. We present a field-programmable-gate-array-based digital signal processing system capable of real-time quadrature demodulation, a determination of the qubit state, and a generation of state-dependent feedback trigger signals. The feedback trigger is generated with a latency of 110 ns with respect to the timing of the analog input signal. We characterize the performance of the system for an active qubit initialization protocol based on the dispersive readout of a superconducting qubit and discuss potential applications in feedback and feedforward algorithms.

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I. INTRODUCTION

Recent quantum physical research is directed towards gaining experimental control of large-scale, strongly interacting quantum systems such as trapped ions [1] and solid-state devices [2]. The ultimate goal is to realize a quantum computer [3–6] with a large number of quantum bits (qubits) which may outperform classical computers for certain computational tasks [7–11]. However, quantum systems do not act as stand-alone components but must be combined with classical electronics to control inputs such as microwave pulses or external magnetic fields and to record and analyze the output signals [12]. Analyzing the output signals in real time can be advantageous for conditioning input signals on prior measurement results and therefore for realizing a feedback loop with the quantum system [13].

Quantum feedback schemes [14] make use of the results of quantum measurements to act back onto the quantum state of the system within its coherence time. Experimental realizations of quantum feedback have shown that it is possible to prepare and stabilize nonclassical states of electromagnetic fields in optical [15,16] and microwave [17] cavities, and to enhance the precision of phase measurements using an adaptive homodyne scheme [18].

The first demonstrations of feedback protocols with superconducting qubits showed an active initialization of qubits into their ground state [19] and the stabilization of Rabi and Ramsey oscillations [20,21]. Further recent feedback experiments with superconducting qubits have demonstrated the deterministic preparation of entangled two-qubit states [22,23], the reversal of measurement-induced dephasing [24], and the stabilization of arbitrary single-qubit states by continuously observing the spontaneous emission from a qubit [25].

Quantum feedforward schemes are closely related to quantum feedback schemes. In quantum feedforward schemes, one part of a quantum system is measured while the action takes place in another part of the quantum system. A prominent example for a feedforward scheme is the quantum teleportation protocol [26], which has been realized with active feedforward in quantum-optics setups [27–30], in molecules using nuclear magnetic resonance [31], trapped ions [32,33], atomic ensembles [34], and solid-state qubits [35,36].

The feedback latency is commonly defined as the time required for a single feedback round, i.e., the time between the beginning of the measurement of the state and the completion of the feedback action onto the state. A general requirement to achieve high success probabilities in quantum feedback schemes is that the feedback latency is much shorter than the time scale on which the quantum state decoheres.

Analog feedback schemes such as those reported in Refs. [20,25] feature feedback latencies on the order of 100 ns, where the latencies are limited by analog bandwidth and delays in the cables in the cryogenic setups. However, analog signal processing circuits have limited flexibility.

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The flexibility can be improved by using a digital signal processing (DSP) unit in the feedback loop, which can be implemented on a central processing unit (CPU) or on a field-programmable gate array (FPGA) [37]. CPU-based DSP systems offer versatile and convenient programing at the cost of several microseconds latency [17,19] due to the delays introduced by the digital input and output of the signal, which are too slow to achieve very low error probabilities for feedback operations on superconducting qubits.

In this paper, we describe a FPGA-based feedback-capable signal analyzer which allows for the real-time digital demodulation of a dispersive readout signal [38–40] and the generation of a qubit-state-dependent trigger with input-to-output latency of 110 ns. Our signal analyzer is therefore among the fastest feedback-capable digital signal analyzers reported thus far [21,22,41–43]. The capabilities of our signal analyzer enabled the feedforward action in the deterministic quantum teleportation experiment presented in Ref. [35]. In this paper, we illustrate the use of the feedback signal analyzer in a feedback loop for qubit initialization [19] and experimentally characterize its latency and performance.

The paper is organized as follows: In Sec. II, we present an overview of a typical feedback loop in which our instrument is used and analyze the feedback latency. In Sec. III, we discuss the implementation of the digital signal processing on the FPGA and analyze the processing latencies. Finally, in Sec. IV, we experimentally characterize the performance of the feedback loop. In the appendixes, we provide more details about our experimental setup and our implementation of the digital signal processing on the FPGA.

II. OVERVIEW OF THE FEEDBACK LOOP

In this section, we explain the elements of the typical feedback loop shown in Fig. 1(a). We design the feedback loop to issue pulses onto a superconducting qubit inside a dilution refrigerator conditioned on a measurement of the qubit state by analog and digital signal processing using cryogenic and room-temperature electronics. We first discuss the elements of the detection scheme and the actuator electronics, then present the latencies of the feedback loop. We provide a detailed description of our experimental setup in Appendix A.

A. Principle of the detection scheme

We consider the dispersive readout of the state of transmon qubits [45,46] with typical frequencies $\omega_q/(2\pi) \approx$ 4–6 GHz for the transition between the ground $|g\rangle$ and first excited state $|e\rangle$. We couple a microwave resonator to the qubit [the green box in Fig. 1(a)] with a frequency difference between qubit and resonator designed to be in the dispersive regime [38,39].

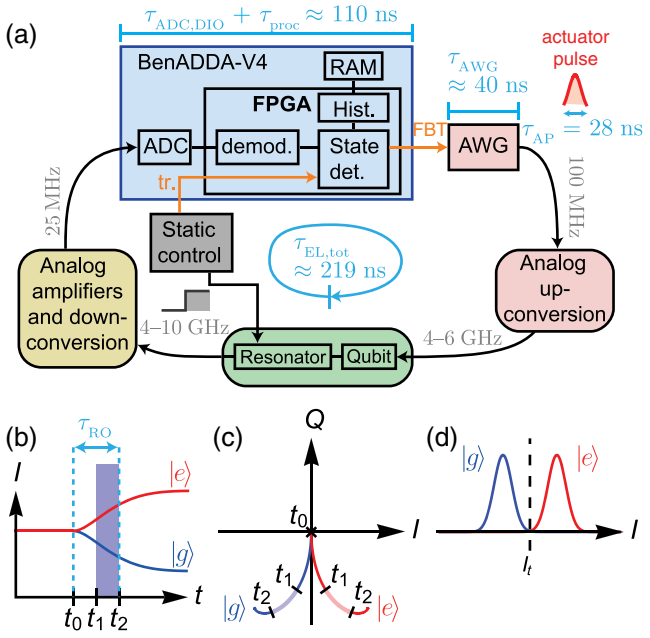

FIG. 1. (a) Overview of the feedback loop. Typical latencies are indicated in blue, and typical carrier frequencies of the signal are indicated in gray. See the text for details. (b) Sketch of the time dependence of the in-phase component I of the readout signal, which approaches different steady-state values depending on whether the qubit is in state $|g\rangle$ (the blue curve) or $|e\rangle$ (the red curve). We consider a scenario in which the response time of the resonator is much shorter than the lifetime of the qubit. Specific times indicated are the onset of the readout pulse (t_0), as well as the beginning (t_1) and the end (t_2) of the integration time (τ_i, the blue shaded region). We define the total readout time τ_{RO} as the time difference between t_0 and t_2 (the blue arrow between the dashed lines) [44]. (c) Sketch of the trajectories in the plane spanned by the I and Q components of the signal for the states $|g\rangle$ (the blue curve) and $|e\rangle$ (the red curve). Specific points in the trajectories are marked corresponding to the times t_0, t_1, and t_2 as defined in (b). (d) Sketch of the typical distribution of the integrated in-phase component (I) when the qubit is in state $|g\rangle$ (the blue curve) or $|e\rangle$ (the red curve). The dashed line represents the threshold value I_t for determining the state of the qubit.

In our experimental realization of the feedback loop (see Sec. IV), the qubit transition frequency is $\omega_q/(2\pi) =$ 6.148 GHz, and the center resonator frequency amounts to $\omega_r/(2\pi) = 7.133$ GHz, with the dispersive coupling rate $\chi/(2\pi) \approx 1.1$ MHz between the qubit and the resonator. Depending on whether the qubit is in state $|g\rangle$ or $|e\rangle$, we observe the dispersively shifted resonator frequency at $\omega_r \pm \chi$, respectively.

The qubit-state-dependent frequency shift leads to a state-dependent resonator response when the resonator is probed with a microwave pulse. In the dispersive readout scheme, high-fidelity quantum nondemolition readout [13] is achieved when probing the resonator with power $\kappa\langle\hat{n}\rangle\hbar\omega_r \approx 10^{-16}$ W, such that the steady-state average photon number $\langle\hat{n}\rangle$ in the resonator is on the order of

1–10 microwave photons [39,44,47–50]. Because of the low power, it is essential to connect the output of the resonator to a Josephson parametric amplifier (JPA) [47,51–59] to be able to discern the qubit-state-dependent resonator response within a single repetition of the experiment and in a time shorter than the qubit lifetime. Other schemes involve the direct coupling of a qubit to a Josephson bifurcation amplifier [60–63], autoresonant oscillator [64], or parametric oscillator [65] to be able to discern the qubit state with a higher microwave power.

For simplicity, we consider the case where the resonator is probed with a microwave pulse with frequency ω_r and a square envelope. The scheme considered here could be extended to include more sophisticated pulse shapes [44,49,66,67], which increase the speed and fidelity of the readout as well as the speed of the reset of the intraresonator field.

We employ the complex representation of the signal $I(t) + iQ(t) \equiv A(t)\exp[\phi(t)]$, where $A(t)$ and $\phi(t)$ are the time-dependent amplitude and phase of the signal at frequency ω_r. Upon transmission of the readout pulse with frequency close to resonance, the time-dependent in-phase $I(t)$ and quadrature $Q(t)$ components of the signal follow an exponential rise towards steady-state values starting at time t_0 after the onset of the readout pulse, as illustrated in Fig. 1(b) [68]. The steady-state values depend on whether the qubit is in state $|g\rangle$ (the blue curve) or state $|e\rangle$ (the red curve). The trajectories of the readout signal in the two-dimensional plane spanned by I and Q, as sketched in Fig. 1(c), start at the center of the plane which corresponds to zero amplitude and move in two different directions depending on the qubit state $|g\rangle$ (the blue curve) or $|e\rangle$ (the red curve).

The signal is subject to noise added by passive and active components [69]. Therefore, we apply a linear filter to the signal with the goal of attenuating noise frequency components while keeping the frequency components that contain the signal [24,40,44,70]. Specifically, we apply a moving-average filter which is advantageous in terms of the signal processing latency (see Sec. III C). The moving average is equivalent to an unweighted integration of the original signal in a particular integration window starting at a variable time t_1 and ending at time $t_2 = t_1 + \tau_i$ [see Figs. 1(b) and 1(c)], where τ_i is a constant integration time. We define the total readout duration as the time difference $\tau_{\mathrm{RO}} \equiv t_2 - t_0$ between the onset of the readout pulse and the end of the integration window. In the experiment presented in Sec. IV, we use an integration window of $\tau_i = 40$ ns and a readout duration of $\tau_{\mathrm{RO}} = (105 \pm 2)$ ns.

In the absence of transitions between qubit states during the integration time, the statistical distribution of the integrated signal, when the experiment is repeated many times, is expected to be represented by two Gaussian-shaped peaks in a histogram of the I component [Fig. 1(d)]. In the presence of qubit state transitions during the readout, the distributions corresponding to the states $|g\rangle$ and $|e\rangle$ are expected to be non-Gaussian with an increased overlap [40,44]. We discern the states $|g\rangle$ and $|e\rangle$ of the qubit by comparing the I signal to a threshold value I_t [the dashed line in Fig. 1(d)]. The fidelity of the readout depends on the signal-to-noise ratio of the readout signal [44,49]. To maximize the readout fidelity, we optimize the integration window and threshold value I_t.

B. Implementation of the detection scheme

The readout pulse is issued by the static-control hardware [the gray box in Fig. 1(a)]. Simultaneously, the static-control hardware sends a trigger [tr. in Fig. 1(a)] to the FPGA to synchronize the digital signal processing with the readout pulse.

We use an analog detection chain [the yellow box in Fig. 1(a)] containing amplifiers with a total gain of approximately 120 dB (see Appendix A) to detect the signal at the output of the resonator. In addition, the detection chain uses analog down-conversion electronics to convert the readout signal to an intermediate frequency ω_{IF} compatible with the sampling rate $f_s = 100 \times 10^6$ samples/s of our DSP unit. We choose an intermediate frequency at a quarter of the sampling frequency, i.e., $\omega_{\mathrm{IF}}/(2\pi) = f_s/4 = 25$ MHz, which allows for efficient digital down-conversion (see Sec. III C). In comparison to $\omega_{\mathrm{IF}} = 0$, an intermediate frequency on the order of tens of megahertz followed by digital demodulation avoids the low-frequency noise and unwanted dc offsets which typically occur when using an analog-to-digital converter (ADC) to digitize the signal [41,71,72].

We digitize the down-converted signal using a single ADC channel followed by digital demodulation into its I and Q components. An alternative method is to separately digitize the I and Q channels obtained from an analog I-Q mixer, which leads to a factor of 2 increase of the effective bandwidth and avoids adding noise from the unwanted sideband. Thus, this two-channel method is useful, especially in combination with a high-bandwidth nondegenerate parametric amplifier [57,73]. However, the separate digitization of the I and Q channels is sensitive to mismatches between the conversion-loss and reference level which lead to a distortion of the digitized complex signal. These imperfections can be adjusted for by digital signal processing or by recombining the two channels into a single one by the introduction of a 90° hybrid coupler after the analog I-Q mixer, effectively realizing an image-rejection mixer [74].

We implement the digital signal processing on a Xilinx Virtex-4 FPGA mounted on a commercial DSP unit by Nallatech (BenADDA-V4™) [the blue box in Fig. 1(a)], which includes an ADC with sampling rate $f_s = 100 \times 10^6$ samples/s and 14-bit voltage resolution. In a first step, the DSP digitally demodulates the signal [labeled as demod. in Fig. 1(a)]. The state discrimination module [state det. in Fig. 1(a)] then compares the filtered I signal

at time τ_{RO} to the threshold I_t, to determine the qubit state from the demodulated signal. Depending on the determined qubit state, a feedback trigger [FBT in Fig. 1(a)] is sent from the FPGA to the actuator electronics.

C. Actuator

The actuator is realized with an arbitrary waveform generator (AWG). When it receives the feedback trigger, the AWG generates a feedback pulse with a sampling rate of 1 GHz. In our experiment, the actuator pulse (AP) has a duration of $\tau_{\mathrm{AP}} = 28$ ns and uses the derivative removal by adiabatic gate (DRAG) technique [75,76] to prevent transitions to higher excited states of the transmon outside of the subspace spanned by the states $|g\rangle$ and $|e\rangle$. We typically generate the actuator pulse with a carrier frequency of 100–300 MHz limited by the bandwidth of the AWG and the analog mixer. In the experiment presented in Sec. IV, we choose a carrier frequency of 100 MHz for the actuator pulse. We use an analog mixer to up-convert the actuator pulse to the qubit transition frequency, which is typically in the range of 4–6 GHz. Forwarding this pulse to the qubit realizes a conditional quantum gate on the qubit closing the feedback loop.

D. Latencies

We define the latency τ_{FB} of the feedback (FB) loop [Fig. 1(a)] as the time from the beginning of the readout pulse until the completion of the feedback pulse, i.e.,

$$\tau_{\mathrm{FB}} \equiv \tau_{\mathrm{EL,tot}} + \tau_{\mathrm{RO}} + \tau_{\mathrm{AP}}, \tag{1}$$

where $\tau_{\mathrm{EL,tot}}$ is the total electronic delay of the signal in the analog and digital components and cables of the feedback loop, τ_{RO} is the readout duration (see Sec. II A), and $\tau_{\mathrm{AP}} = 28$ ns is the length of the actuator pulse (see Sec. II C). We measure the total electronic delay $\tau_{\mathrm{EL,tot}} = (219 \pm 2)$ ns *in situ* by changing the up-conversion frequency of the feedback pulse to the resonance frequency of the readout resonator and adjusting the amplitude of the pulse. The resonant feedback pulse is transmitted through the resonator, which makes it possible to determine the timing of the feedback pulse relative to the readout pulse. By adding up the contributions according to Eq. (1), we infer a feedback latency of $\tau_{\mathrm{FB}} = (352 \pm 3)$ ns.

The electronic delay

$$\tau_{\mathrm{EL,tot}} \equiv \tau_{\mathrm{proc}} + \tau_{\mathrm{ADC,DIO}} + \tau_{\mathrm{AWG}} + \tau_{G,\mathrm{tot}} \tag{2}$$

can be broken up into accumulated contributions. The signal processing, which we implemented in the FPGA, introduces a processing delay of three clock cycles $\tau_{\mathrm{proc}} = 30$ ns (see Sec. III). The feedback trigger is delayed by $\tau_{\mathrm{proc}} + \tau_{\mathrm{ADC,DIO}} = (110 \pm 3)$ ns with respect to the analog input signal, where $\tau_{\mathrm{ADC,DIO}}$ is the delay introduced by the ADC and digital interfaces (see Appendix B).

By subtracting the separately determined quantities τ_{proc}, $\tau_{\mathrm{ADC,DIO}}$, and τ_{AWG} from the total electronic delay $\tau_{\mathrm{EL,tot}}$, we estimate the inferred total group delay $\tau_{G,\mathrm{tot}} = (69 \pm 7)$ ns in the cables and analog components. We expect the total cable length connecting the analog and digital components to be the dominant contribution to the inferred group delay. The inferred group delay corresponds to an approximate total cable length of 14 m considering an effective dielectric constant $\epsilon_{\mathrm{eff}} \approx 2$ for the coaxial cables with polytetrafluoroethylene dielectric. This inferred total cable length is consistent with the experimental setup. The cable length in our setup could be reduced further by placing the individual components of the feedback loop closer to each other, which can be achieved, for example, by placing the FPGA and control electronics inside the dilution refrigerator [77–79].

III. FPGA-BASED DIGITAL SIGNAL PROCESSING

In this section, we describe our DSP circuit, which we implement on the Virtex-4 FPGA. To derive feedback triggers, the DSP circuit (Fig. 2) determines the qubit state by digital demodulation of the readout signal (see Sec. II). We start by discussing the digitization and synchronization of the input signal. Next, we discuss the signal processing features of each block and the corresponding latencies. Details of the FPGA implementation of each signal processing block are discussed in Appendix C. We analyze the FPGA timing and resource usage for the implementation of the DSP circuit on the Xilinx Virtex-4, Virtex-6, and Virtex-7 FPGA in Appendix D.

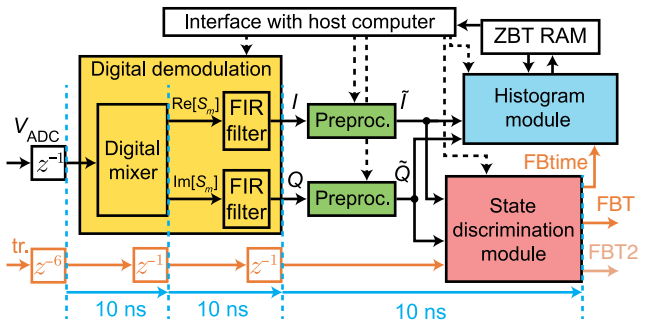

FIG. 2. Overview of the digital signal processing circuit showing the flow of the digitized signal (the black arrows) and the trigger lines (the orange arrows). The symbols z^{-n} denote delays by n clock cycles implemented with synchronous D flip-flops. The blue dashed lines mark positions at which the signal is further registered in pipelined registers not explicitly shown. The corresponding latencies of the pipeline stages are written below the blue arrows. The dotted lines indicate settings defined via the interface with the host computer. Explanations of each circuit block are given in the text.

A. Digitization of the input signal

Before entering the DSP circuit, the readout signal is digitized by an external ADC chip which samples the signal with rate $f_s = 100 \times 10^6$ samples/s. Typical readout signals are sine waves with qubit-state-dependent amplitude and phase, as shown in Fig. 3(a). We parametrize the time-dependent voltage at the input of the ADC as

$$V_{\mathrm{ADC}}(t) = \tilde{A}(t)\cos[\omega_{\mathrm{IF}}t + \phi(t)] = \frac{\tilde{A}(t)}{2}\left(e^{i[\omega_{\mathrm{IF}}t+\phi(t)]} + e^{-i[\omega_{\mathrm{IF}}t+\phi(t)]}\right). \quad (3)$$

As discussed in Sec. II B, we choose an intermediate frequency of $\omega_{\mathrm{IF}}/(2\pi) = f_s/4 = 25$ MHz for the readout signal after analog down-conversion (see Sec. II B), which is a useful choice for digital demodulation, as discussed below. The time-dependent amplitude $\tilde{A}(t)$ is proportional to the amplitude $A(t)$ of the field at the output of the resonator scaled by the gain of the analog detection chain and conversion loss of the mixer.

The ADC samples the signal $V_{\mathrm{ADC}}(t_n)$ at discrete times $t_n = n/f_s = n \times 10$ ns with index n. The ADC encodes the input voltage range of approximately ± 1 V as 14-bit fixed-point binary values. The fixed-point representation leads to a discretization step size of 2^{-13} V ≈ 0.12 mV. A trigger pulse is provided together with the analog signal via a separate digital input of the FPGA to mark the onset of the readout pulse.

B. Pipelined processing

We designed the DSP circuit to process the signal from the ADC in a pipelined manner. The signal from the ADC is initially buffered in a register implemented by synchronous D flip-flops (the ADC z^{-1} block in Fig. 2), which forward the value of the data (D) signal at each event of a rising edge of the sampling clock to the next processing element in the pipeline.

A separate trigger input (the orange lines in Fig. 2) marks the beginning of each experimental repetition. In order to synchronize the trigger with the ADC signal, the trigger initially goes through six pipelined registers (z^{-6} in Fig. 2), which compensate for the difference in delay between the ADC line and the trigger line. To synchronize the signal processing with the sampling clock, we insert further pipelined registers into the signal and trigger lines at specific points in the circuit (the blue dashed lines in Fig. 2).

C. Digital demodulation

As discussed in Sec. II B, we digitally demodulate the readout signal to obtain the I and Q components of the signal. Digital demodulation is achieved by digital frequency down-conversion, which involves digital mixing of the signal with a digital reference oscillator followed by digital low-pass filtering to remove noise and unwanted sideband frequency components [72].

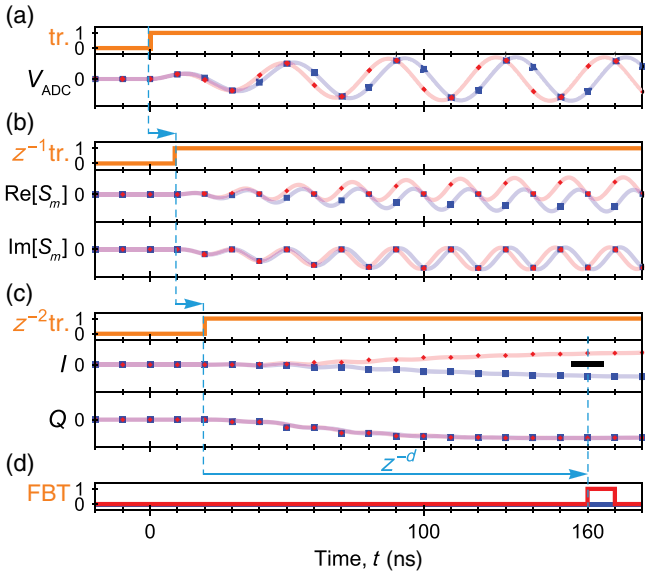

FIG. 3. Calculated signals at different processing stages for exemplary inputs when the qubit is in either the ground state (the blue line) or the excited state (the red line). The blue squares and the red diamonds represent the corresponding simulated digital signals obtained from a simulation of the FPGA design. The vertical axes display arbitrary units. The blue arrows and the dashed lines visualize the delays of the signals relative to each other. (a) The signals V_{ADC} from the ADC with two different phases, depending on whether the qubit is in the ground (blue) or excited state (red), together with the corresponding trigger (tr.) signals (the orange line). (b) Real (Re[S_m]) and imaginary (Im[S_m]) part of the complex signal at the output of the digital mixer with the corresponding trigger delayed by one clock cycle (z^{-1}tr.). (c) In-phase (I) and quadrature (Q) component of the signal obtained at the output of the FIR filter corresponding to a moving average of four consecutive points, with the corresponding trigger delayed by two clock cycles (z^{-2}tr.). (d) Feedback trigger (FBT) conditioned on a threshold on I indicated by the thick horizontal bar at $t = 160$ ns, which is set by the user-definable delay z^{-d} of $d = 14$ clock cycles.

1. Digital mixing

In the first part of the digital demodulation circuit (the yellow box in Fig. 2), we implement a digital mixing method [71,72] (indicated as digital mixer in Fig. 2) to obtain a sideband at zero frequency. In the digital mixer, the input signal V_{ADC} as defined in Eq. (3) is multiplied by a complex exponential with down-conversion frequency ω_{IF} to obtain a complex output signal S_m,

$$S_m(t_n) \equiv V_{\mathrm{ADC}}(t_n)e^{-i\omega_{\mathrm{IF}}t_n} = \frac{\tilde{A}(t_n)}{2}\left(e^{i\phi(t_n)} + e^{-i[2\omega_{\mathrm{IF}}t_n+\phi(t_n)]}\right). \quad (4)$$

The reason for the multiplication is to generate two sidebands corresponding to the two complex exponentials

in Eq. (4): one corresponds to the complex signal $I + iQ \equiv \tilde{A}(t)e^{i\phi(t)}/2$, and the other leads to oscillations with frequency $2\omega_{\mathrm{IF}}$ of the output signals of the mixer [Fig. 3(b)]. The complex signal $I + iQ$ is the basis on which we determine the state of the qubit after filtering out the oscillating sideband (see the following sections).

In practice, the real ($\mathrm{Re}[S_m]$) and imaginary ($\mathrm{Im}[S_m]$) parts of the output signal of the mixer are computed separately by multiplying the input signal with a discrete cosine to obtain the real part, and with a discrete negative sine to obtain the imaginary part. The FPGA implementation of the digital mixer is described in Appendix C 1. For $\omega_{\mathrm{IF}}/(2\pi) = f_s/4$, the digital mixer introduces a latency of less than one clock cycle (10 ns) due to its multiplierless implementation [71,72]. Since the output signal of the mixer is registered by synchronous D flip-flops, the effective latency for the multiplierless method is one clock cycle. For synchronization, the trigger signal is delayed by one clock cycle [z^{-1}tr. in Fig. 3(b)].

Compared to the $f_s/4$ mixing method, multiplication by a sinusoidal digital local oscillator (LO) of arbitrary frequency introduces a latency of one additional clock cycle (10 ns) in our implementation. Digital mixing with multiple arbitrary-frequency LOs will be useful for multiplexed readout [49,63,80–83] in future high-bandwidth versions of the signal processing unit.

2. Digital low-pass filter

The second essential part of the digital down-conversion circuit is a digital low-pass filter, which extracts the I and Q components from the signals $\mathrm{Re}[S_m]$ and $\mathrm{Im}[S_m]$ by removing the sideband spectral components oscillating at frequency $2\omega_{\mathrm{IF}}$ [72]. We implement the digital low-pass filter as a finite impulse response (FIR) filter [72], which is a discrete convolution of the digital signal with a finite sequence of filter coefficients. By matching the filter coefficients (integration weights) to the expected resonator response, it is possible to optimize the single-shot readout fidelity [24,40,44,48,49,70]. While, in principle, our DSP circuit allows for 40-point FIR filters with arbitrary filter coefficients, a moving average is the simplest type of FIR low-pass filter which is possible to implement without multipliers and therefore has a reduced processing latency and uses fewer FPGA resources than a more general FIR filter. The FPGA implementation of the moving average module is described in Appendix C 2.

The moving average (the FIR filter in Fig. 2) is applied separately to the real part ($\mathrm{Re}[S_m]$) and the imaginary part ($\mathrm{Im}[S_m]$) of the complex output signal of the digital mixer, S_m, leading to

$$I(t_n) + iQ(t_n) \equiv \frac{1}{l}\sum_{k=n-l+1}^{n} S_m(t_k), \tag{5}$$

which is a discrete convolution with a square window of length l. In the limit of negligible modulation bandwidth, the moving-average filters a sinusoidal oscillation perfectly if the window length l is a multiple of the oscillation period. In the case of $\omega_{\mathrm{IF}}/(2\pi) = f_s/4$, the periodicity of the unwanted terms at $2\omega_{\mathrm{IF}}$ is equal to two discrete samples. Therefore, any window length which spans an even number of samples is suitable to filter out the $2\omega_{\mathrm{IF}}$ sideband.

The output of the moving average with window length $l = 4$ is shown in Fig. 3(c). The I and Q signals at the output of the moving average show a smooth ramp towards a steady-state value. In the simulated signals shown in Fig. 3, an appropriate global phase offset is chosen such that the difference between the traces corresponding to the $|g\rangle$ and $|e\rangle$ states is maximized in the I component of the signal (see Sec. II A). The moving-average module has a latency of one clock cycle. The trigger is delayed accordingly by one additional clock cycle ($z^{-1}z^{-1}\mathrm{tr.} = z^{-2}\mathrm{tr.}$) for synchronization with the signal.

To implement a mode-matched filter [40,44,84], the moving-average circuit presented in Appendix C 2 could be extended by inserting a multiplication by a series of configurable weighting factors prior to the accumulation [43]. The weighted accumulation is implementable with latencies ≤ 15 ns on recent FPGAs [43].

D. Offset subtraction and scaling

Following the FIR filter block, the I and Q signals enter blocks which perform offset subtraction and scaling of the signal (the green boxes in Fig. 2). The main purpose of offset subtraction is to set a threshold value as described in Sec. III E. Moreover, offset subtraction and scaling allows us to make the best use of the fixed range and resolution used for recording histograms (see Sec. III F).

The outputs of the offset subtraction and scaling blocks are described by

$$\tilde{I}(t_n) \equiv m_I[I(t_n) - c_I], \tag{6}$$

$$\tilde{Q}(t_n) \equiv m_Q[Q(t_n) - c_Q], \tag{7}$$

where c_I and c_Q are offsets in the I-Q plane and m_I and m_Q are multiplication factors. We determine the parameters (c_I, c_Q) and (m_I, m_Q) in a calibration measurement. The latencies of the offset subtraction and scaling blocks are less than one clock cycle, and no synchronous D flip-flops are used.

E. State discrimination module

The state discrimination module (the red box in Fig. 2) determines the state of the qubit based on the preprocessed input signals $\tilde{I}$ and $\tilde{Q}$. Because of the offset subtraction, the threshold value for state discrimination can be kept fixed at

zero, which simplifies the FPGA implementation of the state discrimination module, as discussed in Appendix C 4.

The readout time τ_{RO} relative to the onset of the readout pulse (see Sec. II A) is specified with a variable delay of d clock cycles after the detection of the trigger signal, i.e., $d \times 10\ \text{ns} = \tau_{RO}$. In the example shown in Fig. 3(c), the $|g\rangle$ and $|e\rangle$ states of the qubit are discriminated based on a threshold value (the thick horizontal bar) defined for the I signal at a time $t = 160$ ns, which is $d = 14$ clock cycles after the detection of the trigger signal z^{-2}tr.. The simulated I signals corresponding to the $|0\rangle$ [the blue curve in Fig. 3(c)] and $|1\rangle$ [the red curve in Fig. 3(c)] states are well distinguishable at the time when the threshold is checked, such that the state of the qubit can be determined successfully even in the presence of noise (see Sec. IV). The state discrimination module either issues the feedback trigger [the red curve in Fig. 3(d)] or does not issue the feedback trigger [the blue curve in Fig. 3(d)], based on the determined qubit state.

Our DSP circuit provides the possibility of deriving a second feedback trigger (FBT2 in Fig. 2) based on both the in-phase ($\tilde{I}$) and quadrature ($\tilde{Q}$) signal components. For example, in the quantum teleportation protocol [26], the states of two qubits at the sender's location are measured in order to perform a state-dependent rotation on a qubit at the receiver's location. In our experimental realization of the teleportation protocol discussed in Ref. [35], we discriminated between the states of the two sender's qubits based on two threshold values defined for the I and Q signals. Based on the outcome of comparing the I and Q signals to the two threshold values, we issued two independent trigger signals to two separate AWGs in order to implement a conditional operation on the receiver's qubit [35].

F. Histogram module

The histogram module records how often the values of the signals $\tilde{I}$ and $\tilde{Q}$ obtained from a specific integration window fall into a particular histogram bin when the experiment is repeated many times. The bins are defined by subdividing the signal range from -1 to $+1$ into, typically, 128 bins. From the histogram, an estimate of the probability density function of the signal at the specified times is obtained.

We repeat the experiment 2×10^6 times, corresponding to a maximum count C around 10^4 for each histogram bin. This number of repetitions reduces the relative standard deviation $\sigma_C/C = 1/\sqrt{C}$ to approximately 1% around the maximum of the observed distributions. Storing the histogram of the signal needs less memory than storing the value of the signal in each repetition if the number of repetitions exceeds the number of histogram bins. The histogram module therefore allows for data reduction at the time when the data is recorded.

We have used the histogram module in previous experiments to characterize the quantum statistics of microwave radiation emitted from circuit QED systems [85–88]. In the context of feedback experiments, we record histograms to obtain the probabilities of observing a particular qubit state in two consecutive qubit readouts, as described in Sec. IV.

We update the histogram at the same time as the state discrimination module determines the qubit state in order to analyze the readout fidelity and feedback performance (see Sec. IV). We synchronize the state discrimination module and the histogram module using a marker signal (FBtime in Fig. 2) which is sent from the state discrimination module to the histogram module. We use an external zero-bus-turnaround (ZBT) random-access memory (RAM) (see Fig. 2) to store the histogram. When the recording of the histogram is completed, we transfer the histogram to the host computer via the interface. The implementation details of the histogram module are described in Appendix C 5.

IV. QUBIT STATE INITIALIZATION EXPERIMENT

In this section, the functionality of the presented DSP circuit is demonstrated in the context of a qubit state initialization experiment. In the experiment, we use the feedback loop to reset the state of a superconducting qubit [19,89–91] (see Appendix E) deterministically into its ground state, independent of its initial state. We correlate the outcomes of two consecutive qubit measurements in order to separate out the different effects, such as the qubit lifetime and readout fidelity, which contribute to the overall performance of the feedback protocol.

We choose the repetition period 10 μs of the experiment to be longer than the qubit lifetime $T_1 \approx 1.4$ μs, such that the qubit is approximately in thermal equilibrium with its environment at the beginning of each experimental repetition. We observe a finite thermal population $P_{\text{therm}} \approx 7\%$ of the excited state $|e\rangle$ due to the elevated effective temperature of about 114 mK of the system on which the experiments are performed (see Appendix F).

In order to test the feedback protocol, we prepare an equal superposition of the computational states $|g\rangle$ and $|e\rangle$ of the superconducting qubit. This choice of initial state will ideally lead to equal probabilities to find the states $|g\rangle$ and $|e\rangle$ when the qubit is measured. Preparing an equal superposition as an initial state will therefore test the feedback actuator for both computational states, $|g\rangle$ and $|e\rangle$, of the qubit. An additional data set (Appendix F) shows that the feedback scheme can also be used to reduce the thermal population of the excited state [19,90,92], providing an additional benchmark for our feedback loop.

Ideally, we consider the case where the qubit is initialized in the state $|g\rangle$ corresponding to the Bloch vector pointing to the upper pole of the Bloch sphere [stage 1 in Fig. 4(a)]. A microwave pulse at frequency ω_q [the green line in Fig. 4(b)] is applied to the qubit to realize a $\pi/2$ rotation which brings the qubit into the superposition state $|+\rangle \equiv (|g\rangle + |e\rangle)/\sqrt{2}$ corresponding to a Bloch vector

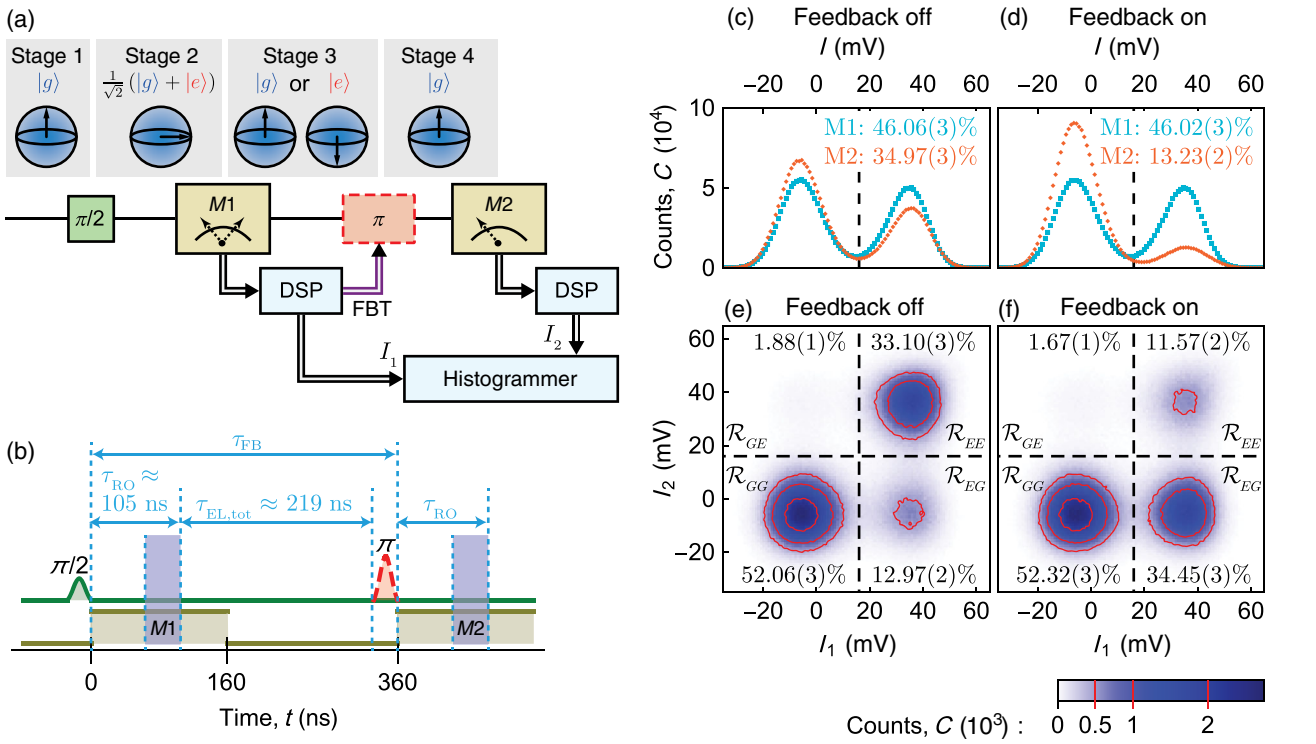

FIG. 4. (a) Quantum circuit depicting the experimental protocol to test the feedback routine. The state at each stage of the protocol is represented on the Bloch sphere (blue). The horizontal black line indicates the evolution of the qubit state over time. Double arrows ($\Rightarrow$) represent the flow of classical information. The sequence of operations is a $\pi/2$ rotation (the green box) of the Bloch vector about an equatorial axis, a first projective measurement ($M1$), a conditional π rotation (the red dashed box) that depends on the feedback trigger (FBT) determined by the digital signal processing (DSP), and a second projective measurement ($M2$) of the qubit state. (b) Pulse scheme showing the timing of microwave pulses applied to the qubit (the green trace), the pulses applied to the resonator (the yellow trace), and the conditional π pulse applied to the qubit (the red dashed line). The blue shaded regions mark the integration windows of the measurements $M1$ and $M2$. The time offset τ_{RO} marks the time from the beginning of each readout pulse to the end of the corresponding integration window, $\tau_{EL,tot}$ (the blue arrow) marks the delay in the feedback electronics, and τ_{FB} marks the total feedback latency as it is defined in the text. (c) Histograms of the in-phase signal I_1 obtained from the first readout pulse $M1$ (the blue dots) and in-phase signal I_2 obtained from the second readout pulse $M2$ (the orange dots) for the case when the feedback actuator is disabled. The dashed line marks the feedback threshold. For $M1$ and $M2$, the percentage of counts on the right side of the threshold is indicated. (d) The same type of histograms as in (c) but with the feedback actuator enabled. (e) Two-dimensional histogram with 128×128 bins counting the combined outcomes of the first readout I_1 (the horizontal axis) and the second readout I_2 (the vertical axis) for the case when the feedback actuator is disabled. The plane is divided into four regions ($\mathcal{R}_{GG}$, $\mathcal{R}_{GE}$, $\mathcal{R}_{EG}$, and $\mathcal{R}_{EE}$) separated by the threshold (the dashed lines). The percentage of counts relative to the total count is indicated in each quadrant. Red lines are contour lines marking specific counts of $\{0.5, 1, 2\} \times 10^3$. (f) The same type of two-dimensional histogram as in (e) but with the feedback actuator enabled.

pointing at the equator of the Bloch sphere [stage 2 in Fig. 4(a)].

When the qubit initially is in state $|e\rangle$—for example, due to the nonzero temperature of the system—the effect of the $\pi/2$ rotation is to prepare the state $|-\rangle \equiv (|g\rangle - |e\rangle)/\sqrt{2}$, which is an equal superposition of $|g\rangle$ and $|e\rangle$ with a different phase. The states $|+\rangle$ and $|-\rangle$ are expected to lead to an identical distribution of outcomes in the state detection.

In the experiment, directly after the preparation of the initial state, at time $t_{M1} = 0$, the state of the qubit is measured with a readout pulse 160 ns long (see $M1$ in Fig. 4) applied to the resonator. The dispersive readout projects the state of the qubit into either the ground or the excited state corresponding to the upper and lower pole of the Bloch sphere [stage 3 in Fig. 4(a)]. The DSP (see Sec. III) extracts the in-phase component I_1 during the readout pulse $M1$. We filter the signal I_1 with a moving average of four consecutive samples, corresponding to an integration window [the blue region $M1$ in Fig. 4(b)] of 40 ns. We extract the time $\tau_{RO} \approx 105$ ns of the end of the integration window [93] relative to the beginning of the readout pulse by fitting a theoretical model to the switch-on dynamics of the readout signal in a time-resolved measurement [44].

The histogram of I_1 [the blue dots in Fig. 4(c)] reveals two Gaussian peaks corresponding to the distributions of the in-phase signal for the qubits in states $|g\rangle$ and $|e\rangle$. The measured initial excited-state probability, $\mathbb{P}[E_1]_{\text{FB off}} = 46.06(3)\%$, is the fraction of counts of values I_1

above the threshold value $I_t = 16$ mV [the dashed line in Fig. 4(c)] relative to the total count $C_{\mathrm{tot}} = 2^{21} \approx 2 \times 10^6$ of the measurements.

With a master equation [94], we simulate the decay of the qubit state with characteristic time $T_1 = 1.4$ μs during the time of the $\pi/2$ pulse and the readout up to the center of the integration window [see Fig. 4(b)]. Furthermore, we take into account a bias of the measured probabilities towards 50% due to the finite readout error of 3% (see Appendix G). From the master equation simulation, we obtain an expected excited-state probability of $\mathbb{P}[E_1]_{\mathrm{sim}} = 47.07\%$ in the first measurement, $M1$, which agrees reasonably well with the measured probability, $\mathbb{P}[E_1]_{\mathrm{FB\,off}}$ (see above). A source of systematic errors is measurement-induced mixing [95]. An additional reason for the systematic deviation of the measured probability from the simulated probability is that the threshold value $I_t = 16$ mV, which is chosen based on a previous calibration measurement, deviates from the value $I_{t,\mathrm{opt}} \approx 13$ mV which optimizes readout fidelity (see Appendix G). This offset leads to a bias of the observed probabilities towards the ground state in addition to a systematic bias due to state transitions during the integration time [44].

The feedback loop is configured to deterministically prepare the state $|g\rangle$ [stage 4 in Fig. 4(a)]. The feedback pulse, inducing a π rotation of the Bloch vector of the qubit, turns the state $|e\rangle$ into $|g\rangle$, and vice versa. Thus, the feedback π pulse is issued only if the first measurement ($M1$) reveals the qubit to be in state $|e\rangle$. The π pulse [the red dashed line in Fig. 4(b)] arrives at the qubit with a delay of $\tau_{\mathrm{EL,tot}}$ (see Sec. II D) conditioned on the readout result of $M1$.

For verification, a second readout pulse ($M2$ in Fig. 4) is applied to the qubit at the time $t_{M2} = 360$ ns directly after the arrival of the feedback pulse at the qubit. The difference between t_{M2} and the beginning of the first readout pulse corresponds to the total feedback latency τ_{FB} (see Sec. II D). We record histograms of I_2, which is the filtered in-phase component of the signal at time $t_{M2} + \tau_{\mathrm{RO}}$. When the feedback actuator is disabled, the histogram of I_2 [the orange dots in Fig. 4(c)] shows reduced counts on the right side of the threshold with an excited-state probability of $\mathbb{P}[E_2]_{\mathrm{FB\,off}} = 34.97(3)\%$. Extending the master-equation simulation introduced above to include the full pulse sequence up to the second readout pulse, we obtain $\mathbb{P}[E_2]_{\mathrm{FB\,off,sim}} = 37.89\%$, which is in reasonably good agreement with the measured value. The state decay between $M1$ and $M2$, which leads to the observed reduction in the excited-state population, causes errors in the feedback action, as discussed below.

When the experiment is repeated with the feedback actuator enabled, the double-peaked histogram obtained from the first readout I_1 [the blue dots in Fig. 4(d)] is approximately identical to the case without feedback, as expected, with the measured excited-state probability $\mathbb{P}[E_1]_{\mathrm{FB\,on}} = 46.02(3)\%$ agreeing with $\mathbb{P}[E_1]_{\mathrm{FB\,off}}$ within the statistical error bars. After the feedback pulse, in the histogram of I_2 [the orange dots in Fig. 4(d)], the measured excited-state probability is significantly reduced to $\mathbb{P}[E_2]_{\mathrm{FB\,on}} = 13.23(2)\%$. This probability compares reasonably well with the simulated value of $\mathbb{P}[E_2]_{\mathrm{FB\,on,sim}} = 10.50\%$ obtained from the master-equation simulation introduced above. We attribute the difference between the measured and simulated values of $\mathbb{P}[E_2]_{\mathrm{FB\,on}}$ to measurement-induced mixing and the deviation of the feedback threshold from the optimal value (see above).

To obtain a figure of merit for the feedback protocol that is independent of characteristics such as state decay and temperature of the quantum system, we study correlations between the outcomes of the two readout pulses $M1$ and $M2$. From the two-dimensional histograms [Figs. 4(e) and 4(f)] with axes I_1 and I_2, we obtain experimental probabilities to observe a specific range $\mathcal{R}$ of two consecutive measurement outcomes (I_1, I_2). The probabilities $\mathbb{P}[\mathcal{R}_{xy}]$ correspond to observing the qubit in state x with the first readout pulse and, consecutively, in state y with the second readout pulse. These probabilities are obtained from the normalized counts in the four quadrants ($\mathcal{R}_{GG}$, $\mathcal{R}_{GE}$, $\mathcal{R}_{EG}$, and $\mathcal{R}_{EE}$) separated by the threshold [the dashed lines in Figs. 4(e) and 4(f)].

When the feedback is enabled, the measured probability $\mathbb{P}[\mathcal{R}_{EE}]_{\mathrm{FB\,on}} = 11.57(2)\%$ [Fig. 4(f)] corresponds to the unwanted event of the state $|e\rangle$ being observed consecutively with both readout pulses. We explain the dominant contribution to $\mathbb{P}[\mathcal{R}_{EE}]_{\mathrm{FB\,on}}$ by state decay between the first readout pulse and the feedback pulse. The probability of state decay between the first and second readout pulses is extracted from a reference measurement of $\mathbb{P}[\mathcal{R}_{EG}]_{\mathrm{FB\,off}} = 12.97(2)\%$ [Fig. 4(e)] when the feedback is disabled. The probabilities $\mathbb{P}[\mathcal{R}_{EE}]_{\mathrm{FB\,on}}$ and $\mathbb{P}[\mathcal{R}_{EG}]_{\mathrm{FB\,off}}$ are close to each other since the conditional π pulse swaps the state $|g\rangle$ with $|e\rangle$ before the second readout pulse. The corresponding simulated probabilities $\mathbb{P}[\mathcal{R}_{EE}]_{\mathrm{FB\,on,sim}} = 8.32\%$ and $\mathbb{P}[\mathcal{R}_{EG}]_{\mathrm{FB\,off,sim}} = 11.37\%$ (see Table I) are in reasonable agreement with the experimental values considering the sources of systematic errors discussed above.

The measured probability $\mathbb{P}[\mathcal{R}_{GE}]_{\mathrm{FB\,on}} = 1.67(1)\%$ [Fig. 4(f)] of a transition from state $|g\rangle$ to $|e\rangle$, when the feedback loop is enabled, is close to the reference value $\mathbb{P}[\mathcal{R}_{GE}]_{\mathrm{FB\,off}} = 1.88(1)\%$ [Fig. 4(e)] when the feedback is disabled. The approximate equality of these two probabilities shows that the state is correctly left unchanged when the qubit is already in state $|g\rangle$. A possible reason for the small systematic deviation of $\mathbb{P}[\mathcal{R}_{GE}]_{\mathrm{FB\,on}}$ from $\mathbb{P}[\mathcal{R}_{GE}]_{\mathrm{FB\,off}}$, which is on the order of 0.2%, could be drifts in the experimental parameters, such as the phase of the readout signal.

In summary, the probabilities of the combined events (Table I) show that, in the feedback protocol, the π pulse is applied only when it is intended, and that the probability of

TABLE I. Experimental and simulated probabilities $\mathbb{P}[\mathcal{R}_{xy}]$ of the events for observing the qubit in state x in the first measurement, and in state y in the second measurement when the feedback is either disabled (off) or enabled (on). The simulated values are obtained from a master-equation simulation. See the text for details.

	Feedback off		Feedback on	
	Experimental	Simulated	Experimental	Simulated
$\mathbb{P}[\mathcal{R}_{GG}]$	52.06(3)%	50.74%	52.32(3)%	50.74%
$\mathbb{P}[\mathcal{R}_{GE}]$	1.88(1)%	2.18%	1.67(1)%	2.18%
$\mathbb{P}[\mathcal{R}_{EG}]$	12.97(2)%	11.37%	34.45(3)%	38.75%
$\mathbb{P}[\mathcal{R}_{EE}]$	33.10(3)%	35.71%	11.57(2)%	8.32%

the unwanted events in region $\mathcal{R}_{EE}$ is limited by state decay between the first measurement and the feedback pulse. Our results show that the latency time of our feedback implementation is sufficiently short to demonstrate its functionality within the qubit lifetime.

In a further experimental run, we use the feedback to prepare the excited state $|e\rangle$ by issuing the feedback π pulse only when the ground state is detected in the initial readout, $M1$ [19]. As in the protocol shown in Fig. 4(a), we prepare the state $(|g\rangle + |e\rangle)/\sqrt{2}$ before the initial readout, $M1$. The experimentally determined excited-state probability in the readout $M2$ after the feedback pulse amounts to 81.8%. For comparison, we obtain a predicted excited-state probability of 83.2% from the master-equation simulation with the same parameters as for the simulations presented above. The feedback-assisted preparation of the excited state provides a further benchmark for the feedback loop.

V. CONCLUSIONS AND DISCUSSION

Here, we develop a low-latency FPGA-based digital signal processing unit for quantum feedback and feedforward applications such as the qubit initialization scheme presented in this paper and the deterministic quantum teleportation realized in Ref. [35]. The histogram module, which we implement on the FPGA, stores the relevant information about the readout signal in real time and in a memory-efficient manner and thus improves the scalability of both the experimental repetition rate and the number of readout channels. The techniques presented in this work are generally applicable independent of the specific quantum system. For example, the signal processing techniques could be adapted for use with charge- or spin-based quantum-dot qubits [96–99].

Our experimental results show that the feedback loop performs as expected. The total electronic delay of the signal in the feedback loop is $\tau_{\mathrm{EL,tot}} = (219 \pm 2)$ ns, determined by the sum of ADC latency, processing latency, AWG latency, and cable delays. Adding the quantum-device-specific readout time and feedback pulse duration, we obtain a total feedback latency $\tau_{\mathrm{FB}} = (352 \pm 3)$ ns. To reduce the probability of state decay between the state detection and the feedback action, the ratio $r \equiv \tau_{\mathrm{FB}}/T_1$ of the feedback latency to the qubit lifetime T_1 needs to be reduced. Since the probability of state decay is expected to be proportional to $1 - \exp(-r)$, a T_1 time of about 40 μs would be needed to achieve error probabilities of less than 1% in one iteration of the feedback scheme presented in this work. With the longest T_1 times achievable with state-of-the-art superconducting circuits of up to approximately 100 μs [100–102], we estimate a probability of approximately 0.3% for errors due to state decay given our total feedback latency. In the present work, we demonstrate digital processing latencies on the order of 30 ns, which is among the shortest latencies reported for FPGA-based signal analyzers [21,22,43] in the context of superconducting qubits. Simultaneously, the use of advanced readout strategies enables shorter optimal readout times [44,49]. Shorter latencies for analog-to-digital conversion and cable delays may be achievable by using custom-made circuit boards which work at cryogenic temperatures [77–79] or by using on-chip logical elements [103–105].

Low-latency feedback loops may play a role in realizing future quantum computers, where a key ingredient is quantum error correction [106–108], in which error syndromes of a quantum-error-correction code are detected by repetitive measurements. The syndrome measurements are designed to keep track of unwanted bit flip and phase errors. In this context, it is essential to have a flexible low-latency classical processing unit to process the error syndromes without causing additional delay for the quantum processor. A large set of quantum-error-correction codes may work with a passive "Pauli-frame" update [109]; however, it still remains an open question [110] whether some level of correction and qubit reset using active feedback is preferable. Therefore, having a low-latency signal processor with feedback capabilities, as presented in this work, will be instrumental for scaling up quantum technologies. In future multiqubit experiments, frequency-multiplexed readout techniques [49,63,80–83] could be implemented, in combination with parallel digital demodulation. We estimate that we can implement on the order of ten parallel digital demodulation channels with adjustable intermediate frequencies on a Virtex-6 FPGA. A further constraint is set by the spectral overlap of the signals for each qubit, which puts a practical limit on the number of qubits that can faithfully be read out within the bandwidth of the ADC.

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APPENDIX A: EXPERIMENTAL SETUP

The device under test (DUT, the green box in Fig. 5) is a superconducting circuit with one superconducting transmon qubit. The DUT is thermalized to the 20-mK stage of a dilution refrigerator (the purple box in Fig. 5).

Single-qubit quantum gates are realized by driving transitions between the ground and first excited states of the transmon by applying microwave pulses through a dedicated microwave line (port *A* in Fig. 5). The microwave line is thermalized by attenuators at three cryostat stages (4-K plate, 100-mK plate, and baseplate in Fig. 5). The attenuators reduce the signal and noise coming from the room-temperature electronics and add Johnson-Nyquist noise at their respective temperature T, thereby reducing the effective temperature of the microwave radiation in the cable. The qubit pulses for static control (the gray box in

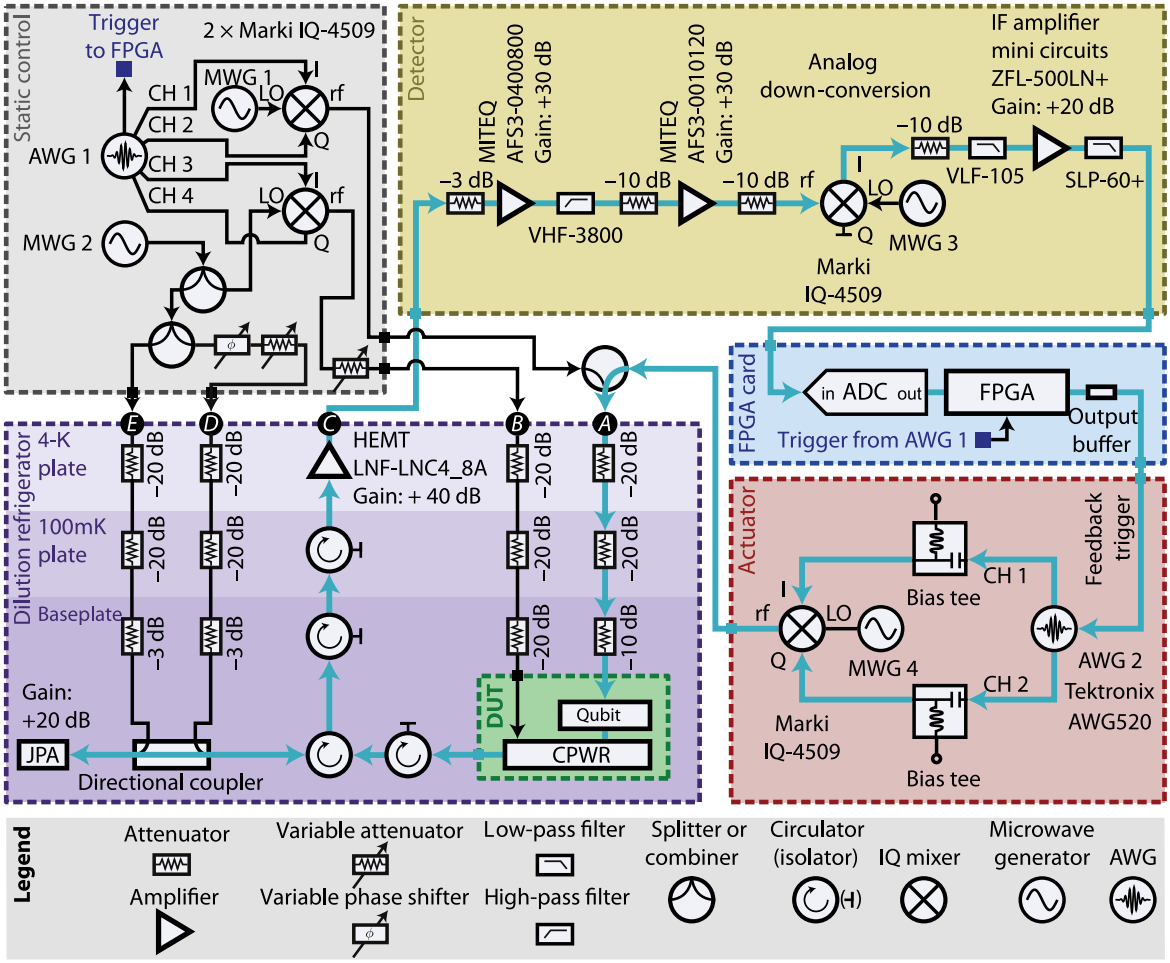

FIG. 5. Schematic of the experimental setup used for quantum feedback. Cyan arrows point into the direction of the signal flow in the feedback loop. The device under test (DUT) is a superconducting circuit comprising a qubit coupled to a coplanar waveguide resonator (CPWR). The color scheme of the blocks, DUT (green), static control (gray), detector (yellow), Nallatech BenADDA-V4 card (blue), and actuator (red), corresponds with Fig. 1. In addition, the three different shades of purple in the dilution refrigerator (the purple box) indicate the temperature stages (4-K plate, 100-mK plate, and baseplate) to which the corresponding components are thermalized. The signal ports at the dilution refrigerator are labeled with letters in circles (*A*–*E*). The AWG 1 in the static control unit has four channels (CH 1–4) while the AWG 2 in the actuator has two channels (CH 1–2).

Fig. 5) are generated by AWG 1 and up-converted to microwave frequencies using an *I*-*Q* mixer driven by a LO signal from microwave generator MWG 1.

Readout of the qubit is realized by a pulsed measurement of the transmission of microwaves through a coplanar waveguide resonator (CPWR). The readout pulse is applied to the CPWR through the resonator drive line (port *B* in Fig. 5). The readout pulses are also generated by AWG 1. An *I*-*Q* mixer with a LO signal from MWG 2 allows for shaping the readout pulses which can be useful to achieve faster ringup and ringdown of the intracavity field [66,67]. In order to adjust the power range for the resonator drive, a variable attenuator is used at the rf output of the mixer.

The transmitted signal is directed through an isolator, a circulator, and a directional coupler to a JPA [51] based on a $\lambda/4$ resonator shunted with an array of superconducting quantum-interference device loops [52,53,56]. The isolators and circulators protect the DUT from pump leakage and thermal noise. The pump tone needed to achieve a gain of approximately 20 dB in the JPA is derived via splitters from the same microwave generator MWG 2 that is used for the readout pulses, which reduces drifts of relative phase between the two signals. Low phase noise is essential if the JPA is operated in a phase-sensitive mode [88,111]. The pump signal (port *E* in Fig. 5) is combined with the signal from the resonator through a directional coupler.

Both the signal and the pump tone are reflected from the JPA. To avoid saturation of the subsequent amplifiers, we destructively interfere the reflected pump tone with a cancellation tone applied to the directional coupler (port *D* in Fig. 5). The phase and amplitude of the cancellation tone are adjusted using a variable phase shifter and attenuator.

After amplification by the JPA, the signal is passed via isolators which attenuate reversely propagating radiation towards a high-electron-mobility transistor (HEMT) amplifier to further amplify the signal with a gain of 40 dB before it exits the dilution refrigerator (port *C* in Fig. 5).

In the detection electronics (the yellow box in Fig. 5) at room temperature, the signal is amplified further using low-noise microwave amplifiers. In order to reduce noise below the frequencies of interest, the signal is high-pass filtered with a cutoff frequency of about 4 GHz. The carrier frequency of, typically, 7 GHz is converted down to an intermediate frequency (IF) using an analog *I*-*Q* mixer and a separate microwave generator, MWG 3, for the LO signal. The IF signal at the *I* output of the mixer is further amplified using an IF amplifier, and low-pass filters are used to suppress noise outside the detection bandwidth of the ADC (50 MHz). Attenuators between the amplifiers and the mixer are used to suppress standing waves due to impedance mismatches and in order to prevent saturation of the mixer, the amplifiers, and the ADC.

After amplification and analog down-conversion, the signal is digitized by the ADC and forwarded to the FPGA on the Nallatech BenADDA-V4 card. The DSP circuit which we implemented on the FPGA generates a feedback trigger conditioned on the digitized and processed signal (see Sec. III).

The feedback trigger is forwarded to AWG 2, which is part of the actuator electronics (the red box in Fig. 5). When receiving the feedback trigger, AWG 2 generates a pulse which is up-converted to the qubit frequency, typically at 5 to 6 GHz, using an *I*-*Q* mixer and LO from microwave generator MWG 4. Bias tees allow us to compensate for unwanted dc offsets of the *I*-*Q* inputs of the mixer in order to suppress LO leakage. The up-converted microwave pulses are forwarded to the qubit (port *A* in Fig. 5).

All AWGs, MWGs, and ADC and DSP clocks are synchronized to a 10-MHz sine wave from an SRS FS725 rubidium frequency standard.

APPENDIX B: LATENCY OF ANALOG-TO-DIGITAL CONVERSION AND DIGITAL INPUT

The ADC latency and digital input-output latencies of the FPGA are inferred from the timing relative to the input trigger and the feedback trigger. When the variable delay in the state discrimination module (see Appendix C 4) is set to $d = 1$ clock cycle, we measure the delay from the trigger input to the feedback trigger with an oscilloscope at $\tau_{\text{tr-FBT}} = 110\ \text{ns} \pm 3\ \text{ns}$. Since the input trigger is synchronized with the digitized signal from the ADC in the DSP circuit, we infer that the ADC delay and digital input-output delay is $\tau_{\text{ADC,DIO}} = \tau_{\text{tr-FBT}} - \tau_{\text{proc}} = 80\ \text{ns} \pm 3\ \text{ns}$.

The delay $\tau_{\text{ADC,DIO}}$ has several contributors, which we do not determine individually. The pipelined architecture of the AD6645 ADC introduces a delay of four clock cycles (40 ns) and a latency of one additional clock cycle (10 ns) to transfer the digitized signal from the ADC to the FPGA, where it is registered in a synchronous *D* flip-flop. Further delays are expected to contribute to $\tau_{\text{ADC,DIO}}$ due to the routing of the digital signal on the BenADDA-V4 board as well as pad–to–flip-flop and flip-flop–to–pad delays on the FPGA (see Appendix D 1).

APPENDIX C: IMPLEMENTATION DETAILS OF DIGITAL SIGNAL PROCESSING BLOCKS

Here, we specify the implementation details of the blocks of the DSP circuit presented in Sec. III, which are relevant to the processing latency.

1. Digital mixer

The cosine and sine signals, $\cos(\omega_{\text{IF}} t_n)$ and $-\sin(\omega_{\text{IF}} t_n)$, for digital mixing are typically generated using either a lookup table with precomputed values or an iterative algorithm and then multiplied by two copies of the signal, as shown in Fig. 6(a). While these methods work for arbitrary frequencies ω_{IF}, a simplified method exists for the

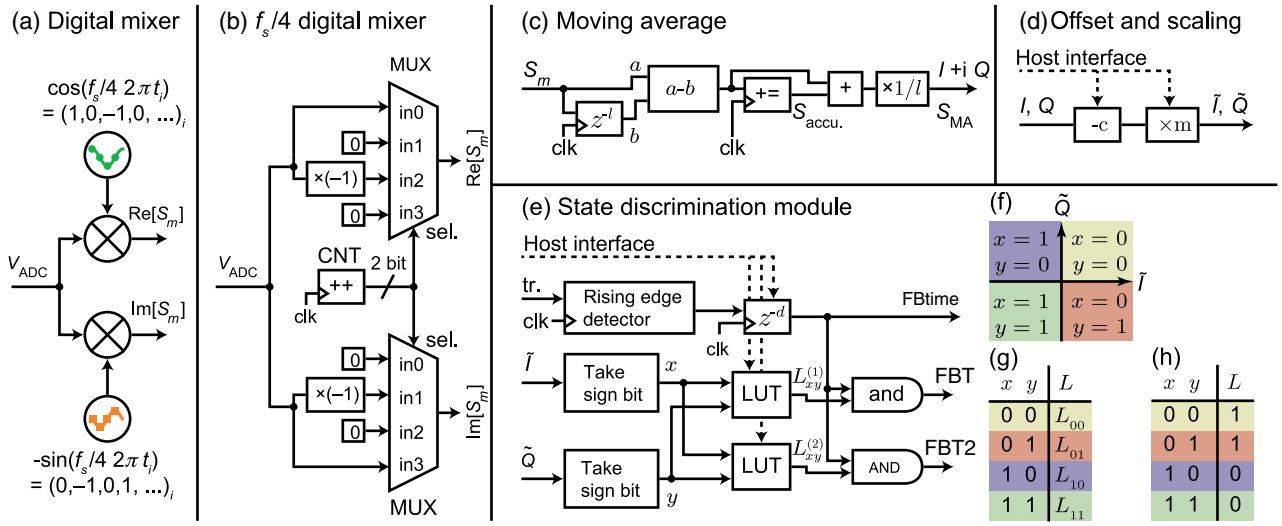

FIG. 6. Details of the blocks of the DSP circuit relevant to feedback generation. (a) Digital I-Q mixer implemented with multipliers (the circles with crosses). (b) Quarter sampling rate $f_s/4$ digital I-Q mixer implemented with multiplexers (MUXs) that forward one of their inputs to their output based on the selection (sel.). The sel. signal is driven by a repeating two-bit counter (CNT,++). (c) Moving average using an accumulator (+ =). (d) Circuit for offset subtraction and scaling. (e) Schematic of the logic circuit of the state discrimination module based on lookup tables (LUTs). (f) Representation of the plane spanned by the offset-subtracted in-phase ($\tilde{I}$) and quadrature ($\tilde{Q}$) signal components. The four quadrants are labeled with the corresponding values of the sign bits x and y. (g) Representation of one LUT based on the inputs x and y (the first two columns). The third column contains the symbolic value L_{xy} stored in the LUT for every combination of input bits x and y. (h) Specific example of how to fill in the LUT.

special case when ω_{IF} equals a quarter of the sampling rate, i.e., $\omega_{\mathrm{IF}}/(2\pi) = f_s/4$ [71,72].

In the $f_s/4$ case, the periodic sequences for the cosine and negative sine are simply $(1,0,-1,0)$ and $(0,-1,0,1)$, respectively [71]. Since multiplication by 0, 1 and -1 is trivial, we replace the multipliers by counter-driven multiplexers (MUXs) that periodically switch between four inputs, as shown in Fig. 6(b). The 2-bit repeating counter (CNT) iterates through a sequence of four values (0, 1, 2, 3), jumping to the next value in every clock cycle and restarting from 0 after it has reached 3. The output of the counter is forwarded to the selection (sel.) input of the MUXs. The selection input of the multiplexers determines which of the four inputs (in0, in1, in2, in3) of the multiplexers are forwarded to their output. The four inputs of the multiplexer for the real part ($\mathrm{Re}[S_m]$) correspond to multiplying the signal by $(1,0,-1,0)$, while the inputs of the multiplexer for the imaginary part ($\mathrm{Im}[S_m]$) correspond to multiplication by $(0,-1,0,1)$.

2. Moving average

In the following, we discuss how to implement the moving average [the circuit shown in Fig. 6(c)], which is the simplest type of FIR filter, with a processing latency of less than one clock cycle (10 ns). The moving average is applied in parallel to the real and imaginary parts of the output S_m of the mixer; i.e., two copies of the circuit shown in Fig. 6(c) are implemented, with outputs I and Q, respectively.

The first step in the circuit for computing the moving average, as shown in Fig. 6(c), is to fan out the input signal into two branches. One branch, b, is delayed by a variable delay (z^{-l}) of l clock cycles, while no operation is performed on the other branch, a; i.e., $b_m = a_{m-l}$. A subtractor then computes the difference $a-b$ between the values of the two branches, which is forwarded to an accumulator [+ = in Fig. 6(c)]. In every clock cycle, the accumulator adds the value at its input to the sum stored internally and forwards the updated sum to the output. Therefore, the output $S_{\mathrm{accu},n}$ at clock cycle n of the accumulator is the sum of all input samples up to clock cycle $n-1$; i.e.,

$$\begin{aligned} S_{\mathrm{accu},n} &\equiv \sum_{m=0}^{n-1}(a_m - b_m) = \sum_{m=0}^{n-1}(a_m - a_{m-l}) \\ &= \sum_{m=n-l}^{n-1} a_m + \underbrace{\sum_{m=0}^{n-l-1}(a_m - a_m)}_{=0} - \underbrace{\sum_{m=-l}^{-1} a_m}_{=0} \\ &= \sum_{m=n-l}^{n-1} a_m, \end{aligned} \tag{C1}$$

where the last equality holds assuming that all input samples with negative index are equal to zero; i.e., $a_m = 0$ for $m < 0$. To make sure that this assumption holds true, we initialize the registers of the variable delay and the

accumulator to zero. As depicted in Fig. 6(c), an additional adder (+) adds the most recent value of the difference $a_n - b_n$ at the input of the accumulator to its output, and a constant factor of $1/l$ normalizes the moving average. Thus, the final signal at the output of the moving-average module (S_{MA}) is

$$\begin{aligned} S_{\mathrm{MA,n}} &\equiv \frac{1}{l}(S_{\mathrm{accu},n} + a_n - b_n) \\ &= \frac{1}{l}\left(\sum_{m=n-l}^{n-1} a_m + a_n - a_{n-l}\right) \\ &= \frac{1}{l}\sum_{m=n-l+1}^{n} a_m. \end{aligned} \tag{C2}$$

As opposed to the sums in Eq. (C1), which stop at index $n-1$, the final sum in Eq. (C2) includes the most recent sample with index n, which shows that the additional adder reduces the effective processing latency to less than one clock cycle.

3. Preprocessing module

Offset subtraction [$-c$ in Fig. 6(d)] is implemented with lookup tables (LUTs). The parameter c is configurable via the interface with the host computer (indicated by the dashed arrows). The multiplication [$\times m$ in Fig. 6(d)] is implemented without the use of actual multipliers but rather uses bit shift units, which perform effective multiplications with powers of 2. Avoiding the allocation of multipliers reduces hardware resource consumption and leads to reduced processing latencies. The multiplication is made configurable using multiplexers to choose between different bit shift units. The bit shift unit is chosen via the host computer interface.

4. State discrimination module

The state discrimination module determines the qubit state and provides feedback triggers based on the sign bits x and y of the preprocessed signals $\tilde{I}$ and $\tilde{Q}$, as shown in Fig. 6(e). The sign bits of $\tilde{I}$ and $\tilde{Q}$ are 0 if the respective signal is positive and 1 if it is negative, as depicted in Fig. 6(f). Because of the prior offset subtraction, determining the sign bits of $\tilde{I}$ and $\tilde{Q}$ is equivalent to comparing the I and Q signals each to an arbitrary threshold value. Two LUTs define the binary feedback with two independent bits, $L_{xy}^{(1)}$ and $L_{xy}^{(2)}$, which are selected based on the two sign bits x and y, as depicted in Fig. 6(g). The entries of the LUT can be set via the host computer interface [the dashed arrows in Fig. 6(e)]. In the example shown in Fig. 6(h), the value of the feedback bit is 1 if and only if $x = 0$, corresponding to a non-negative value of the I component of the signal.

The input trigger signal is used as a reference for the timing of the feedback triggers relative to the onset of the readout pulse. As shown in Fig. 6(e), the trigger first enters a rising edge detector block. The output of the rising edge detector block is 1 if and only if the input binary value of the trigger is 0 in the previous clock cycle and 1 in the present clock cycle. The output of the rising edge detector is delayed with a variable delay z^{-d}, where d is the number of clock cycles (with each being 10 ns) corresponding to the readout time τ_{RO}, i.e., $d \times 10\ \mathrm{ns} = \tau_{\mathrm{RO}}$. The parameter d can be set via the host computer interface. The output of the variable delay, which we refer to as the FBtime marker, marks the specific time at which the feedback pulse is provided. To ensure that the feedback triggers are issued at the correct time, the feedback triggers FBT and FBT2 are based on the AND operation of the output of the LUT and the FBtime marker.

5. Histogram module

The histogram module is important for assessing the feedback performance and for calibrating the experimental setup. Here, we explain how our multidimensional histogram module is implemented. The histogram module has different operational modes. We first introduce the circuit for recording two-dimensional histograms, as shown in Fig. 7(a). The input signals $\tilde{I}$ and $\tilde{Q}$ are rounded to 7-bit fixed-point numbers, which means that the full range of ± 1 V is subdivided into $2^7 = 128$ bins. The 7-bit fixed-point representations of $\tilde{I}$ and $\tilde{Q}$ are concatenated into a 14-bit address of the histogram bin which stores the number of occurrences of the combination of values $(\tilde{I}, \tilde{Q})$. The "increase count" block manages the communication with the ZBT RAM in order to increase the stored count whenever the enable flag (en.) is active. For feedback experiments, the enable flag is derived from the FBtime marker such that the histogram is updated when the feedback decision is made (see Sec. III).

In the correlation mode of our histogram module, a buffer [Fig. 7(b)] stores the value of $\tilde{I}$ at every reception of the FBtime marker. The buffered signal $\tilde{I}_1$ is combined with the most recent signal $\tilde{I}_2$ to record the probability of observing a specific combination $\tilde{I}_1$ and $\tilde{I}_2$ in two consecutive readouts (see Sec. IV). In addition, a segment counter [seg. cnt in Fig. 7(b)] allows us to distinguish alternating experimental scenarios, such as when the feedback is enabled or disabled alternately in consecutive runs of the experiment. In the correlation mode, the value of $\tilde{Q}$ is, in principle, not needed, but it is an additional piece of useful information. In order to make use of the total amount of 2^{25} bits (4 MB) available space in the ZBT RAM, we reduce the Q dimension to 5 bits and concatenate the values ($\tilde{I}_2$, $\tilde{Q}$, $\tilde{I}_1$, seg.) into a 21-bit address with a word size of 16 bits to store the counts as presented in Fig. 7(b).

In the time-resolved mode, a time counter [time cnt in Fig. 7(c)] is used to add time as an additional dimension of the histogram. The time counter starts upon the reception of the FBtime marker, and the enable flag is held active for up

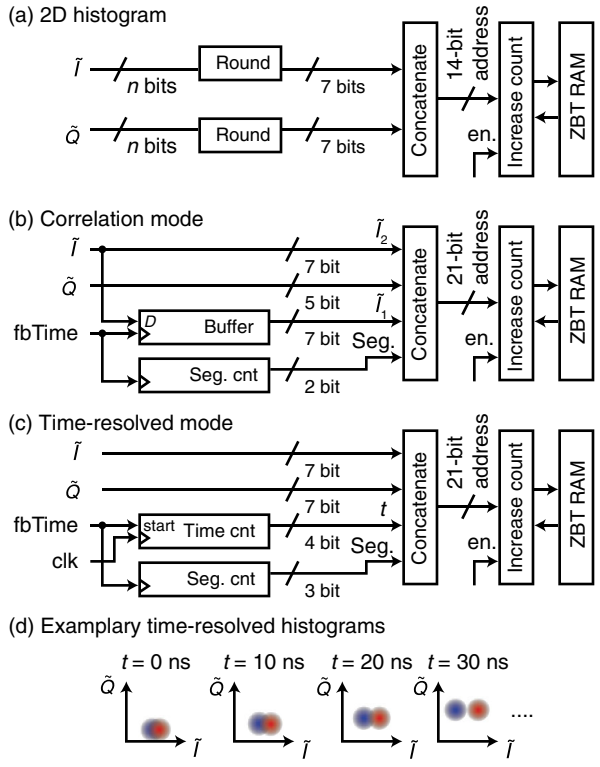

FIG. 7. (a) Sample circuit for recording two-dimensional histograms whose dimensions are the preprocessed 7-bit signals $\tilde{I}$ and $\tilde{Q}$. See the text for details. (b) Correlation mode with buffer and segment counter (seg. cnt). For simplicity, the rounding steps are not shown here. (c) Time-resolved mode with a time counter (time cnt). For simplicity, the rounding steps are not shown here. (d) Illustration of exemplary time-resolved histograms of the $\tilde{I}$ and $\tilde{Q}$ values at four consecutive times t when the qubit state is $|g\rangle$ (blue) or $|e\rangle$ (red).

to 16 clock cycles. As for the correlation mode, there is a segment counter [seg. cnt in Fig. 7(c)] which allows us to discern different consecutive scenarios, such as when the qubit is prepared in the $|g\rangle$ or $|e\rangle$ state alternately. This segmentation makes the time-resolved mode useful for calibration tasks such as finding the optimal qubit readout time by observing the separation of the distributions of the I and Q values for the states $|g\rangle$ [the blue histogram in Fig. 7(d)] and $|e\rangle$ [the red histogram in Fig. 7(d)] over time.

APPENDIX D: FPGA TIMING AND RESOURCE ANALYSIS

1. FPGA timing analysis

Using the Xilinx ISE® tool suite [112], we extract information about the timing of the signal processing for our present implementation of the DSP circuit in the Virtex-4 (xc4vsx35-10ff668), and for future implementations on the Virtex-6 (xc6vlx240t-1ff1156) and Virtex-7 (xc7vx485t-2ffg1761c) FPGAs. In Appendix D 2, we present the corresponding FPGA resource allocations.

TABLE II. Summary of the simulated FPGA timings: the pad-to-pad delay $\tau_{\text{p-p}}$ from the data input to the feedback trigger output, the processing time τ_{proc}, the chosen clock period τ_{clk}, the minimum clock period $\tau_{\text{clk,min}}$ and the maximum clock frequency f_{max}. See the text for details.

	$\tau_{\text{p-p}}$ (ns)	τ_{proc} (ns)	τ_{clk} (ns)	$\tau_{\text{clk,min}}$ (ns)	f_{max} (MHz)
V-4 full	35.3	30	10	6.7	149
V-4 core	20.7	10	9.7	9.7	103
V-6 core	14.7	6.2	6.2	6.2	161
V-7 core	14.3	5.3	5.3	5.3	188

We define the pad-to-pad delay $\tau_{\text{p-p}}$ as the delay that the digitized signal encounters in the path from the signal input pads of the FPGA to the feedback trigger output pad. For the full implementation on the Virtex-4 FPGA ("V-4 full" in Table II), the predicted pad-to-pad delay amounts to

$$\begin{aligned}\tau_{\text{p-p}} &\equiv \tau_{\text{p-f}} + \tau_{\text{proc}} + \tau_{\text{f-p}} \\ &= 1.5\ \text{ns} + 30\ \text{ns} + 3.8\ \text{ns} = 35.3\ \text{ns}, \end{aligned} \quad \text{(D1)}$$

where $\tau_{\text{proc}} = 30$ ns is the processing latency of three pipeline stages (see the blue dashed lines in Fig. 2). Moreover, the pad–to–flip-flop delay $\tau_{\text{p-f}} = 1.5$ ns is the maximum delay from the ADC input pads to the D flip-flops of the first pipelined register. Furthermore, the flip-flop–to–pad delay $\tau_{\text{f-p}} = 3.8$ ns is the maximum delay from the flip-flops of the last pipelined register to the output pad of the feedback trigger. The pad–to–flip-flop $\tau_{\text{p-f}}$ and flip-flop–to–pad $\tau_{\text{f-p}}$ delays are expected to contribute to the digital input and output delay $\tau_{\text{ADC,DIO}}$ (see Sec. II D).

A clock period analysis shows that the minimum clock period due to the timing of the signals between two pipelined registers amounts to $T_{\text{min}} = 6.7$ ns, which corresponds to a maximum clock frequency of $f_{\text{max}} = 149$ MHz. Increasing the clock frequency in a pipelined architecture is, however, beneficial only when the sampling rate of the ADC is also increased. Instead removing pipeline stages in the signal path can lead to a further decrease in processing time, as long as the minimal clock period is larger than the sampling period; i.e., $T_{\text{min}} \geq 1/f_s$.

As a first step towards a future optimization of the processing and pad-to-pad delay, we separately simulate the implementation of what we consider to be the core feedback functionality of the DSP circuit, which includes only the $f_s/4$ mixer, the moving average, the offset subtraction and scaling modules, and the state discrimination module. For the implementation of the core DSP circuit, we keep only two pipelined registers, one at the ADC input and one at the feedback outputs FBT and FBT2. Therefore, the processing latency amounts to one clock cycle. In order to optimize the pad-to-pad delay, we first optimize the register-to-register delay, which determines the maximal clock frequency. Afterwards, we optimize the

pad-to-register and register-to-pad delays. Assuming that the sampling rate is equal to the maximal clock frequency, we obtain a pad-to-pad delay of 4 ns + 9.7 ns + 7 ns = 20.7 ns [cf. Eq. (D1)] for the Virtex-4 implementation, 3 ns + 6.2 ns + 5.5 ns = 14.7 ns [cf. Eq. (D1)] for the Virtex-6 implementation ("V-6 core" in Table II), and 4 rmns + 5.3 ns + 5 ns = 14.3 ns for the Virtex-7 implementation ("V-7 core" in Table II). These results show that a further reduction of the latency introduced by the DSP from 35.3 to 14.3 ns is possible with an optimized implementation of the core functionalities and by using a recent FPGA. We therefore consider the integration of a recent FPGA into our experimental setup a possibility for future work.

2. FPGA resource analysis

Here, we report the FPGA resource allocation for the full design implemented on the Virtex-4 FPGA and compare it to the resources needed to implement the core functionality consisting of the $f_s/4$ mixer (Appendix C 1), the moving average (Appendix C 2), the preprocessing module (Appendix C 3), and the state discrimination module (Appendix C 4). The analysis of the resource allocation is done for the implementation of the core design on the Virtex-4, Virtex-6, and Virtex-7 FPGAs corresponding to the timing analysis performed in Appendix D 1.

The resource usage is summarized in Table III. The full design (V-4 full) uses $n_{DFF} = 15\,312$ D flip-flops corresponding to 49% of the total number of D flip-flops and $n_{LUT} = 18\,361$ four-input LUTs, which is 59% of the available LUTs on the Virtex-4 FPGA. The majority of the resources in the full design are consumed by the flexibility in signal processing, such as the phase-adjustable mixer and the FIR filter with arbitrary coefficients and the possibility of recording histograms. In addition, the full design includes hardware modules for interfacing with the host computer and ZBT memory. To implement the added flexibility in the signal processing, the full design requires $n_{DSP} = 184$ dedicated DSP slice resources, which contain multipliers and adders.

The core design (V-4 core, V-6 core, and V-7 core in Table III) implements only a subset of the functionality to maintain the minimal requirements for the DSP operations. Therefore, the number of D flip-flops n_{DFF} and LUTs n_{LUT} is reduced by almost 2 orders of magnitude compared to the full implementation. In addition, the implementation of the core functionality does not require dedicated DSP slices of the FPGA (n_{DSP} in Table III) since no multipliers are used in the blocks of the core design. The numbers n_{DFF} and n_{LUT} vary depending on whether the core design is implemented for the Virtex-4 (V-4 core), Virtex-6 (V-6 core), or Virtex-7 (V-7 core) FPGA, as displayed in Table III. We ascribe the variations in resource usage among the implementations of the core design to differences in the slice and LUT structure among the respective FPGA models. Different slice and LUT structures result in differences in resource optimization in the mapping process using the Xilinx ISE software.

TABLE III. FPGA resource summary specifying the allocated number of D flip-flops n_{DFF}, the number of LUTs n_{LUT}, and the number of dedicated DSP slice resources n_{DSP}. Percentages are relative to the total amount of resources on the corresponding FPGA. See the text for details.

	n_{DFF}	(Relative)	n_{LUT}	(Relative)	n_{DSP}	(Relative)
V-4 full	15 312	(49%)	18 361	(59%)	184	(95%)
V-4 core	361	(1%)	535	(2%)	0	
V-6 core	372	(<1%)	369	(<1%)	0	
V-7 core	371	(<1%)	509	(<1%)	0	

APPENDIX E: EXPERIMENTAL PARAMETERS

The superconducting transmon qubit [45] has a resonance frequency $\omega_q/(2\pi) = 6.148$ GHz corresponding to the transition between the ground and first excited states, and an anharmonicity of $\alpha = -401$ MHz. The qubit is capacitively coupled to a $\lambda/2$ coplanar waveguide resonator with a coupling strength $g/(2\pi) \approx 65$ MHz. We measure a fundamental mode resonance frequency of $\omega_r/(2\pi) = 7.133$ GHz, which is defined as the center of the dispersively shifted resonance frequencies for the qubit states $|g\rangle$ and $|e\rangle$. We measure a linewidth of $\kappa/(2\pi) = 6.3$ MHz of the resonator. The qubit shows an exponential energy relaxation with time constant $T_1 \approx 1.4$ μs. We choose an experiment repetition period of 10 μs, which, for the given T_1, is sufficient to obtain a residual out-of-equilibrium excited-state population of 0.1%. The measured thermal equilibrium excited-state probability is $P_{\text{therm}} \approx 7\%$ (see Appendix F).

The envelope of the microwave pulses for qubit rotations is Gaussian with $\sigma = 7$ ns, truncated symmetrically at $\pm 2\sigma$, as seen in the pulse scheme Fig. 4(b), and it uses the DRAG technique [75,113] to avoid errors due to the presence of states outside the qubit subspace.

From pulsed spectroscopy, we observe a dispersive shift of the resonator frequency $\omega_r^{|g\rangle(|e\rangle)}$ for the qubit in the ground $|g\rangle$ or excited state $|e\rangle$ of

$$2\chi \equiv \omega_r^{|e\rangle} - \omega_r^{|g\rangle} = -2.2 \text{ MHz} \times 2\pi. \tag{E1}$$

We choose the frequency of the resonator drive pulses for dispersive readout at the center between the two shifted resonator frequencies; i.e., $\omega_r \equiv (\omega_r^{|e\rangle} + \omega_r^{|g\rangle})/2$. The amplitude of the readout pulse is chosen such that the expected steady-state mean photon number is $\langle n \rangle_{\text{readout}} \approx 10$, which we calibrate by measuring the ac Stark shift [114] of the qubit frequency when a continuous coherent drive is applied to the resonator.

APPENDIX F: REDUCTION OF THERMAL EXCITED-STATE POPULATION

A possible application of active feedback initialization is to temporarily reduce the excited-state population when the qubit is initially in thermal equilibrium with its environment [19,90,92]. In order to test the performance of our feedback loop for reducing the thermal excited-state population, we omit the $\pi/2$ pulse at the beginning of the protocol presented in Sec. IV, such that the expected input state is a mixed state described by the density matrix

$$\rho_{\text{therm}} \equiv (1 - P_{\text{therm}})|g\rangle\langle g| + P_{\text{therm}}|e\rangle\langle e|, \qquad \text{(F1)}$$

where P_{therm} is the excited-state population when the system is in thermal equilibrium with its environment.

As discussed in Sec. IV, the qubit state is measured by two successive readout pulses, $M1$ and $M2$. When the feedback actuator is disabled, the measured histogram of the in-phase component I_1 of the signal during $M1$ (the blue dots in Fig. 8(a)] is almost identical to the histogram of the in-phase component I_2 of the signal during $M2$ [the orange dots in Fig. 8(a)). By counting the values on the right side of the threshold [the dashed line in Fig. 8(a)], we obtain the corresponding thermal excited-state probabilities of $\mathbb{P}[E_1]_{\text{FB off}} = 8.21(2)\%$ for the first measurement, $M1$, and $\mathbb{P}[E_2]_{\text{FB off}} = 8.18(2)\%$ for the second measurement, $M2$. The approximate equality of these two probabilities indicates that, regardless of the measurement outcome, the measurement leaves the thermal steady state ρ_{therm} unperturbed. Note that the overlap readout error (see Appendix G) biases the measured probabilities towards 50%. Taking this bias into account, we infer a thermal excited-state population of $P_{\text{therm}} \approx 7\%$ from the measured probabilities $\mathbb{P}[E_1]$ and $\mathbb{P}[E_2]$. The inferred thermal excited-state population P_{therm} corresponds to a temperature of a bosonic environment of $T_{\text{env}} \approx 114$ mK. The effective temperature T_{env} is close to the measured base temperature of the dilution refrigerator, which, for the presented experiment, is 90 mK instead of the typical temperature of 20 mK due to problems with the cryogenic setup.

When feedback is enabled, the excited-state probability in the second measurement amounts to $\mathbb{P}[E_2]_{\text{FB on}} = 5.43(2)\%$, as obtained from the histogram of I_2 [the orange dots in Fig. 8(b)], and is reduced compared to the excited-state probability in the first measurement $\mathbb{P}[E_1]_{\text{FB on}} = 8.29(2)\%$ obtained from the histogram of I_1 [the blue dots in Fig. 8(b)], showing that a reduction of the thermal excited-state population is possible with our feedback loop. The measured probability $\mathbb{P}[E_2]_{\text{FB on}}$ is in reasonably good agreement with the simulated value of $\mathbb{P}[E_2]_{\text{FB on,sim}} = 5.24\%$ obtained from a master-equation simulation using the same model and parameters as discussed in Sec. IV.

We record two-dimensional histograms of the values I_1 and I_2 for the case when feedback is disabled and enabled as shown in Figs. 8(c) and 8(d), respectively. The measured

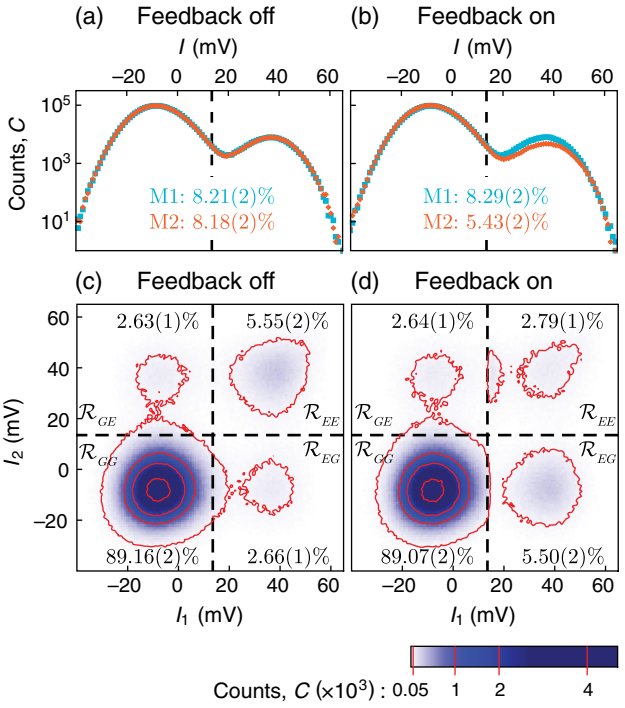

FIG. 8. Same type of histograms as presented in Fig. 4 for the scenario where the initial $\pi/2$ pulse is omitted. (a) Histograms of the in-phase signal in the first measurement I_1 (the blue dots) and second measurement I_2 (the orange dots) when feedback is disabled. The dashed line marks the feedback threshold. Percentages are the summed counts of occurrences above the threshold relative to the total count $C_{\text{tot}} = 2\,097\,152$ for the signals in $M1$ and $M2$, respectively. (b) The same type of histograms as in (a) but with feedback enabled. (c) Two-dimensional histogram with 128×128 bins as a function of the in-phase signal in the first measurement I_1 versus the in-phase signal in the second measurement I_2 with feedback disabled. The red lines are contour lines marking specific counts of $\{0.05, 1, 2, 4\} \times 10^3$. In each region ($\mathcal{R}_{GG}$, $\mathcal{R}_{GE}$, $\mathcal{R}_{EG}$, and $\mathcal{R}_{EE}$) separated by the threshold (the dashed lines), the percentage of counts relative to the total count is indicated. (d) The same type of two-dimensional histogram as in (c) but with feedback enabled.

relative counts in the four regions ($\mathcal{R}_{GG}$, $\mathcal{R}_{GE}$, $\mathcal{R}_{EG}$, and $\mathcal{R}_{EE}$) of the two-dimensional histograms show the swapping of the probabilities $\mathbb{P}[\mathcal{R}_{EG}]$ and $\mathbb{P}[\mathcal{R}_{EE}]$ and the invariance of the probabilities $\mathbb{P}[\mathcal{R}_{GG}]$ and $\mathbb{P}[\mathcal{R}_{GE}]$ under the feedback action discussed in Sec. IV. The histogram of the signal in the region $\mathcal{R}_{EG}$ for the "feedback off" case [Fig. 8(c)] matches well with the histogram in region $\mathcal{R}_{EE}$ for the "feedback on" case [Fig. 8(d)]. Specifically, the corresponding probabilities $\mathbb{P}[\mathcal{R}_{EG}]_{\text{FB off}} = 2.66(1)\%$ and $\mathbb{P}[\mathcal{R}_{EE}]_{\text{FB on}} = 2.79(2)\%$ match reasonably well, which shows that the feedback pulse is applied when the state $|e\rangle$ is detected in the first measurement. The experimentally observed probabilities are in reasonably good agreement with the simulation results $\mathbb{P}[\mathcal{R}_{EG}]_{\text{FB off,sim}} = 1.98\%$ and

TABLE IV. Experimental and simulated probabilities $\mathbb{P}[\mathcal{R}_{xy}]$ of the events for observing the qubit in state x in the first measurement and in state y in the second measurement when the feedback is either disabled or enabled. The simulated values are obtained from a master-equation simulation. See the text for details.

	Feedback off		Feedback on	
	Experimental	Simulated	Experimental	Simulated
$\mathbb{P}[\mathcal{R}_{GG}]$	89.16(2)%	88.01%	89.07(2)%	88.01%
$\mathbb{P}[\mathcal{R}_{GE}]$	2.63(1)%	3.79%	2.64(1)%	3.79%
$\mathbb{P}[\mathcal{R}_{EG}]$	2.66(1)%	1.98%	5.50(2)%	6.75%
$\mathbb{P}[\mathcal{R}_{EE}]$	5.55(2)%	6.22%	2.79(1)%	1.45%

$\mathbb{P}[\mathcal{R}_{EE}]_{\text{FB on,sim}} = 1.45\%$ (Table IV) considering the sources of systematic errors discussed in Sec. IV. We observe that the histogram in the region $\mathcal{R}_{EE}$ in Fig. 8(d) is double peaked, which is a consequence of the readout error since the tail of the distribution associated with the $|g\rangle$ state extends into the region $\mathcal{R}_{EG}$.

Furthermore, the histograms in the region $\mathcal{R}_{GE}$ match for both the feedback off [Fig. 8(c)] and the feedback on case [Fig. 8(d)]. The probabilities of $\mathbb{P}[\mathcal{R}_{GE}]_{\text{FB off}} = 2.63(1)\%$ and $\mathbb{P}[\mathcal{R}_{GE}]_{\text{FB on}} = 2.64(1)\%$ agree within the statistical error bars, which shows that the feedback pulse is not applied when the state $|g\rangle$ is detected in the first measurement.

The data presented here serve as a further experimental benchmark of our implementation of the feedback scheme and illustrate the use of two-dimensional histograms to provide insight into processes that lead to the observed excited-state probabilities.

APPENDIX G: READOUT FIDELITY

The readout is calibrated in a separate calibration step where either no pulse or a π pulse is applied to the qubit prior to the measurement. A threshold check, as described in Sec. II A, leads either to the result G corresponding the qubit state $|g\rangle$ or E corresponding to $|e\rangle$. The single-shot readout fidelity is defined as

$$F_r = 1 - \mathbb{P}[E|\text{“no pulse”}] - \mathbb{P}[G|\text{“}\pi\text{ pulse”}], \qquad \text{(G1)}$$

where $\mathbb{P}[E|\text{no pulse}]$ represents the conditional probability of obtaining the result E when no pulse is applied, whereas $\mathbb{P}[G|\pi\,\text{pulse}]$ represents the conditional probability of obtaining the result G when a π pulse is issued. For a fixed moving-average window length of $l = 4$ digital samples (40 ns), the single-shot fidelity reaches a maximal value of $F_r = 77\%$ at time $\tau_{\text{RO}} \approx 105$ ns relative to the onset of the readout pulse. We expect the contributions to the readout infidelity to be

$$1 - F_r \approx 2P_{\text{therm}} + P_{\text{decay}} + P_{\text{overlap}}, \qquad \text{(G2)}$$

where $P_{\text{therm}} \approx 7\%$ is the initial excited-state population in thermal equilibrium (see Appendix F), $P_{\text{decay}} \approx 1 - \exp(-\tau_{\text{RO}}/T1) \approx 6\%$ is the error due to the decay of the $|e\rangle$ state, and $P_{\text{overlap}} \approx 3\%$ is the probability of misidentification of the qubit state due to the overlap of the probability density functions for the signals corresponding to the $|g\rangle$ and $|e\rangle$ states. We extract the contributions to the readout infidelity from fits to recorded histograms using methods similar to the ones described in Ref. [44].

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