Impact of Silicon Doping on Low-Frequency Charge Noise and Conductance Drift in $GaAs/Al_xGa_{1-x}As$ Nanostructures

S. Fallahi,[1,2,*] J. R. Nakamura,[1,2] G. C. Gardner,[2,3,4] M. M. Yannell,[5] and M. J. Manfra[1,2,3,4,5,†]

[1]*Department of Physics and Astronomy, Purdue University, West Lafayette, Indiana 47907, USA*
[2]*Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907, USA*
[3]*School of Materials Engineering, Purdue University, West Lafayette, Indiana 47907, USA*
[4]*Station Q Purdue, Purdue University, West Lafayette, Indiana 47907, USA*
[5]*School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, USA*

(Received 17 September 2017; revised manuscript received 7 December 2017; published 13 March 2018)

We present measurements of low-frequency charge noise and conductance drift in modulation-doped $GaAs/Al_xGa_{1-x}As$ heterostructures grown by molecular beam epitaxy in which the silicon doping density is varied from 2.4×10^{18} (critically doped) to 6.0×10^{18} cm^{-3} (overdoped). Quantum point contacts are used to detect charge fluctuations. A clear reduction of both short-time-scale telegraphic noise and long-time-scale conductance drift with decreased doping density is observed. These measurements indicate that the *neutral* doping region plays a significant role in charge noise and conductance drift.

DOI: 10.1103/PhysRevApplied.9.034008

I. INTRODUCTION

Semiconductor nanostructures such as quantum dots and quantum point contacts (QPCs) are essential building blocks of mesoscopic devices used to realize solid-state qubits [1–5]. Molecular beam epitaxy (MBE) growth is a mature technology for growing extremely pure $GaAs/Al_xGa_{1-x}As$ two-dimensional electron gases (2DEGs) with minimal defects. Nevertheless, devices with metallic Schottky gates fabricated on $GaAs/Al_xGa_{1-x}As$ heterostructures often suffer from $1/f$-like noise and random telegraph noise (RTN) which degrade device performance and may preclude stable device operation. Low-frequency noise is believed to arise from time-dependent fluctuations in the occupation of charge trapping sites in the vicinity of the nanostructure that result in fluctuations of the local electrostatic potential. The etiology and the dynamics of these charge trapping sites are not fully understood.

Low-frequency charge noise was observed in early experiments on QPCs in $GaAs/Al_xGa_{1-x}As$ heterostructures [6–9], and it has continued to be a problem for mesoscopic devices ever since [10–15]. Several different techniques have been tried to combat noise. Bias cooling has been used to reduce charge noise by reducing the required voltage on the gates [10,11]. Similarly, charge noise has been reduced in QPCs by including a global top gate, which reduces the amount of negative voltage required to operate the QPCs [11]. Charge noise has been suppressed by etching the heterostructure underneath the metal gates, which also reduces the gate voltage required [13]. The insertion of an insulator between the metal gates and the substrate can potentially reduce charge noise by suppressing current leakage from the metal gate [1]. In an alternative approach, undoped heterostructures have been used for mesoscopic devices, in which the 2DEG is induced by applying positive bias to a global gate rather than by ionized donors [14,15]; this scheme may also help form stable quantum dots. These studies suggest that current leakage from the gates plays a significant role in the generation of low-frequency charge noise. However, while all of these techniques are palliative, they do not provide insight into the underlying states in the heterostructure that give rise to low-frequency charge noise.

A second problem frequently afflicting gated GaAs heterostructures is drift in device conductance over long time scales upon initial cooldown to cryogenic temperatures. This drift makes operating mesoscopic devices difficult, requiring frequent retuning. Conductance drift has not been studied as extensively as short-time-scale charge noise. In this work, we systematically investigate the relationship between modulation-doping density and both low-frequency charge noise and drift in device conductance. Both conductance drift and charge noise are shown to depend strongly on the density of silicon doping. We discuss the underlying mechanisms; our results will inform future designs of quiet semiconductor platforms for quantum-information research.

II. EXPERIMENT

In order to study the effect of doping concentration on low-frequency charge noise, modulation-doped $GaAs/Al_{0.36}Ga_{0.64}As$ heterostructures with three different silicon doping densities, N_D, 2.4×10^{18} cm^{-3} (wafer *A*), 4.2×10^{18} cm^{-3} (wafer *B*), and 6.0×10^{18} cm^{-3} (wafer *C*), are investigated. These uniformly doped single-interface

*sfallahi@purdue.edu
†mmanfra@purdue.edu

TABLE I. Characteristics of the studied wafers, including Si doping concentration N_D, doping width W, 2DEG density n, mobility μ, operating gate voltage V_g, number of QPCs measured, and Ohmic contact resistance for each wafer. The size of each Ohmic contact is $150 \times 150\ \mu m^2$.

Wafer name	N_D (cm^{-3})	W (nm)	n (cm^{-2})	μ ($cm^2/V\,s$)	V_g (V)	No. of QPCs measured	Ohmic contacts (Ω)
Wafer *A*	2.4×10^{18}	14.5	1.1×10^{11}	2.7×10^6	−0.5	6	140
Wafer *B*	4.2×10^{18}	14.5	1.3×10^{11}	5.1×10^6	−0.6	3	60
Wafer *C*	6.0×10^{18}	14.5	1.4×10^{11}	4.7×10^6	−0.6	6	50

heterostructures are grown by MBE with a 60-nm thick $Al_{0.36}Ga_{0.64}As$ spacer between the 2DEG and the doping region (14.5 nm thick) and a total 90-nm 2DEG depth measured from the top surface. An overview of the sample parameters is given in Table I. We note that the heterostructure design of wafer *B* is frequently implemented to fabricate spin qubits, and recent advances in two-qubit gate operation have been made with this design [2]. In Fig. 1, we show the conduction-band profile for wafer *B* simulated using the NEXTNANO software package [16]. We also show the ionized donor density for wafers *A*, *B*, and *C*.

Three distinct regions exist in the doping layer for each wafer: (1) a positively charged region closer to the cap layer that compensates for surface states and produces a Schottky barrier $eV_b \sim 0.8$ eV at the surface; (2) a neutral region in the middle of the doping layer, where the Fermi level is located at an energy $E_D \sim 150$ meV [17,18] below the conduction-band edge; and (3) a thin (<1 nm) positively ionized layer from which electrons have been transferred to the 2DEG. Microscopically, the neutral region is believed to be composed of positively and negatively charged Si donors with almost the same concentration. According to the negative-*U* model proposed independently by Chadi and Chang [18] and Khachaturyan *et al.* [19], the substitutional Si donor in $Al_xGa_{1-x}As$ (for an Al mole fraction where $x > 0.2$) occupying a Ga site has two possible electronic states: (1) a shallow donor level E_d with no lattice relaxation and (2) a deep and localized donor level

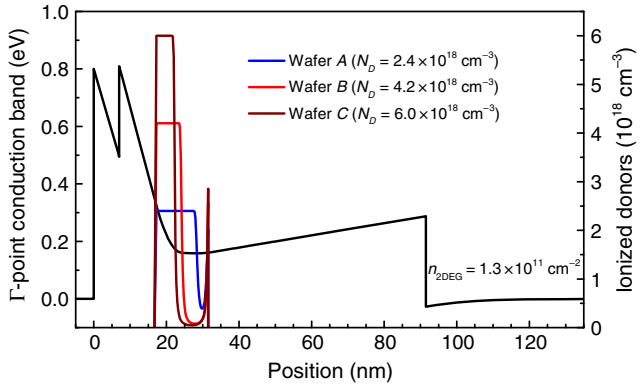

FIG. 1. Simulated heterostructure band diagram for a uniformly doped single-interface heterojunction with a varying doping density. Colored solid lines indicate the ionized donor profile for each doping concentration.

E_{DX^-} with large lattice relaxation which binds two electrons. Based on the negative-*U* model, half of the donors in the neutral region are positively charged (ionized) shallow d^+ states, and the remaining half are negatively charged DX^- states.

Importantly for our experiments, the doping width is kept constant at 14.5 nm for the three wafers, *A*, *B*, and *C*; only the silicon doping density is varied. As the charge transfer to the 2DEG is determined by the constant conduction-band offset and setback, an increase in doping density does not significantly change the 2DEG density or the charge transferred to the surface. Rather, the width of the neutral region increases, as is seen by comparing the blue, red, and brown traces in Fig. 1. Wafer *A* is close to critical doping (meaning that nearly all dopants are positively ionized); if the doping is exactly critical, there is no neutral region. At the other extreme, wafer *C* is significantly overdoped and has a large neutral region. Owing to the presence of DX^- centers, the electrons in this neutral region can be frozen at low temperatures (below 100 K) [20,21]; no parallel conduction is observed in magnetotransport measurements (not shown). It has been experimentally found that doped $GaAs/Al_xGa_{1-x}As$ heterostructures in which DX^- centers form exhibit lower charge noise than structures without DX^- centers [11]. Additionally, we observe that, after brief illumination with a red light-emitting diode at $T = 4.2$ K, the 2DEG density of these structures increases significantly. This persistent photoconductivity is a signature of DX^- centers and confirms that our heterostructures are doped in the regime in which DX^- centers form; however, all of our charge-noise measurements are performed without any illumination.

It is noteworthy that the mobility of wafer *A* is nearly a factor of 2 lower than the mobilities of wafers *B* and *C*. It has been shown that a correlation between the positively ionized d^+ states and negatively ionized DX^- states results in a significant enhancement of mobility in overdoped structures [22,23]; however, nearly all of the donors must be positively ionized in wafer *A*. Thus, no correlation is possible for this wafer, resulting in lower mobility.

We utilize QPCs as charge sensors to detect charge noise. QPCs with a nominal width of 300 nm are fabricated on all wafers using identical fabrication procedures to compare the level of charge noise for each wafer. A SEM image of a typical QPC is shown in the inset to Fig. 2. The processing steps are as follows: (1) photolithography of

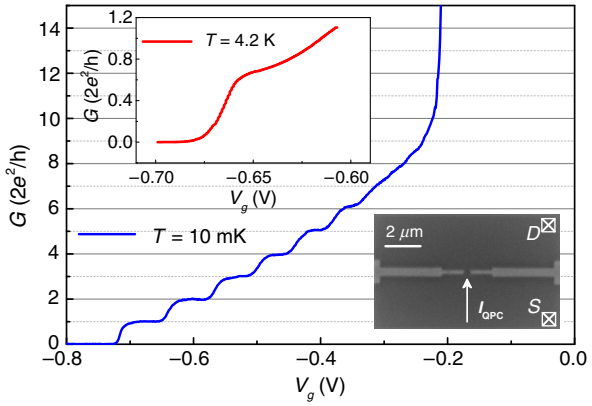

FIG. 2. Conductance G of a QPC as a function of the gate voltage V_g at $T = 10$ mK. (Top inset) First riser of QPC conductance at $T = 4.2$ K. (Bottom inset) SEM image of a fabricated QPC on wafer B.

mesa pattern and mesa etch; (2) photolithography of Ohmic contacts, evaporation of Ni/Au/Ge metal contacts, and annealing; (3) electron-beam lithography and evaporation of QPC gates with a Ti/Au (10 nm/25 nm) metal stack; and (4) photolithography and evaporation of bonding pads to wire bond devices to a chip carrier for measurement.

Figure 2 shows a typical conductance plot of a QPC as a function of gate voltage V_g taken in a dilution refrigerator with a mixing-chamber-plate temperature of $T = 10$ mK; the conductance is quantized in units of $2e^2/\mathrm{h}$ corresponding to discrete conductance modes of the device. Bias cooling is not employed in any of our experiments. The gate voltage required to deplete the 2DEG beneath the gates is essentially identical for all of the studied wafers and is equal to -185 mV. The geometric capacitance between the gate and 2DEG is $C = \epsilon_0\epsilon_r/d$ per unit area, where d equals the 2DEG depth beneath the top surface. Assuming only the coupling between the gate and 2DEG, we calculate the depletion gate voltage $V_{\mathrm{dep}} = en/C = -180$ mV for $n = 1.3 \times 10^{11}$ cm^{-2}. This nearly perfect agreement implies that charges in the neutral region do not respond to gate voltage and are frozen at low temperature. The top inset of Fig. 2 shows the first riser in QPC conductance at $T = 4.2$ K, where we operate the devices for noise measurements. At $T = 4.2$ K, the QPC still has very high transconductance on the riser of the first quantized conductance plateau, making it very sensitive to the position of individual charges in the vicinity of the device. We use a two-terminal measurement in which a 200-μV dc voltage bias is applied to the source contact, and the drain current is measured with a DL1211 current preamplifier; the output is fed to a National Instruments NI-DAQ digitizer.

III. RESULTS

A. Short-time-scale conductance fluctuations

The most striking observation of our work is the dramatic increase in low-frequency noise associated with

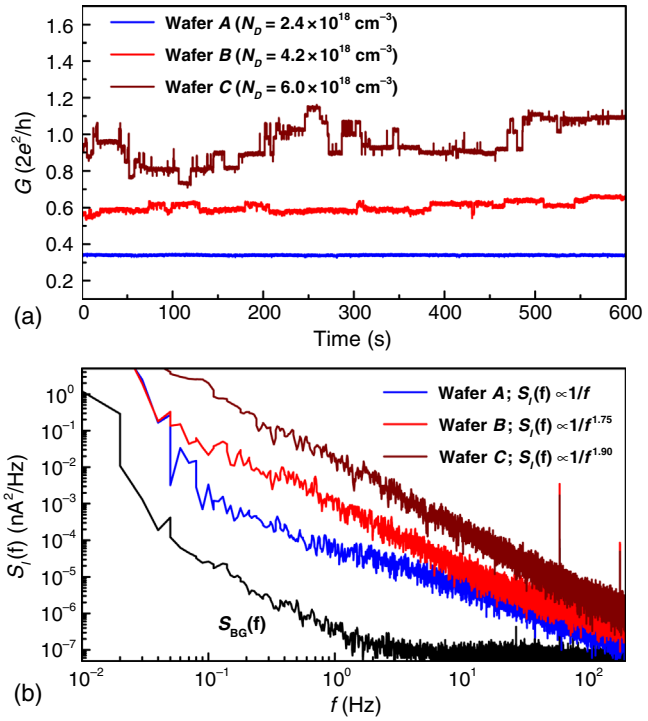

FIG. 3. (a) QPC time traces for structures with different doping densities, offset for clarity [wafer B is offset by $0.2 \times (2e^2/\mathrm{h})$ and wafer C is offset by $0.4 \times (2e^2/\mathrm{h})$]. (b) Noise power spectral density $S_I(f)$ obtained from a FFT of the time traces, with experimental background noise $S_{I;\mathrm{BG}}(f)$ measured at zero source-drain voltage (the black trace).

the increased doping density, as shown in Fig. 3. Conductance time traces for QPCs sitting at the first riser of conductance are shown in Fig. 3(a) for QPCs from wafers A, B, and C. Note that the operating gate voltage is nearly identical in all three cases. The conductance of the QPC on wafer A is nearly constant, indicating that this QPC suffers minimal charge noise. The QPC from wafer B shows increased noise and discrete switching events, while the QPC from wafer C shows significant noise amplitude, and severe RTN is visible in the raw data. Clearly, the level of charge noise increases as the doping density is increased. The noise power spectral density, obtained from a fast Fourier transform (FFT) of the time traces, is shown in Fig. 3(b). For comparison, the noise power spectrum of the measurement circuit with zero source-drain bias applied to the device is also shown. The increase of RTN as doping density is increased is reflected in the frequency dependence of power spectral density, which shifts from $1/f$ (for the lowest doping density), indicative of a broad ensemble of trapping sites with a homogeneous distribution of switching time scales, to the Lorentzian dependence $1/f^2$ (for the highest doping density), indicative of the strong influence of proximal two-level traps [24].

We quantify the noise level for each wafer in terms of equivalent gate-voltage noise ΔV_g, given in Eq. (1) (this

represents the voltage noise level applied on the QPC gates that would produce the same conductance fluctuations as caused by the charge noise) [25]. In Eq. (1), $S_I(f)$ is the power spectral density of the current fluctuations through the QPC and $S_{I;\mathrm{BG}}(f)$ is the background noise due to noise in our instruments:

$$\Delta V_g = \sqrt{\int_{0.1\ \mathrm{Hz}}^{100\ \mathrm{Hz}} [S_I(f) - S_{I;\mathrm{BG}}(f)]df} \Big/ \left(\frac{dI_{\mathrm{QPC}}}{dV_g}\right). \quad (1)$$

Figure 4 shows the equivalent gate-voltage noise vs doping density for each wafer. Each data point represents the average of different QPCs from each wafer; six QPCs are measured from wafer *A*, three are measured from wafer *B*, and six are measured from wafer *C*. This plot shows a correlation between the noise level and the doping density. For example, the equivalent gate-voltage noise is substantially larger for the highest-doping-density wafer, wafer *C*, as is the device-to-device variation, as indicated by the increase of the standard error.

According to the negative-*U* model [18,19], the neutral region of the doping layer is expected to contain ionized shallow donors (d^+) that may act as trapping sites and contribute to charge noise. Prevailing theory suggests that electrons tunneling from the Schottky gates are temporarily trapped on these sites and contribute to noise. As our heterostructures are essentially identical—apart from the doping density—the operating voltages are nearly identical. This fact implies that the tunneling matrix element for electrons leaking from the surface gate is the same for all three wafers. Since the noise clearly increases as a function of doping density, we propose that the *number* of trapping sites (shallow ionized d^+ donors) within the neutral region has a primary impact. The noise level increases due to the increasing width of the neutral region and a corresponding increase in the available donor states. We are, in essence, increasing the final density of states for the tunneling process, which leads to enhanced low-frequency noise. While this analysis clearly suggests that heterostructures should be minimally doped to reduce low-frequency noise, other considerations, including the formation of a low-resistance Ohmic contact and the production of high-mobility 2DEGs, make the determination of optimal doping a subtle optimization problem.

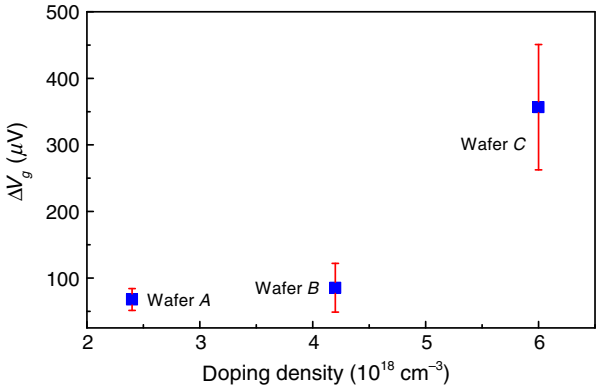

FIG. 4. Equivalent gate-voltage noise ΔV_g vs doping density for wafers *A*, *B*, and *C*. Each data point represents the average of different QPCs from each wafer. Six QPCs are measured from wafers *A* and *C*, and three QPCs are measured from wafer *B*. Error bars represent the standard error computed from the measurements of different QPCs from each wafer.

B. Long-time-scale conductance drift

The second phenomenon we investigate is drift in conductance over long time scales at a fixed gate voltage. A typical conductance time trace upon initial cooldown for a QPC sitting on the first riser of a conductance plateau is shown in Fig. 5(a). Although both negative and positive jumps in conductance occur, the overall trend is that conductance *decreases* over time at a fixed gate bias; equivalently, the operating point of the QPC shifts to a *less negative* voltage over time. We observe this trend for all QPCs cooled with the gates grounded and then energized at $T = 4.2$ K. Typically, the largest amount of drift occurs within the first 24 h after initially biasing the QPC at low temperature, after which the conductance starts to saturate.

We quantify the amount of drift exhibited by each sample as the shift in gate voltage required to operate the QPC on the first conductance riser after 24 h. This quantity is plotted for each wafer in Fig. 5(b); the data are from the same QPCs which are used to characterize the noise. As with the RTN, it is clear that the level of QPC drift increases with an increasing doping density.

Our data suggest that the drift phenomenon may be understood in the following way. Applying negative voltage to the surface gates raises the chemical potential at the gate, μ_{gate}, relative to the chemical potential of the 2DEG, μ_{2DEG}, that is connected to ground. Because the doping layer lies between the gate and the 2DEG, the chemical potential at the doping layer will tend to increase so that it falls between μ_{gate} and μ_{2DEG}, leading to an

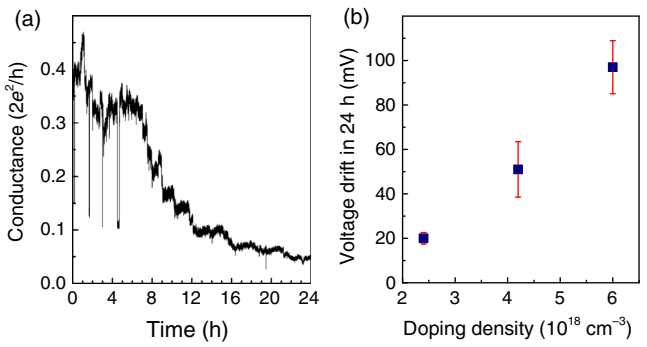

FIG. 5. (a) Long-time-scale conductance drift. (b) The total amount of gate-voltage drift within the first 24 h of operation of QPCs for wafers *A*, *B*, and *C* with different doping densities.

increase over time in the average occupation of donor states. Each time an electron tunnels to a donor site near the QPC, the repulsive potential causes a *negative* jump in the conductance of the QPC. However, because of the substantial tunneling barrier between the surface and the doping layer, the average occupation of donor sites increases slowly; the chemical potential at the doping layer slowly rises as electrons tunnel to the available donor states before saturating at a steady-state value. The dynamics and saturation of this long-time-scale behavior may also be impacted by the complex electric-field configuration in the immediate vicinity of the gate edges, where the electric field has both vertical and horizontal components. Additionally, the fact that the drift occurs over time scales much longer than the RTN suggests that drift may involve deep donor levels with a barrier to electron capture [18], whereas RTN may primarily involve shallow donor d^+ levels.

C. Origin of conductance drift

We perform an additional experiment to investigate the temperature stability of the charge accumulation associated with the conductance-drift phenomenon. A QPC from wafer B is biased on the riser of the first conductance plateau at $T = 4.2$ K for 24 h; significant conductance drift occurs during this period, consistent with the trend shown in Fig. 5. The shift in the conductance vs gate-voltage curve due to drift is shown in Fig. 6 (the dashed black line compared to the solid black line). The QPC is then swept to zero gate bias and kept at zero gate bias at $T = 4.2$ K for an additional 24-h period. Next, the QPC gate bias is again swept to obtain the conductance vs gate-voltage curve (the blue line in Fig. 6). After being kept at zero bias for 24 h, the conductance vs gate-voltage curve does not return to the original state before the drift occurs but remains shifted and closely matched with the curve *after* the drift occurs. This observation indicates that, at $T = 4.2$ K, the accumulated charge that contributes to the conductance drift is frozen; it does not relax after the gate bias is removed. Next, we warm the QPC to a series of increasingly higher temperatures: 40, 80, and 140 K. The QPC is kept at zero gate bias and held at each temperature for approximately 20 h; immediately after this period, the QPC is cooled to $T = 4.2$ K and its conductance vs gate-voltage characteristics are measured. After warming to 40 K, the conductance vs gate-voltage curve shifts to a more negative bias (the dashed blue line in Fig. 6), but it does not return all the way to its original state before the drift occurred, indicating that a significant fraction, but not all, of the charge accumulated due to drift remains frozen in place at $T = 40$ K. After warming to 80 K, the conductance curve (the dashed red line in Fig. 6) shifts to an even more negative bias beyond the initial predrift curve. We take this observation as an indication that the majority of donor states that have trapped electrons in the vicinity of the QPC are now thermally depopulated. Warming to 140 K results in a slight shift in the conductance vs gate-voltage curve (the solid red line in Fig. 6). We attribute the small difference in the initial gate sweep at 4.2 K and the sweep after warming the sample to $T = 140$ K to the random rearrangement of donors states, as is typically seen in the majority of QPCs upon thermal cycling to room temperature.

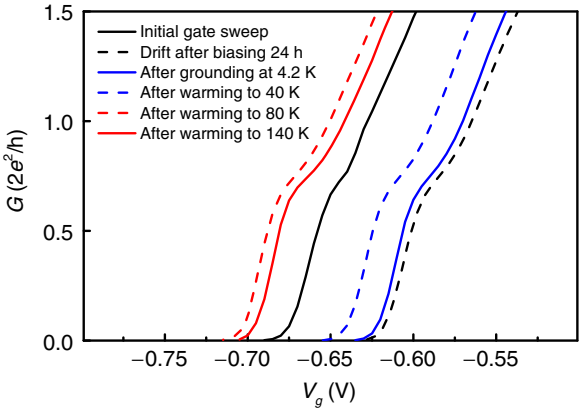

FIG. 6. QPC conductance plot vs gate voltage for wafer B after warming up the QPC to $T = 40$, 80, and 140 K.

The fact that the charge accumulated in the drift process remains frozen at $T = 4.2$ K after the gate bias is removed indicates that the donor state involved in conductance drift has a barrier to emission. The DX^- donor state traps an electron and is known to have a barrier to emission; however, the charge in DX^- states remains frozen at temperatures below 100 K [20,21]. The fact that we observe partial thermal depopulation at 40 K and full depopulations at 80 K suggests that the state responsible for conductance drift is shallower than the DX^- state. Evidence for a trap state associated with the Si donors with a smaller barrier to emission than the DX^- state was reported in Ref. [26]; it is plausible that these states could be responsible for the drift we observe.

IV. CONCLUSION

In conclusion, we unambiguously identify the total number of silicon donors as an important parameter influencing low-frequency charge noise and conductance drift in modulation-doped $GaAs/Al_xGa_{1-x}As$ heterostructures. Our data suggest that electron tunneling to available donor states, especially those in the neutral region, contributes to charge noise and device drift. The comparatively short time scale of the charge noise implies that it primarily involves shallow donor states, while the much longer time scale and the apparent freezing of the charge involved in drift suggest that the drift involves deep donor states. Modulation-doped $GaAs/Al_xGa_{1-x}As$ heterostructures should be grown close to critical doping (that is, with a minimal neutral region in the doping layer) to minimize the number of charge trap sites available. We emphasize that wafers used for mesoscopic devices are frequently grown with a significant degree of

overdoping (similar to wafer *B*), so there is ample room for reducing charge noise by reducing the doping density. Using this guideline, devices with minimal charge noise may be achieved that can serve as a robust, stable platform for spin-qubit-based quantum computing.

ACKNOWLEDGMENTS

This work was supported by the U.S. DOE Office of Basic Energy Sciences, Division of Materials Sciences and Engineering Award No. DE-SC0006671. Additional support from Nokia Bell Laboratories for the MBE facility is gratefully acknowledged. M. J. M. acknowledges the many useful conversations with David Reilly concerning charge noise in mesoscopic semiconductor devices.

[1] F. Martins, F. K. Malinowski, P. D. Nissen, E. Barnes, S. Fallahi, G. C. Gardner, M. J. Manfra, C. M. Marcus, and F. Kuemmeth, Noise Suppression Using Symmetric Exchange Gates in Spin Qubits, Phys. Rev. Lett. **116**, 116801 (2016).

[2] J. M. Nichol, L. A. Orona, S. P. Harvey, S. Fallahi, G. C. Gardner, M. J. Manfra, and A. Yacoby, High-fidelity entangling gate for double-quantum-dot spin qubits, npj Quantum Inf. **3**, 3 (2017).

[3] M. Avinun-Kalish, M. Heiblum, O. Zarchin, D. Mahalu, and V. Umansky, Crossover from "mesoscopic" to "universal" phase for electron transmission in quantum dots, Nature (London) **436**, 529 (2005).

[4] J. R. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, and A. C. Gossard, Coherent manipulation of coupled electron spins in semiconductor quantum dots, Science **309**, 2180 (2005).

[5] Y. Li, C. Ren, P. Xiong, S. von Molnár, Y. Ohno, and H. Ohno, Modulation of Noise in Submicron GaAs/AlGaAs Hall Devices by Gating, Phys. Rev. Lett. **93**, 246602 (2004).

[6] G. Timp, R. E. Behringer, and J. E. Cunningham, Suppression of impurity scattering in a one-dimensional wire, Phys. Rev. B **42**, 9259 (1990).

[7] D. H. Cobden, N. K. Patel, M. Pepper, D. A. Ritchie, J. E. F. Frost, and G. A. C. Jones, Noise and reproducible structure in a GaAs/Al_xGa_{1-x}As one-dimensional channel, Phys. Rev. B **44**, 1938 (1991).

[8] D. H. Cobden, A. Savchenko, M. Pepper, N. K. Patel, D. A. Ritchie, J. E. F. Frost, and G. A. C. Jones, Time-Irreversible Random Telegraph Signal due to Current along a Single Hopping Chain, Phys. Rev. Lett. **69**, 502 (1992).

[9] C. Kurdak, C. J. Chen, D. C. Tsui, S. Parihar, S. Lyon, and G. W. Weimann, Resistance fluctuations in GaAs/Al_xGa_{1-x}As quantum point contact and Hall bar structures, Phys. Rev. B **56**, 9813 (1997).

[10] M. Pioro-Ladrière, J. H. Davies, A. R. Long, A. S. Sachrajda, L. Gaudreau, P. Zawadzki, J. Lapointe, J. Gupta, Z. Wasilewski, and S. Studenikin, Origin of switching noise in GaAs/Al_xGa_{1-x}As lateral gated devices, Phys. Rev. B **72**, 115331 (2005).

[11] C. Buizert, F. H. L. Koppens, M. Pioro-Ladrière, H.-P. Tranitz, I. T. Vink, S. Tarucha, W. Wegscheider, and L. M. K. Vandersypen, *In Situ* Reduction of Charge Noise in GaAs/Al_xGa_{1-x}As Schottky-Gated Devices, Phys. Rev. Lett. **101**, 226603 (2008).

[12] K. Hitachi, T. Ota, and K. Muraki, Intrinsic and extrinsic origins of low-frequency noise in GaAs/AlGaAs Schottky-gated nanostructures, Appl. Phys. Lett. **102**, 192104 (2013).

[13] J. You, H.-O. Li, K. Wang, G. Cao, X.-X. Song, M. Xiao, and G.-P. Guo, Suppression of low-frequency charge noise in gates-defined GaAs quantum dots, Appl. Phys. Lett. **107**, 233104 (2015).

[14] H.-O. Li, G. Cao, M. Xiao, J. You, D. Wei, T. Tu, G.-C. Guo, H.-W. Jiang, and G.-P. Guo, Fabrication and characterization of an undoped GaAs/AlGaAs quantum dot device, J. Appl. Phys. **116**, 174504 (2014).

[15] S. Mondal, G. C. Gardner, J. D. Watson, S. Fallahi, A. Yacoby, and M. J. Manfra, Field-effect-induced two-dimensional electron gas utilizing modulation-doped Ohmic contacts, Solid State Commun. **197**, 20 (2014).

[16] S. Birner, T. Zibold, T. Andlauer, T. Kubis, M. Sabathil, A. Trellakis, and P. Vogl, NEXTNANO: General purpose 3-D simulations, IEEE Trans. Electron Devices **54**, 2137 (2007).

[17] E. F. Schubert and K. Ploog, Shallow and deep donors in direct-gap *n*-type Al_xGa_{1-x}As: Si grown by molecular-beam epitaxy, Phys. Rev. B **30**, 7021 (1984).

[18] D. J. Chadi and K. J. Chang, Energetics of DX-center formation in GaAs and Al_xGa_{1-x}As alloys, Phys. Rev. B **39**, 10063 (1989).

[19] K. Khachaturyan, E. R. Weber, and M. Kaminska, in *Defects in Semiconductors*, Vols. 38–41, edited by G. Ferenczi (Trans Tech Publications, Aedermannsdorf, Switzerland, 1989), p. 1067.

[20] H. Künzel, A. Fischer, J. Knecht, and K. Ploog, Investigation of persistent photoconductivity in Si-doped *n*-Al_xGa_{1-x}As grown by molecular beam epitaxy, Appl. Phys. A **32**, 69 (1983).

[21] H. Künzel, K. Ploog, K. Wünstel, and B. L. Zhou, Influence of alloy composition, substrate temperature, and doping concentration on electrical properties of Si-doped n-Al_xGa_{1-x}As grown by molecular beam epitaxy, J. Electron. Mater. **13**, 281 (1984).

[22] E. Buks, M. Heiblum, Y. Levinson, and H. Shtrikman, Scattering of a two-dimensional electron gas by a correlated system of ionized donors, Semicond. Sci. Technol. **9**, 2031 (1994).

[23] E. Buks, M. Heiblum, and H. Shtrikman, Correlated charged donors and strong mobility enhancement in a two-dimensional electron gas, Phys. Rev. B **49**, 14790 (1994).

[24] A. L. McWhorter, in *Semiconductor Surface Physics*, edited by R. H. Kingston (University of Pennsylvania Press, Philadelphia, 1957), p. 207.

[25] S. W. Jung, T. Fujisawa, Y. Hirayama, and Y. H. Jeong, Background charge fluctuation in a GaAs quantum dot device, Appl. Phys. Lett. **85**, 768 (2004).

[26] Y. B. Jia, M. F. Li, J. Zhou, J. L. Gao, M. Y. Kong, P. Y. Yu, and K. T. Chan, Discovery of a new photoinduced electron trap state shallower than the DX center in Si doped Al_xGa_{1-x}As, J. Appl. Phys. **66**, 5632 (1989).