Electronic Transport in Hydrogen-Terminated Si(001) Nanomembranes

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Charge carrier transport in thin hydrogen (H)-terminated Si(001) sheets is explored via a four-probe device fabricated on silicon-on-insulator (SOI) using the bulk host Si as a back gate. The method enables electrical measurements without the need to contact the sample surface proper. Sheet conductance measurements as a function of back-gate voltage demonstrate the presence of acceptor- and donorlike surface states. These states are distributed throughout the gap and can be removed or transformed with low-temperature annealing. The density of donorlike states is just under 10^{12} cm^{-2} eV^{-1} and 3 times higher than that of the acceptorlike states. We discuss the possible origins of these states. The conductance through the surface layer is too small to measure.

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I. INTRODUCTION

In conventional semiconductors, the properties of the charge carriers in the bulk of the material generally dominate the electrical conductance, even though surfaces (or internal interfaces for composite systems) may have their own characteristic conduction properties. As the semiconductor becomes thinner, that is no longer true. The electrical conductance becomes sensitively controlled by an interplay between the electronic structure of the surface(s) and that of the interior of the material (which we call "bulk") [1–6]. To separate these effects and to identify and potentially enhance the contribution of the surface proper, one can investigate increasingly thin semiconductor sheets, thereby minimizing the possible bulk contribution [1,6–8]. In materials such as diamond in which the bulk conductivity is already very small, it is not necessary to make a very thin sheet [6], but that is not true for semiconductors in general and Si in particular.

Single-crystal sheets with thicknesses of less than a few 100 nm have come to be called nanomembranes (NMs) [9]. Through thinness, extreme flexibility, and a high surface- or interface-to-volume ratio, NMs exhibit remarkable mechanical, optical, and electrical properties that are quite different from those of a corresponding bulk crystal. Consequently, NMs have spawned applications in diverse fields such as flexible and stretchable electronics [10–13], photonic structures [14–16], energy-storage devices [17,18], and solar cells [19]. NM structures can be completely freestanding, tethered to a substrate, or bonded to different host materials [7,20]. Obviously, for electronic applications of NMs or NM-host systems, it becomes imperative that the impact of surfaces and interfaces on charge transport be identified and understood [21,22].

We recently developed an ultrahigh-vacuum (UHV) conductance spectroscopy method that generates electrical-transport information in thin semiconductor sheets via back-gate voltage tuning [23]. We utilized a four-probe device fabricated on the semiconductor, along with a back gate separated from the sample by a dielectric material. This method allows isolation and quantitative determination of the factors that contribute to charge transport in very thin semiconductor sheets. We used this approach to identify and quantify surface charge transport in clean (2×1) reconstructed Si(001) NMs by using ever thinner Si sheets to reduce more and more the bulk Si contribution to conduction [23]. We showed how surface structure can influence this charge transport and how the band structure of the bulk can interact with that of the surface. We were able to show that the minimum conductance was controlled by the surface, because, as the Si sheet was made thinner, the conductance reached a constant value, as the bulk contribution became smaller and smaller [23]. We also suggested there that the method is broadly applicable.

Here, we extend that work to study the electrical conductance of a similar Si(001) sheet but with a chemically modified surface, namely, a hydrogen termination. As we mention above, measuring a range of NM thicknesses

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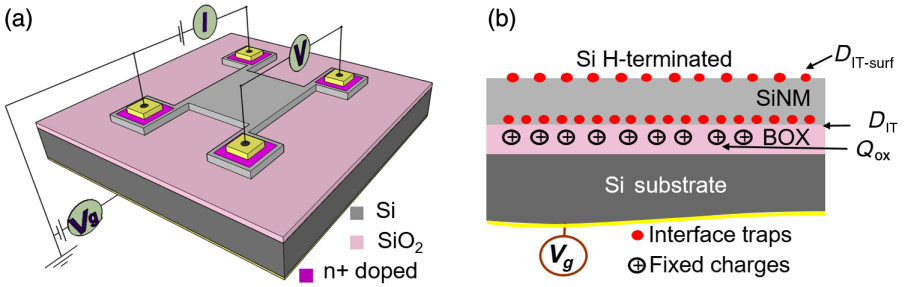

FIG. 1. Schematic diagram of the van der Pauw measurement on Si NMs and a cross section of the device. (a) A mesa is patterned on the SOI wafer representing an inverted MOSFET structure. The central region is 4×4 mm^2; the four corner contacts are doped with P. One of eight possible measurements is shown in the diagram, with current passing through two adjacent contacts and voltage measured between the other two. The Si substrate serves as a back gate. (b) Schematic cross-sectional view of H-terminated SOI(001) showing localized states, as we describe in the text.

is critical in order to decouple the factors influencing the conductance that relate to the surface or interface from the conductance of the bulk Si sheet. In contrast to the results for the clean surface, the minimum sheet conductance here continues to decrease as the Si sheet becomes thinner, implying that we are unable to provide an actual value for the surface conductance. As for the clean surface, however, the shapes of the sheet conductance–back-gate-voltage curves provide much information on surface states controlling the charge transport. An analysis of these shapes for Si(001) sheets with H-terminated surfaces demonstrates the presence of acceptorlike and donorlike surface states, with the donorlike states dominant by approximately a factor of 3, at a density on the order of 10^{12} cm^{-2} eV^{-1}. They are removed or transformed with low-temperature annealing.

II. EXPERIMENT

Understanding charge transport in thin semiconductor sheets with chemically modified surfaces is important for the following reasons. In the processing of electronic or optoelectronic devices, the initial surface structure and chemical terminations largely determine subsequent interfacial electronic properties [24–27]. Additionally, for thin enough materials, surfaces or interfaces may influence the charge transport properties of the entire structure, highlighting the need for both understanding the mechanisms behind surface-bulk interactions and developing new ways to control and tailor these interactions.

Common techniques to examine the surface and interfacial electronic properties and charge transport include conductance-voltage and capacitance-voltage measurements [28], with surface sensitivity down to 10^{10} defects/cm^{-2} eV^{-1} [29]. In these methods, however, the required procedures exert a strong influence on the surface and underlying interface [30,31]. Consequently, the interpretation of the experimental results is semiquantitative and sometimes masked by band-bending effects at the surface. For that reason, spatially indirect contact for electrical characterization of the surface of thin sheets is extremely appealing.

To characterize the H-terminated Si(001) sheet, we pattern a Si NM into a van der Pauw geometry while it is still bonded to the original host, 3-μm-thick SiO_2 on a Si handle wafer, part of silicon-on-insulator (SOI) [32]. The Si NM template layer is p type (boron doped with a nominal doping level approximately 10^{15} cm^{-3}) with thickness varying from 77 to 220 nm. We create the H termination with a weak hydrofluoric acid (HF) dip.

Figure 1(a) shows a schematic diagram of the van der Pauw geometry patterned on SOI and the measurement setup. The device architecture is akin to a pseudo-MOSFET, except that we have a four-probe geometry and vacuum at the front surface. We use the Si handle wafer as a back gate, which is a key element in our measurements. Details of the fabrication are summarized in Sec. III and are described in detail in our earlier paper [23].

Figure 1(b) shows a schematic cross section of the layer structure indicating the factors [23] that interact to determine the sheet conductance of the Si NM, including surface states with a density $D_{\text{IT-surf}}$, states at the interface between the Si NM and the buried oxide with a density D_{IT}, and fixed oxide charge with a density Q_{ox}. In addition, there may be a surface charge Q_{surface}. We extract information about these states and their influence on charge transport in the Si NM through measurement of the sheet conductance as a function of the back-gate voltage and modeling to fit the experimental results.

III. MATERIALS AND METHODS

A. Device fabrication

The sheet conductance method employs a four-probe van der Pauw configuration geometry fabricated on Si NMs bonded on their original host substrate, SOI, [32], as shown in Fig. 1(a). The nominal doping of the substrate is p type $N_A \sim 10^{15}$ cm^{-3}. In essence, a mesa is patterned with four contacts pads, and the surrounding Si is removed to isolate the structure. The pads are then doped to ensure Ohmic contact with the four metal sample holder pressure clamps that are used to inject current and measure the voltage across

the sample. Before introduction to the UHV system, the surface is thoroughly degreased with acetone and isopropanol, followed by a 15-min UV ozone exposure, and then chemically cleaned using standard Radio Corporation of America procedures [33] before a final HF dip (10% HF, 20 s) to terminate it with hydrogen. Immediately after, the sample is mounted and transferred to the measurement chamber, where spring-loaded connectors attach to the sample holder clamps. All contacts are grounded throughout the sample installation to prevent electrostatic shock, which is detrimental to the BOX layer. The procedure is required to avoid oxide leakage current. A base pressure of $<1\times 10^{-10}$ Torr enables stable and repeatable measurements. Different membrane thicknesses are obtained by thinning the SOI prior to device fabrication. An initial 220-nm SOI wafer is thinned with repeated oxidation at 1150 °C, followed each time by oxide stripping in HF.

B. Theory

Surface electrical information is obtained from comparisons between experimental results and numerical simulations. The entire SOI system is treated as a gate-insulator-semiconductor capacitor (from substrate toward the surface). The band diagram is constructed by solving Poisson's equation throughout the system. The membrane sheet conductance, G, is then calculated from the local carrier concentration. In this way, G is obtained as a function of V_g. A detailed description of the model can be found in the Supplemental Material [34] and in Ref. [35].

C. Measurement system

UHV provides excellent control of the sample surfaces and is crucial to the stabilization of measurement conditions. From a load lock at approximately 10^{-8} Torr, a mechanical arm pushes the sample holder into the main chamber, whose base pressure is approximately 8×10^{-11} Torr.

The sample is heated radiatively or by electron bombardment with a tungsten filament behind the sample. Radiative heating alone is used for annealing at low temperature.

D. X-ray photoelectron spectroscopy and electrical measurements

X-ray photoelectron spectroscopy (XPS) is performed primarily with a PHI 5600 ESCA system with a monochromatic Al $K\alpha$ source ($h\nu = 1486.6$ eV). The Supplemental Material provides more detail [34].

We make eight four-probe measurements for each back-gate voltage, from which we deduce the conductance per square using the standard van der Pauw formulas [36]. By using the van der Pauw analysis, we implicitly assume the template layer is thin enough (220 nm or less) compared with its lateral dimensions (4×4 mm^2) and that equilibrium between the front and the back interfaces is achieved over lateral length scales much smaller than the device dimensions [23]. Furthermore, the (4×4)-mm^2 central device mesa is defined by etching down to the BOX. The mesa reaches the contact regions via four 500-μm-wide and 500-μm-long arms. This geometry causes less than 1% experimental error in the van der Pauw sheet resistance measurements.

IV. RESULTS AND DISCUSSION

To measure the sheet conductance, we sweep the back-gate voltage V_g from high positive to high negative values. Figure 2(a) shows a representative sheet conductance vs V_g curve with the regions of interest highlighted (see figure caption). As we sweep to more negative back-gate voltage, holes accumulate at the oxide-Si NM interface, eventually forming an accumulation channel, with the flat-band voltage (V_{FB}) defined by the onset of this channel. A schematic band diagram representative of this condition is shown in the top left of the plot. Similarly, as we sweep to positive V_g, electrons accumulate in the Si NM at the oxide-NM interface to form an inversion channel with the threshold voltage V_T defining the onset. It is the region between the flat-band and threshold voltages that yields critical information on the electronic behavior of the NM [23,37].

Figure 2(b) shows log sheet conductance vs V_g curves of H-terminated Si NMs having thicknesses of 77, 120, and 220 nm. All NMs show both hole accumulation and electron inversion regions when the gate voltage is highly negative or highly positive, respectively, with clear ambipolar behavior (both electron and hole conduction). Between these regions, the NM conductance reaches a minimum (G_{min}). Moreover, the conductance-voltage curve has a distinctly asymmetric shape, with an obvious change of curvature on the positive-voltage side. The G_{min} value drops by more than 1 order of magnitude as the membrane thickness decreases from 220 to 77 nm. In addition, the conductance minimum is broader for thinner NMs.

As we indicate above and illustrate schematically in Fig. 1(b), the various localized states at the surface and interfaces will influence the conductance-voltage characteristics of this type of structure. In addition, the NM bulk will contribute to the sheet conductance. The nominal doping level (here, $N_A\sim 10^{15}$ cm^{-3}) and the thickness of the NM control this contribution. We deliberately use a thin sheet to lower this contribution. For this doping density and the range of NM thicknesses used here, the total number of dopants contained in the NM is 10^9–10^{10} cm^{-2}, depending on the NM thickness. As we show next, the combination of low N_A and thinness diminishes the effect of bulk doping on the conductance, allowing any influence caused by the surface termination to become observable [23].

Figure 2(c) shows the minimum sheet conductance of the bulk of the NM calculated for three different NM thicknesses and compares it to the measured values [the minima

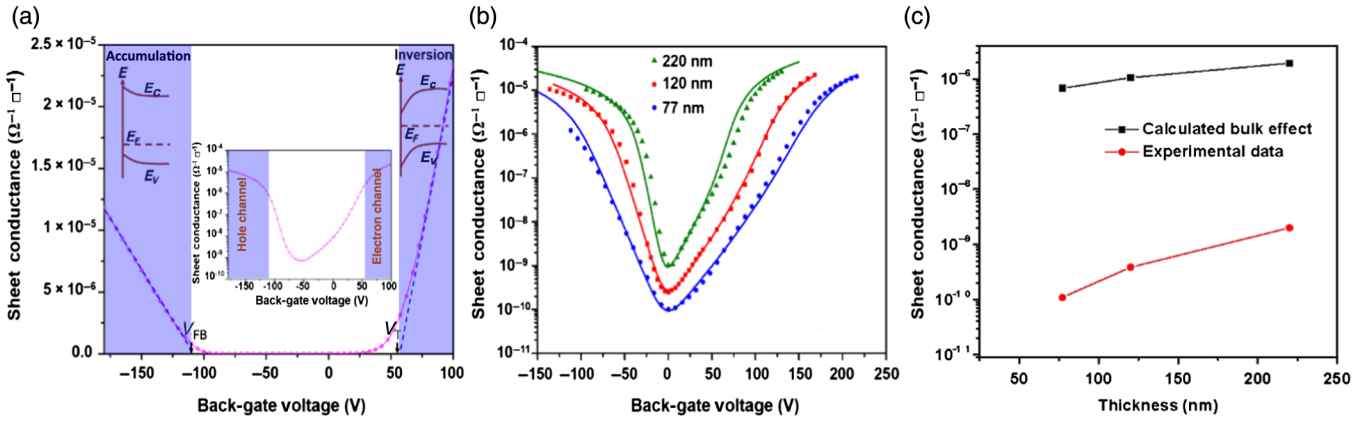

FIG. 2. Sheet conductance as a function of back-gate voltage for H-terminated SOI(001). (a) Graph for a 120-nm-thick Si template layer. The data are plotted in linear and log (inset) scales. The flat-band voltage V_{FB} and the threshold voltage V_T are extracted from linear extrapolations of the curve at high negative and positive gate voltages, respectively. Surface- and interface-related electrical information is determined from the low-conductance region (white region between V_{FB} and V_T). The insets show the band diagrams at the oxide-NM interface. Figure adapted from Ref. [23]. (b) Data (symbols) and simulation fits (lines) of conductance-voltage measurements of H-terminated SOI(001) for three different Si template thicknesses: 77, 120, and 220 nm. The curves are shifted along the voltage axis to have the sheet conductance minima appear at zero back-gate voltage. Uncertainties in the NM thickness and the electrical measurements are sufficiently small so that the resulting uncertainty in the sheet conductance does not exceed the size of the data points shown in (b). (c) Comparison between the naive calculated minimum conductance, as we describe in the text, of the NM bulk and experimental data (containing both bulk and surface effects) for G_{min} shown in (b) for 77-, 120-, and 220-nm-thick Si NMs.

shown in Fig. 2(b)]. To calculate this sheet conductance, we use

$$G_{\min}(\text{bulk}) = qt(\mu_h n_h + \mu_e n_e), \tag{1}$$

where q is electronic charge, t is NM thickness, μ_e is electron mobility, n_e is electron density, μ_h is hole mobility, and n_h is hole density. For this calculation, we assume that the NM bulk dopants alone determine the minimum sheet conductance of a thin NM; i.e., there is no effect of surface and interface. As the NM is p doped, $\mu_h n_h$ has the dominant role in this bulk sheet conductance. Using Eq. (1), we calculate for p-doped NMs ($n_p = 10^{15}$ cm^{-3}) with thicknesses of 77-, 120-, and 220-nm sheet conductances of 6.8×10^{-7}, 1.1×10^{-6}, and 1.9×10^{-6} $\Omega^{-1}\,\square^{-1}$, respectively. The decrease of G_{min} with thickness for the bulk is linear, as it is proportional to the volume, which decreases linearly with decreasing thickness.

The measured values, also shown in Fig. 2(c), of the sheet conductance at the value of V_g corresponding to G_{min} are several orders of magnitude lower than the G_{min} value calculated for the bulk component at corresponding thicknesses, thus demonstrating the dominant influence of the chemically modified surface and states associated with it. The measured minimum sheet conductance values do not decrease linearly with reduced thickness (2×10^{-9} $\Omega^{-1}\,\square^{-1}$ for 220 nm, 3.9×10^{-10} $\Omega^{-1}\,\square^{-1}$ for 120 nm, and 1.1×10^{-10} $\Omega^{-1}\,\square^{-1}$ for 77 nm). The thickness of the NM determines the coupling strength between the front H-terminated surface and the back gate via modification of the membrane capacitance. Thinner membranes have a higher capacitance, and, therefore, the effects at the surface exert a stronger influence on the conduction properties.

Previous studies of pseudo-MOSFETs [21,22] have shown that states at the interface of the Si template layer and the BOX trap charge, and thereby affect the subthreshold slope via $1/C_{ox}$, where C_{ox} is the oxide capacitance ($C_{ox} = \varepsilon_{ox}/t_{ox}$, approximately 1 nF/cm^2). The states at the top Si surface affect the slope via a more complex term $(1/C_{ox})[C_{Si}/(C_{Si} + C_{IT|Si\text{-}H})]$. Here, C_{Si} is the membrane capacitance ($C_{Si} = \varepsilon_{Si}/t_{Si}$, about 50 nF/cm^2 for a 220-nm-thick NM and 140 nF/cm^2 for a 77-nm-thick NM), and $C_{IT|Si\text{-}H}$ is the interface state capacitance of H-terminated Si ($C_{IT|Si\text{-}H} = q^2 D_{IT|Si\text{-}H}$, about 160 nF/cm^2 for $D_{IT} = 10^{12}$ cm^{-2} eV^{-1}). For our thin NMs, the latter term roughly equals 0.24 and 0.47 of the value of $1/C_{ox}$ at the Si/SiO$_2$ interface for 220- and 77-nm-thick Si NMs, respectively. The H-terminated surface, therefore, should have an important influence on the carrier transport within the NM. A thinner membrane has a larger C_{Si}, thus a stronger coupling strength between the H-terminated Si surface and the back gate, and a stronger effect of this surface on the NM conductance.

Figure 2(b) also shows fits to the data using a model [23,28,35] that includes both fixed oxide charges (Q_{ox}) and interface states ($D_{IT|ox}$) at the Si template layer-SiO$_2$ interface. The positive fixed oxide charges are located on the SiO$_2$ side, within 3 nm of the interface [38]. The energies of the interface states are uniformly distributed across the Si band gap, with acceptorlike states above and donorlike states below the center of the band gap [28]. By definition, donorlike states are neutral when occupied

TABLE I. Fitting parameters used for the simulation curves shown in Fig. 1(b). $D_{IT|ox}$ and Q_{ox} represent the interface state density and the fixed oxide charge at the Si/SiO_2 interface, respectively. $D_{IT|H\,donor}$ and $D_{IT|H\,acceptor}$ are donorlike and acceptorlike surface states at the H-terminated Si(001) surface. The values have an uncertainty from 3% to 9%.

Membrane thickness (nm)	$D_{IT\|ox}$ ($cm^{-2}\,eV^{-1}$)	Q_{ox} (cm^{-2})	$D_{IT\|H\,donor}$ ($cm^{-2}\,eV^{-1}$)	$D_{IT\|H\,acceptor}$ ($cm^{-2}\,eV^{-1}$)
220	8.7×10^{11}	1.0×10^{10}	6.7×10^{11}	2.3×10^{11}
120	1.4×10^{12}	1.0×10^{10}	8.1×10^{11}	2.9×10^{11}
77	1.9×10^{12}	2.7×10^{11}	9.3×10^{11}	3.3×10^{11}

by electrons and positively charged when empty, while acceptorlike ones are negatively charged when occupied and neutral when empty. For H-terminated Si(001), the model fully described in Ref. [35] assumes that donorlike states ($D_{IT|H\,donor}$) and acceptorlike states ($D_{IT|H\,acceptor}$) coexist but in different amounts. For simplicity, we also assume that both types of these NM surface states have a uniform energetic distribution throughout the band gap. This assumption is equivalent to a picture in which the neutrality point lies away from the center of the Si band gap. This model captures the main aspects of the surface electronic structure with the fewest number of fitting parameters [23,28,35]. A schematic diagram of our one-dimensional simulation model [23,35] is shown in Fig. 1(b). Using the four parameters $D_{IT|ox}$, $D_{IT|H\,donor}$, $D_{IT|H\,acceptor}$, and Q_{ox} and setting up the corresponding boundary conditions, we solve 1D Poisson's equations numerically, extracting the local potential as well as the carrier concentrations as a function of the depth into the Si NM. The membrane conductance is then calculated from the carrier concentration and the electron and hole mobilities, taking into consideration the mobility degradation caused by phonons, dopants, and above all, interface roughness (see the Supplemental Material for more details [34]). The simulated conductance vs V_g curves agree well with the data. The fitting parameters used for the three thicknesses are consistent with each other, suggesting the simple model we are using describes the actual system quite well.

Table I shows these fitting parameters and demonstrates that we can quantitatively determine the state densities. In particular, there is a large population of localized trap states on H-terminated Si(100) surfaces, and the majority of these trap states are donorlike. The approximately 3 times as many donorlike states as acceptorlike states leads directly to the asymmetric conductance-voltage curve. The opposite situation, i.e., a majority of acceptorlike states, leads to a curve shape in contradiction to what is observed in Fig. 2(b) (see Fig. S2 in the Supplemental Material [34]). Table I also shows that all fitting parameters become slightly larger as the NM becomes thinner. All values except for Q_{ox} are within a factor of 2 for the different thicknesses. We may be able to attribute the increase in $D_{IT|ox}$ and Q_{ox} to additional cycles of thermal oxidation at a high temperature (1050 °C) followed by oxide removal in HF in order to reach the desired NM thicknesses. Q_{ox} in any case affects only the value of V_g at which G_{min} occurs. The small increases in surface state densities as the NM gets thinner may be associated with surface roughness induced by multiple exposures of the surface to HF during the thinning process.

To explain the sheet conductance-voltage results and to understand the influence of these donorlike states on the carrier transport in Si NMs, it is useful to investigate the band bending in a Si NM at different back-gate voltages. The simulated band diagrams at three different conditions are examined in Fig. 3 for a 77-nm-thick Si NM at accumulation [Fig. 3(b)], at the conductance minimum G_{min} [Fig. 3(c)], and at inversion [Fig. 3(d)], which are marked with red circles on the sheet-conductance–gate-voltage curve shown

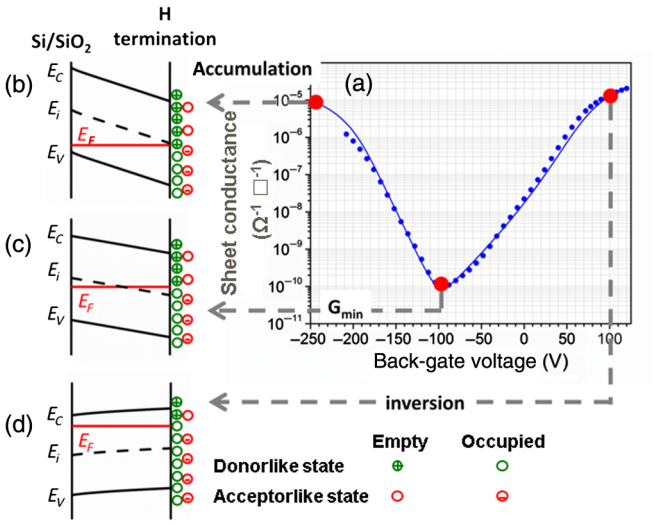

FIG. 3. Diagrams for bands at three back-gate voltage conditions for a H-terminated Si(001) NM. (a) The sheet conductance–voltage curve for a 77-nm-thick Si NM. Unlike the curves presented in Fig. 2(b), the curve here is not shifted along the voltage axis. (b)–(d) are simulated diagrams of the positions of bands and the Fermi level across the Si NM at three different voltages: $V_g = -250$ V (accumulation), $V_g = -96$ V (at conductance minimum), and $V_g = 96$ V (inversion). The values of V_g, from −210 to 120 V, are limited by the range of the voltage source. For simplicity, the only band bending shown in these diagrams is due to back-gate voltage. The value of E_F at the surface is described as E_{FS} in the text.

in Fig. 3(a). The data of Fig. 3(a) are already shown as part of Fig. 2(b), but here $G_{\min}$ appears at a negative gate voltage because the minimum is not shifted to zero gate voltage as it is in Fig. 2(b) to enhance comparison. The positive fixed oxide charge at the template Si/SiO_2 interface and a large number of unoccupied donorlike states (positively charged) at the H-terminated Si(100) surface act effectively as a gate voltage to shift $G_{\min}$.

At $V_g = -250$ V, as expected, the Fermi level is very close to the valence-band edge at the template Si/SiO_2 interface, and holes accumulate at the interface near the oxide. However, the Fermi level is pinned near midgap for H-terminated Si(001) surfaces because of the large number of donor states at the surface. Above the surface Fermi level E_{FS}, those donorlike states are unoccupied and, thus, positively charged. As a result, there exists a large band bending within the membrane, with the electric field pointing from the Si-H surface to the template Si/SiO_2 interface. When the back-gate voltage is increased, the Fermi level moves up correspondingly. The change in position of E_{FS}, the Fermi level at the H-terminated Si (001) surface, is considerably less than it is at the Si/SiO_2 interface, with E_{FS} remaining near the midgap. Moreover, the band bending across the membrane, as well as the number of positive surface charges, is slightly reduced; see Fig. 3(c). The conductance reaches its minimum value when E_{FS} intersects E_i [$V_g = -96$ V; see Fig. 3(a)]. The thickness comes into play because the carrier concentration in the membrane per unit area is proportional to the thickness. At this voltage, the total carrier concentration within the membrane is as small as it can be, and the numbers of electrons and holes are approximately equal. When V_g is further increased to more positive voltages, the conductance increases again as E_{FS} moves closer to the conduction band; see Fig. 3(d). Finally, the whole membrane becomes inverted (for this 77-nm NM at $V_g = 96$ V). Most of the donorlike states at the H-terminated Si(100) surface are now filled and so are the acceptorlike states. This fact gives rise to the slightly negatively charged H-terminated Si surface at this condition and the relatively flat bands in the Si NM.

The simulation demonstrates that the position of E_{FS} at the H-terminated Si surface can be varied under the influence of a back gate. For most of the range of gate voltages, H-terminated Si(100) has a net positive surface charge because of the unoccupied donor states; therefore, a large electric field is established across the membrane. The position of the Fermi level at the surface has a limited range (from approximately the midgap to near the conductance-band edge for a 77-nm-thick NM) under the influence of the back gate. This range is reduced for a thicker membrane (see Fig. S3 in the Supplemental Material [34] for simulations on 220-nm-thick NMs). Consequently, fewer surface electrical defects are probed, resulting in a narrower shape of the sheet conductance curve for thicker NMs, as is evident in Fig. 2(b). Around $G_{\min}$, the band bending in NMs of different thicknesses is approximately the same. Also, those surface states on H-terminated Si(100) that are below the midgap cannot be detected even for the thinnest NM used in our experiment. This conclusion will not change even when we change the substrate doping from low p type to low n type, as the bulk dopants are completely irrelevant here. The only way to increase the probing range is to use a thinner membrane, which increases the membrane capacitance C_{Si} and, therefore, the coupling strength between the back gate and the top surface. An extremely thin Si NM (below 10 nm) may enable characterization of the states in the H-terminated surface within the entire Si band gap.

Our back-gated four-probe measurements in conjunction with simulations allow us to extract quantitative information on the role interface states play in the electronic transport properties of thin semiconductors or surfaces.

We now consider the origin of the donorlike states at the H-terminated Si(001) surface. It is known that this surface is atomically disordered with dihydrides as the dominant surface species [39]. Prior measurements using spectroscopic methods found a large band bending on bulk Si(100) surfaces after HF treatment [40–42] for various doping levels and types. As shown in Fig. 3(a), NMs are under weak inversion when no gate voltage is applied because of these unoccupied donorlike surface states. They constrain the movement of the surface Fermi level during sweeps of the gate voltage until the membrane is strongly inverted, equivalent to highly n-doped bulk Si (which is the one doping type that does not produce the band bending suggestive of donorlike surface states [40]). Our simulation shows that positive fixed oxide charges, which are located at the template Si/SiO_2 interface, are 1 order of magnitude lower in density than $D_{IT|H\,donor}$ and, thus, play a minor role. With back-gate tuning, the effective carrier density in the NM is efficiently changed.

Although we identify surface states as unoccupied donorlike states, their origin is uncertain. Residual species such as OH and fluorine groups are often detected on H-terminated Si(100) after HF etching, and their amount depends on the HF concentration and the following rinse time (when it occurs) in DI water. XPS studies of the as-prepared H-terminated Si(100) surfaces frequently show traces of O and C but no F signal (see the Supplemental Material [34]). In any case, as both oxygen and fluorine are more electronegative than Si, they will not donate electrons to Si and become positively charged. Some studies suggest the very initial attack of the H termination by humidity as a cause of the large band bending observed on Si-H terminations [43].

There appear to be two possibilities to explain our measurements: (1) adventitious contamination on the HF-treated surfaces that is introduced via the HF or via the ambient in the time between removal of the sample from the bath and introduction to the UHV system. Because

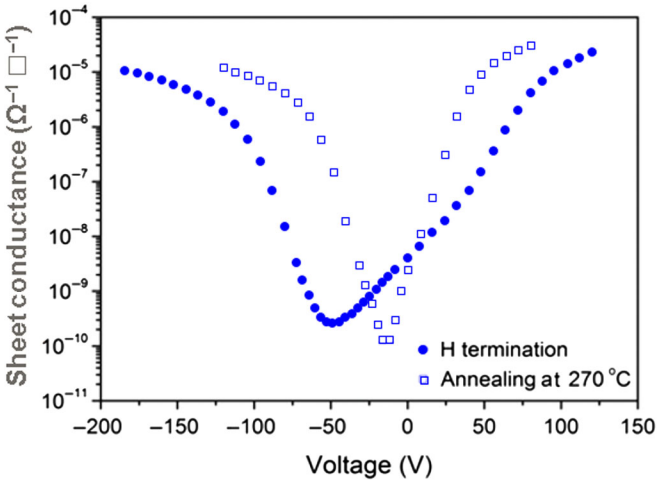

FIG. 4. Measured sheet conductance-voltage curves of a 77-nm-thick H-terminated Si NM before and after short-time low-temperature annealing at 270 °C.

of the low density of states relative to a monolayer, a concentration of contaminants far below the detection limit of XPS is needed. (2) Disordered adsorbed H rather than contamination. To search for further understanding, we anneal the H-terminated sample by radiatively heating it via a filament from the back. The annealing temperature is low enough (approximately 270 °C) not to desorb any hydrogen [44] or affect the properties of the BOX interface, but adventitious contamination that is weakly bound to the surface can be removed. Additionally, disordered H can rearrange on the surface into better order. With a short 270 °C anneal, the sheet conductance curve changes dramatically. The minimum in the curve shifts to more positive gate voltages, and the curve itself becomes distinctly narrower and more symmetric, as is shown in Fig. 4. A sharp 1×1 LEED pattern appears after the anneal, while no LEED pattern can be observed on the as-prepared H-terminated surface. This behavior is also frequently observed in STM studies of the H/Si(001) surface [43].

One can explain the drastic change in the sheet conductance-voltage curve by the removal of donorlike states. Figure 4 shows that the left part of the *G-V* curve stays almost the same. It is known from our simulation that this part is mainly determined by the Si/SiO_2 interface, suggesting no change happens at the BOX interface. On the other hand, the right part of the conductance-voltage curve becomes much steeper after the annealing, indicating a decrease of the total number of defects. Obviously, the decrease of localized states must come from the top surface. Because the curve shifts to more positive voltages after the annealing, the change in surface charge is thus of positive sign, pointing to donorlike states. The decrease in $D_{\mathrm{IT|H\,donor}}$ unpins the surface Fermi level, and the characteristic asymmetric *G-V* curve due to the imbalance between acceptor and donor states disappears.

These observations alone cannot distinguish between removal of adventitious adsorbates or ordering of H on the surface when the surface is annealed, nor can the sharpening of the LEED pattern or the ability to see STM images after annealing distinguish between these choices. However, the following might bias the conclusion in one direction. We have the ability to dose the surface *in situ* with monatomic H. A clean surface dosed with H assumes the broad shape of the conductance curves for the original HF-terminated surface [45,46]. Thus, disordered clean, atomic H can have the same effect as a HF treatment. We, therefore, favor a conclusion that the states that low-temperature annealing removes appear to be caused by very loosely bound (e.g., physisorbed) or easily transformable H species.

V. CONCLUSION

We characterize H-terminated Si(001) surfaces using a contactless NM conductance method [23]. The contribution that this method makes to the general problem of surface states on clean or chemically modified surfaces is the ability to identify different states and quantify their relative contributions, as fits to the sheet conductance-voltage curves are extremely sensitive to the nature and density of states. For H-terminated Si(001), donorlike states at a density in the high 10^{11} $\mathrm{cm^{-2}\,eV^{-1}}$ range are found to exist on the surface. Low-temperature annealing easily removes or transforms these states. Their origin is uncertain, as we explain above. The simplest explanation is that adventitious contamination is removed with a soft anneal; however, dosing a clean surface with atomic H *in situ* produces quite similar conductance curves as found for HF-terminated surfaces [45,46].

The use of very thin sheets and back-gated van der Pauw measurements described here can readily be applied to other surface terminations and other semiconductor systems. For semiconductor surfaces other than Si, the influence of surface chemistry on charge transport is even less well known. For example, in III-V semiconductors, surface terminations that significantly lower the surface defect density would largely improve the technological development of III-V semiconductors. Accurate surface electrical characterization will also benefit the development of semiconductor surface passivation chemistries.

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