Letter

Fast Low-Current Spin-Orbit-Torque Switching of Magnetic Tunnel Junctions through Atomic Modifications of the Free-Layer Interfaces

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Future applications of spin-orbit torque will require new mechanisms to improve the efficiency of switching nanoscale magnetic tunnel junctions (MTJs), while also controlling the magnetic dynamics to achieve fast nanosecond-scale performance with low-write-error rates. Here, we demonstrate a strategy to simultaneously enhance the interfacial magnetic anisotropy energy and suppress interfacial spin-memory loss by introducing subatomic and monatomic layers of Hf at the top and bottom interfaces of the ferromagnetic free layer of an in-plane magnetized three-terminal MTJ device. When combined with a β-W spin Hall channel that generates spin-orbit torque, the cumulative effect is a switching current density of $5.4 \times 10^6\ \mathrm{A/cm^2}$.

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I. INTRODUCTION

Spin-orbit torque (SOT) from the spin Hall effect (SHE) [1–8] in heavy metals (HMs) can rapidly and reliably switch an adjacent ferromagnet (FM) free layer of a nanoscale magnetic tunnel junction in a three-terminal configuration (3T MTJ). This effect provides the strategy for a fast current- and energy-efficient cache magnetic memory [9–15]. The separate read and write channels in the 3T MTJ geometry offer additional advantages: faster readout without read disturbance and lower write energy. While the development of SOT switching has focused primarily on nanoscale *perpendicularly magnetized* (PM) MTJs, their SOT effective-field switching requires much higher currents than can be provided by a reasonably scaled CMOS transistor (current densities in the SH channel are $\geq 1.4 \times 10^8\ \mathrm{A/cm^2}$) [16], and fast low-write-error-rate (WER) switching has not yet been demonstrated. SOT switching of a PM MTJ also requires an in-plane bias field to obtain deterministic reversal, but strategies have been recently demonstrated where an antiferromagnetic pinning layer or an electric field successfully provides this bias field [5,17,18]. Here, we report a dramatic performance improvement for *in-plane-magnetized* (IPM) 3T MTJs, wherein the strong SOT arising from nanochannels of β-phase W is combined with two recently discovered effects of Hf atomic layer modifications of the FM-MgO and HM-FM interfaces that, respectively, enhance the interfacial perpendicular magnetic anisotropy (PMA) energy density [19] and reduce interfacial spin-memory loss [20]. The result is an antidamping SOT switching current density of just $5.4 \times 10^6\ \mathrm{A/cm^2}$. We also achieve reliable (WER approximately equal to 10^{-6}) switching with 2-ns pulses, which we tentatively attribute, at least in part, to the beneficial assistance of the fieldlike SOT arising from the spin current generated by the W spin Hall effect.

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II. RESULTS AND DISCUSSION

The high-performance 3T MTJ devices reported here are lithographically patterned from a thin-film multilayer stack sputter deposited onto an oxidized Si wafer consisting of $\mathrm{W(4.4)/Hf(0.25)/Fe_{60}Co_{20}B_{20}(1.8)/Hf(0.1)/MgO(1.6)/Fe_{60}Co_{20}B_{20}(4)/Ta(5)/Ru(5)}$ (thickness in nanometers), where W represents the high-resistivity β phase of W [21]. In Fig. 1(a), we show a schematic of the W-based 3T MTJ device structure along with (inset) a scanning-electron-microscope (SEM) image of a typical elliptical nanopillar MTJ on top of the W SHE channel after it is defined by electron-beam lithography and argon ion milling.

A. Low critical switching current

We demonstrate the potential of these W-based IPM 3T MTJ devices by reporting in detail on the representative performance of a high-aspect-ratio $(190 \times 30\ \mathrm{nm^2})$ MTJ device fabricated on a 480-nm-wide W channel. This device is annealed in an air furnace at 240 °C for 1 h after patterning to increase the tunneling magnetoresistance (TMR) of the MTJ and also reduce the switching current, as we discuss below. In the inset to Fig. 1(b), we first show the minor magnetic loop response of the MTJ resistance as an in-plane magnetic field H_{ext} is applied along the long

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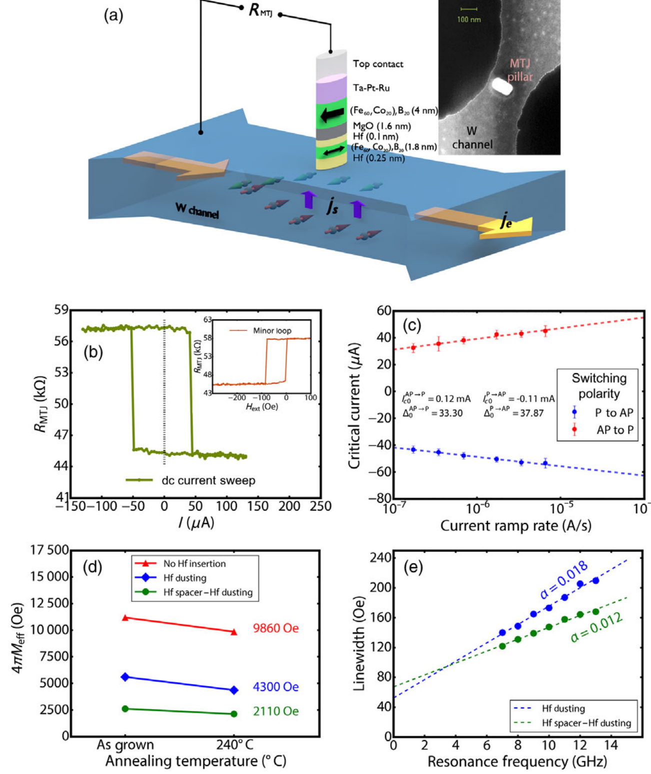

FIG. 1. Hf-spacer–Hf-dusting sample annealed at 240 °C. (a) The Hf-spacer–Hf-dusting sample structure and measurement schematics. Inset: SEM image shows a representative nanopillar situated on a W channel after *e*-beam exposure, development, and ion-beam etching. (b) Current-induced switching loop of the MTJ free layer showing a thermally assisted switching current of 50 μA. The device is 190×30 nm^2 and is situated on a 480-nm-wide W channel. Inset: In-plane field-switching minor loop of the free layer. (c) Current ramp rate measurement on the device of (b). Fitting to the macrospin model gives a zero-thermal-fluctuation critical current of 115 μA with a thermal stability factor of 35.6. (d) The free layer demagnetization field change with annealing temperature for a Hf-spacer–Hf-dusting sample compared to that of a Hf-dusting-only sample and a sample without Hf insertion as measured by flip-chip FMR. M_{eff} significantly decreases in the samples with Hf dusting due to enhanced interfacial perpendicular anisotropy. (e) Linewidths at different resonance frequencies (applied fields) for the Hf-dusting-only sample and the Hf-spacer–Hf-dusting sample measured by flip-chip FMR. Both samples are annealed at 240 °C. The damping decreases significantly with the insertion of the 0.25-nm Hf spacer.

axis of the MTJ device and ramped over ± 300 Oe, which is sufficient to reverse the orientation of the thin bottom free layer of the MTJ from being parallel (P) to antiparallel (AP) to the thicker $Fe_{60}Co_{20}B_{20}$ reference layer but not strong enough to reverse the orientation of the reference layer due to its stronger shape anisotropy. The horizontal offset of the minor loop (approximately -50 Oe) is due to the dipole field from the reference layer. All subsequent SOT measurements are taken when this offset is canceled by an appropriate H_{ext} [21].

In the main part of Fig. 1(b), we show the characteristic dc SOT hysteretic switching behavior of the IPM 3T MTJ as the bias current in the W channel is ramped quasistatically. The switching polarity is consistent with the negative spin Hall sign of β-W in comparison to that of platinum [4,22]. For nanoscale MTJs, thermal fluctuations assist the reversal during slow current ramps. Within the macrospin or rigid monodomain model, the critical current I_c that is observed is dependent on the current ramp rate [23],

$$I_c = I_{c0}\left\{1 - \frac{1}{\Delta}\ln\left[\frac{1}{t_0\Delta}\left(\frac{|I_{c0}|}{|\dot{I}|}\right)\right]\right\}. \tag{1}$$

Here, I_{c0} is the critical current in the absence of thermal fluctuation, $\dot{I}$ is the current ramp rate, Δ is the thermal stability factor that represents the normalized magnetic energy barrier for reversal between the P and AP states, and τ_0 is the thermal attempt time, which we assume to be 1 ns. To characterize the SOT behavior of this device, we measure the mean switching current for $\dot{I}$ varying from 10^{-7} to 10^{-5} A/s [Fig. 1(c)]. By fitting to Eq. (1), we obtain nearly symmetric SOT switching results with an averaged zero-fluctuation switching current of $|I_{c0}| = 115$ μA and $\Delta = 35.6$. With the W channel width $w_{\mathrm{SH}} = 480$ nm and thickness $t_{\mathrm{SH}} = 4.4$ nm, this corresponds to a switching current density $J_{c0} = 5.4 \times 10^6$ A/cm^2, more than 3 times lower than reported originally for a W-based 3T MTJ [4].

In Table I, we compare the critical switching current density J_{c0} achieved in various in-plane and out-of-plane 3T structures. The different types of SOT devices have different minimum sizes as determined by thermal stability requirements, which, in turn, set the current amplitude required for switching or domain-wall motion. For the PMA SOT nanodot devices, currently a 40 nm diameter is required [16], which necessitates a minimum current of approximately 300 μA for reversal using a 40-nm-wide, 4-nm-thick β-W spin Hall channel. In comparison, our IPM 3T MTJ 190×30 nm^2 device requires a switching current of approximately 40 μA for a 190-nm-wide channel.

B. Fast and reliable pulse switching

The critical question is whether these W-based IPM 3T MTJ devices can also exhibit fast reliable switching with low-amplitude current pulses as required for high-speed cache memory. Aradhya *et al.* have recently reported nanosecond-time-scale switching of Pt-based IPM 3T MTJs with low WER [22], but a high-current pulse amplitude was required, 2–3 I_{c0} with $I_{c0} > 500$ μA. To characterize the performance of the W-based 3T MTJ device in the short-pulse regime, we separately measure the switching phase diagram for the two cases P → AP and AP → P using a fast-pulse measurement method [21]. The results are shown in Figs. 2(a) and 2(b), where each data point is the statistical result of 1000 switching attempts, with the scale bar on the right showing the switching

TABLE I. Comparison of J_{c0} between the different 3T MTJ structures reported to date.

	W with Hf insertion layers	W	Pt	Ta	PMA W/(Co, Fe)B/MgO nanodot	PMA MTJ with Ta channel	3T DW motion device
Anisotropy	In-plane magnetized				PMA		
Critical current density (x10^6 A/cm^2)	5.4	18	40	32	>140	>50	>50
Reference	This work	Pai *et al.* [4]	Aradhya *et al.* [22]	Liu *et al.* [2]	Fukami and Ohno [16]	Cubukcu *et al.* [15]	Fukami *et al.* [24]

probability. Although micromagnetic modeling indicates that for strong short pulses these 3T MTJ devices do not reverse simply as a rigid domain [22], we can still utilize the macrospin model [25] as an approximation to characterize the short-pulse response by fitting the 50% switching probability boundary between the switching and non-switching regions with

$$V = V_0\left(1 + \frac{\tau_0}{t}\right). \quad (2)$$

The results shown in the solid curves provide a reasonable fit to the data despite the simplifying macrospin assumption. From these fits, we extract the characteristic switching times τ_0 and critical switching voltages V_0 to be 0.76 ns and 0.48 V for P → AP and 1.20 ns and 0.44 V for AP → P. The short-pulse critical switching current (current density) as calculated from V_0 and the channel resistance $R \approx 3.6$ kΩ is $I_{c0} \approx 120$ μA ($J_{c0} \approx 5.9 \times 10^6$ A/cm^2), consistent with the ramp rate results.

For the cache memory, the SOT reversal has to be both fast and highly reliable, and in this latter regard, our results with this W-based IPM 3T MTJ approach offer encouraging prospects as indicated by Fig. 2(c), where we show the WER results measured with 2-ns pulses on the same device. We apply square switching pulses of increasing voltages to the W channel and record states of the device after each switching pulse. For every voltage level, we repeat the switching attempts 10^6 times and calculate the WER based on switching probability WER = 1-P_{switch}. At 2 ns, WER close to 10^{-6} is achieved for both polarities P → AP and AP → P, which indicates the potential of this approach for high reliability. Note that our current results are limited to 10^{-6} WER ($V \leq 3.5V_0$) due to the constraint on the highest pulse voltage we can apply to the channel imposed by a less than optimal electrode design (spreading resistance) and a poor-quality field insulator. Straightforward improvements in both should lower V_0 and enable measurements with $V \gg V_0$.

The observed antidamping SOT reversal on the $\tau_0 \leq 1$ ns time scale is much faster than predicted by the rigid domain, macrospin model. A key conclusion in the initial report on fast switching with Pt-based IPM 3T MTJs is that the in-plane Oersted field H_{Oe} generated by the pulsed current is advantageous in promoting the fast reliable switching because it opposes the anisotropy field H_c of the free layer at the beginning of the reversal [22,26]. Because of the opposite sign of the SHE for W-based 3T MTJs, the pulsed H_{Oe} in our case is parallel to H_c at the beginning of the pulse, which micromagnetic modeling indicates should be disadvantageous for very fast reversal [22]. However we make spin-torque ferromagnetic

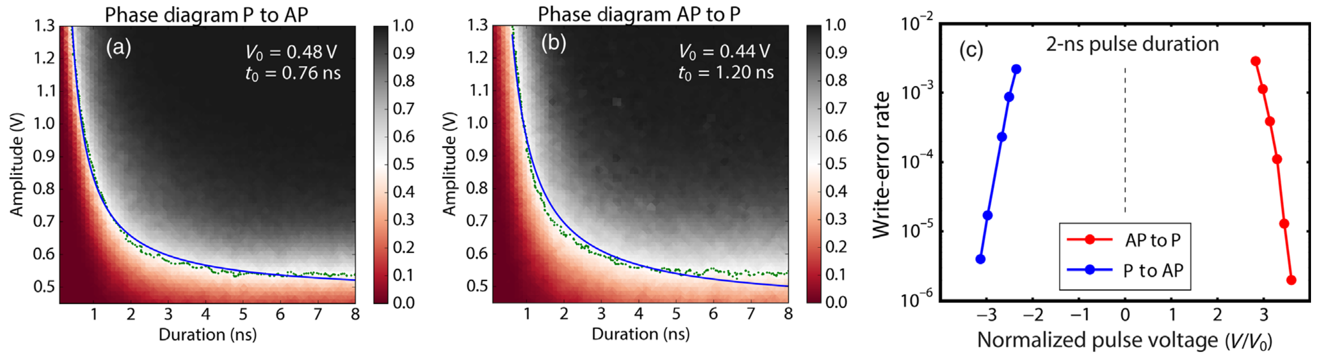

FIG. 2. Fast and reliable pulse switching of a Hf-spacer–Hf-dusting sample. Pulse-switching phase diagrams and macrospin fits for polarities P → AP (a) and AP → P (b), respectively, with the switching probability scale bar on the right. Each point is a result of 10^3 switching attempts. A characteristic switching time of approximately 1 ns and a critical voltage of 0.46 V are obtained after fitting 50% probability points (green points) to the macrospin model. (c) WER measurement results for 2-ns square pulses applied to the device (a) and (b). Each point is a result of 10^6 switching attempts. WER of approximately 10^{-6} is obtained at sufficiently high-voltage (current) amplitudes for both polarities.

resonance (ST FMR) measurements on W(4)/Hf(0.25)/$Fe_{60}Co_{20}B_{20}(t_{Fe_{60}Co_{20}B_{20}})$/Hf(0.1)/MgO/Ta microstrips that are annealed at 240 °C for 1 h to determine both the *dampinglike* (DL) and the *fieldlike* (FL) spin-orbit torque efficiencies ξ_{DL} and ξ_{FL} of this heterostructure, and we obtain $\xi_{DL} = -0.20 \pm 0.03$ and $\xi_{FL} = -0.0364 \pm 0.005$ [21]. This *fieldlike* torque efficiency corresponds to an effective field -6.68×10^{-11} Oe/(A/m^2) in the MTJ structure with a 1.8-nm free layer that is oriented in opposition to the Oersted field generated by the electric current, as previously reported for W devices [4], and approximately 3 times larger. Thus, the net transverse field is in opposition to the free layer in-plane anisotropy field at the beginning of the reversal and, hence, may be playing an important role in the fast, reliable W-based 3T MTJ results reported here.

C. Hf dusting and Hf spacer

In addition to utilizing the high-spin-torque efficiency of β-W, we employ two other material enhancements—the submonolayer "dusting" and monolayer "spacer" of Hf that are inserted, respectively, between the free layer and the MgO and between the W and the free layer, to achieve this exceptionally low-pulse-current (density) switching performance. For 3T MTJs, the SOT switching current density within the macrospin model is predicted to vary as [27,28]

$$J_{c0} = I_{c0}/w_{SH}t_{SH} = \frac{2e}{\hbar}\mu_0 M_s t_{FM}\alpha(H_c + M_{eff}/2)/\xi_{DL}, \quad (3)$$

where e is the electron charge, $\hbar$ is the reduced Plank constant, μ_0 is the permeability of free space, M_s is the saturation magnetization of the free layer, and t_{FM} is the free layer's effective magnetic thickness, which are measured to be 1.2×10^6 A/m and 1.7 nm [21], $M_{eff} = M_s - K_s/t_{FM}$ is the free layer's effective demagnetization field, where K_s is the interfacial perpendicular magnetic anisotropy energy density, and α is the effective magnetic damping constant of the free layer. To compare our experimental results with the prediction of Eq. (3), we conduct a flip-chip FMR measurement [21] of an unpatterned section of the wafer to determine $M_{eff} = 2110$ Oe and $\alpha = 0.012$. With these parameter values, we calculate from Eq. (3) that $\xi_{DL} = -0.15 \pm 0.03$ for the measured device, a bit lower than the result from the ST FMR measurement of a larger-area microstrip of the same heterostructure composition [21]. This difference may be due to an increase in damping due to side-wall oxidation of the nanopillar in the lithography process, which can be addressed by *in situ* passivation in the future [29].

The benefits of the Hf insertion layers for reducing the critical current for SOT switching are illustrated by comparisons with FMR measurements performed on two control samples, one with only the Hf dusting, W(4)/$Fe_{60}Co_{20}B_{20}$(1.8)/Hf(0.1)/MgO(1.6)/$Fe_{60}Co_{20}B_{20}$(4)/Ta(5)/Ru(5) and one without either Hf layer W(4)/$Fe_{60}Co_{20}B_{20}$(1.8)/MgO(1.6)/$Fe_{60}Co_{20}B_{20}$(4)/Ta(5)Ru(5).

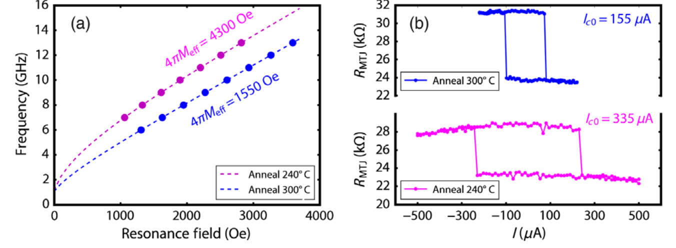

FIG. 3. Temperature dependence of the Hf-dusting effect. (a) Flip-chip FMR measurement on two Hf-dusting-only samples annealed at 240 °C (magenta) and 300 °C (blue), respectively, showing a further reduction of M_{eff} at higher annealing temperature. (b) Current-induced switching of Hf-dusting-only samples annealed at two different temperatures, 240 °C (magenta) and 300 °C (blue). The spin-torque switching loops indicate a substantial reduction in critical current with the higher-temperature anneal as quantified by the results of ramp rate measurements of I_{c0}.

Consistent with a previous report that Hf dusting can greatly enhance the perpendicular magnetic anisotropy energy density K_s at FM/MgO interfaces [19], we find that M_{eff} for the Hf-dusting-only structure is reduced to 4300 Oe compared to 9860 Oe for the W MTJ system without Hf [Fig. 1(d)]. We confirm with switching experiments that this reduction of M_{eff} indeed significantly reduces the critical switching current [21]. The additional reduction to $M_{eff} = 2110$ Oe for the sample with the added Hf spacer can be attributed to some of the Hf diffusing through the $Fe_{60}Co_{20}B_{20}$ to the MgO interface during the anneal [20,30]. Another benefit of the Hf spacer is that its insertion decreases α very substantially from 0.018 to 0.012 [Fig. 1(e)], which we attribute to a passivation of the W surface that suppresses the reaction between the W and $Fe_{60}Co_{20}B_{20}$ that otherwise results in interfacial spin-memory loss [31]. While there is some spin-current attenuation from the use of the Hf spacer [20,32], its effectiveness in lowering the effective damping and M_{eff} substantially outweighs the cost.

The integration of magnetoresistive random-access memory with CMOS usually requires thermal processing above 240 °C. Annealing at higher temperatures can also be beneficial in producing higher TMR. The 190×30 nm^2 free layers analyzed above become thermally unstable due to further decrease in M_{eff} after annealing at 300 °C, but it is important to note that the Hf-dusting technique itself becomes even more effective after processing at $T \geq 300$ °C. We perform FMR measurements on an unpatterned section of the wafer with only the 0.1-nm Hf-dusting layer after it is annealed at 300 °C for 1 h. As illustrated in Fig. 3(a), raising the annealing temperature from 240 °C to 300 °C results in approximately a 2.5 × reduction in M_{eff} from 4300 to 1550 Oe, while there is no material effect on M_s [21], a compelling demonstration of the effectiveness of Hf dusting in enhancing K_s. To examine the SOT switching behavior of devices with such a low M_{eff}, we pattern larger 390×100 nm^2 and, hence, more thermally stable MTJs

from the wafer and anneal two of them at the two different temperatures 240 °C and 300 °C, respectively. Consistent with the M_{eff} change, we see clean SOT switching with a much lower critical current $I_{c0} = 155\ \mu\mathrm{A}$ after 300 °C annealing temperature in comparison to the 240 °C critical current $I_{c0} = 335\ \mu\mathrm{A}$.

III. CONCLUSION

In summary, we achieve nanosecond-scale, reliable, low-amplitude pulse current switching in W-based IPM 3T MTJs by utilizing a partial atomic layer of Hf dusting between the free layer and the MgO, which very effectively reduces M_{eff} of the free layer, while a further reduction in the required pulse amplitude is achieved by inserting approximately one Hf monolayer between the HM and FM, which significantly reduces interfacial spin-memory loss. This ability to achieve a low M_{eff} with a relatively thick free layer through the use of the particularly strong interfacial anisotropy effect of Hf—O—Fe bonds [19] enables us to minimize the detrimental effect of interfacial enhancement of magnetic damping, and, due to the thicker free layer, it arguably also hinders the formation of localized nonuniformities during the fast reversal that otherwise results in write errors.

Further decreases in I_c, to well below 100 μA, should be quite straightforward with refinements in the device design. For example, to ensure successful fabrication, the major axis of our elliptical MTJ nanopillars is less than 50% of the width of the spin Hall channel so that up to a factor of 2 reduction in I_c can be expected simply with more aggressive, industry-level lithography. Smaller nanopillars on even narrower channels, ≤100 nm, should be possible through the use of slightly thicker free layers (approximately 2 nm) to promote thermal stability, with the robust interfacial magnetic anisotropy effect of the Hf-dusting technique providing the means to still achieve a low M_{eff}. We anticipate that these approaches, in conjunction with an improved device geometry that substantially reduces the spreading resistance, should lower the pulse write current for fast, reliable switching to approximately 20 μA and the write energy to the ≤10 fJ scale.

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