Transistor Concepts Based on Lateral Heterostructures of Metallic and Semiconducting Phases of MoS_2

Damiano Marian,[1] Elias Dib,[1] Teresa Cusati,[1] Enrique G. Marin,[1] Alessandro Fortunelli,[2] Giuseppe Iannaccone,[1,*] and Gianluca Fiori[1]

[1]*Dipartimento di Ingegneria dell'Informazione, Università di Pisa, Via G. Caruso 16, 56122 Pisa, Italy*
[2]*CNR-ICCOM, Istituto di Chimica dei Composti Organometallici, Via G. Moruzzi 1, 56124 Pisa, Italy*

(Received 19 June 2017; revised manuscript received 21 September 2017; published 27 November 2017)

We propose two transistor concepts based on lateral heterostructures of monolayer MoS_2, composed of adjacent regions of 1*T* (metallic) and 2*H* (semiconducting) phases, inspired by recent research showing the possibility to obtain such heterostructures by electron-beam irradiation. The first concept, the lateral heterostructure field-effect transistor, exhibits the potential of better performance with respect to the foreseen evolution of CMOS technology, both for high-performance and low-power applications. Performance potential is evaluated by means of detailed multiscale materials and device simulations. The second concept, the planar barristor, also exhibits potential competitive performance with CMOS, and an improvement of orders of magnitude in terms of the main figures of merit with respect to the recently proposed vertical barristor.

DOI: 10.1103/PhysRevApplied.8.054047

I. INTRODUCTION

Engineering alternative materials with tailored properties for electronic applications is the quintessential frontier of electronics. It was embodied in the "band-gap engineering" [1] or "band-structure engineering" [2] paradigm of III–V materials systems in the 1980s, and it is embodied now in the "materials-on-demand" paradigm [3] of "van der Waals heterostructures" [4], where 2D materials of incommensurable lattice, including a broad set of atomic species, are stacked to create alternative 3D materials.

One can also have "lateral heterostructures" [5], as in the example by Levendorf *et al.* [6], where a planar heterostructure of graphene and hexagonal boron nitride has been fabricated by successive graphene growth, patterning, and boron nitride regrowth in the same 2D sheet, exploiting the almost ideal lattice match.

With lateral and vertical heterostructures of 2D materials, the prospect emerges of combining materials with different electronic properties, such as semiconductors, insulators, and metals, in order to engineer materials for particular applications.

In this paper, we focus on monolayer MoS_2. The advantage of designing devices made of 2D materials relies on an excellent electrostatic control of the channel by the gate. MoS_2 also has a direct band gap between 1.5 and 1.8 eV, which makes it favorable for digital applications against other 2D materials such as graphene, which does not present a gap. MoS_2 has already shown remarkable electronic and optoelectronic properties [7], including a higher mobility than ultrathin silicon and germanium, and the possibility to be used in flexible electronic circuits, which is currently out of reach for silicon technology [8].

Molybdenum disulphide has also been used in vertical heterostructure devices, such as atomically thin *p*-*n* heterojunctions [9] combining monolayer *n*-type MoS_2 and *p*-type WSe_2, which shows a rectifying behavior. Also, lateral heterostructures based on junctions of 1*T* and 2*H* phases have been proposed experimentally showing interesting and promising properties [10–12].

An intriguing property of MoS_2, which is decisive for the realization of lateral heterostructures, is that, by high-dose electron-beam irradiation, one can induce a phase transition from the semiconducting phase (2*H*) to the metallic phase (1*T*) in a size-controllable region [13]. This property enables, in principle, top-down patterning of MoS_2 lateral 2*H*-1*T* heterostructures, whose in-plane charge-transport properties critically depend on the quality of the lateral heterointerface.

The first demonstration of a Schottky diode, through the patterning of a lateral heterostructure with a metal region (1*T*-MoS_2) and a semiconducting region (2*H*-MoS_2), has already been reported [14]. Here, we exploit the possibility of fabricating lateral heterostructures in single-layer MoS_2 to explore two device concepts, evaluating by multiscale simulations its potential performances.

The first transistor concept is a lateral heterostructure field-effect transistor (LH FET), which is shown in Fig. 1(a): It is a double-gate FET in which the channel consists of single-layer molybdenum disulfide. We have the semiconducting phase in the central region aligned with the gate, and the metallic phase in the source and drain extensions. The gate dielectric is silicon oxide with a thickness of 0.5 nm. It can be seen as an embodiment of the LH FET proposed in 2011 for the graphene–boron nitride heterostructure [15,16].

*g.iannaccone@unipi.it

 © 2017 American Physical Society

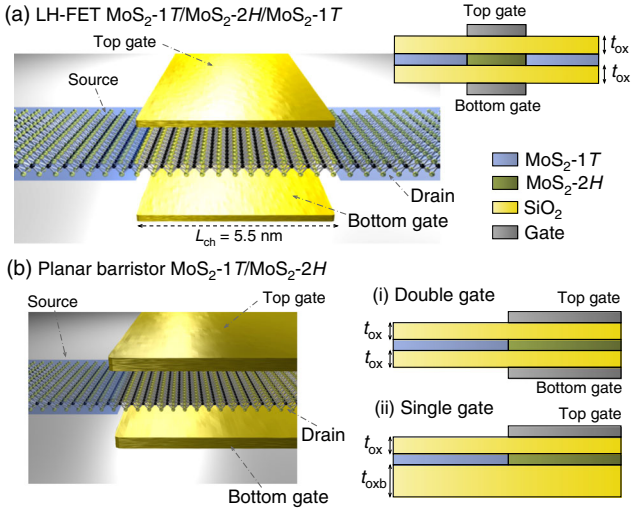

FIG. 1. (a) MoS_2-2H/MoS_2-1T/MoS_2-2H double-gate FET. The source, drain, bottom gate, top gate, and channel length ($L_{ch} = 5.5$ nm) are indicated. The oxide is SiO_2, with thickness $t_{ox} = 0.5$ nm. (Inset) Longitudinal cross section of the device. (b) Double-gate MoS_2-1T/MoS_2-2H planar barristor. (Inset i) Longitudinal cross section of the double-gate device, with $t_{ox} = 0.5$ nm. (Inset ii) Longitudinal cross section of a single-gate configuration, where t_{oxb} is the bottom oxide thickness.

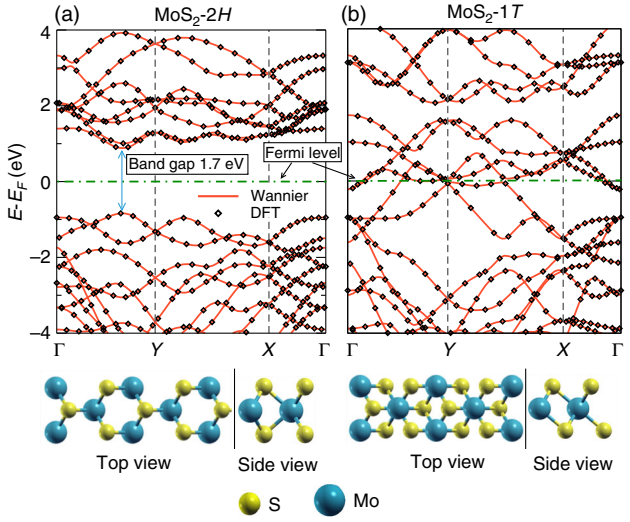

FIG. 2. Bands of (a) MoS_2-2H and (b) MoS_2-1T computed with DFT calculations (the black dots) and with MLWF (the red solid lines, 22 bands). Below each panel, the schematic top and side views of the two different atomic-structured monolayers, (a) MoS_2-2H and (b) MoS_2-1T, are shown.

The second transistor concept is a lateral gated Schottky diode [Fig. 1(b)] with a metallic source (1T-MoS_2) and a semiconducting drain (2H-MoS_2). We consider a double-gate structure with a gate oxide thickness t_{ox} [Fig. 1(b)(i)] and a single- (top-) gate configuration with a top oxide thickness t_{ox} and a bottom oxide thickness t_{oxb} [Fig. 1(b)(ii)]. The gate voltage modulates the height of the Schottky barrier—and therefore the current. We call this transistor a "planar barristor" because the operating principle is similar to that of the vertical barristor proposed in 2012 [17].

II. THEORY

In order to explore the viability and potential performance of such devices, we adopt a first-principles multiscale modeling approach [18], articulated in three steps. We start from density-functional-theory (DFT) simulations of the electronic properties of 1T-2H heterostructures, from which we obtain a Hamiltonian defined on the basis of plane waves. From this, we then extract a Hamiltonian on a maximally localized Wannier function (MLWF) basis set. Finally, the resulting Hamiltonian is used in the open-source device simulator NanoTCAD ViDES [19], based on a nonequilibrium Green's-function formalism, to investigate the device performance for digital applications.

Ab initio calculations are performed with Quantum Espresso [20], using an $8 \times 12 \times 1$ Monkhorst-Pack grid, ultrasoft pseudopotentials, and the Perdew-Burke-Ernzerhof (PBE) exchange-correlation functional. A 60-Ry wave-function cutoff, a 600-Ry charge-density cutoff, and a vacuum layer of 20 Å, to avoid interactions with periodic replicas, are considered. The band structure and the Hamiltonian in the MLWF basis are computed with Wannier90 [21] using the same grid as in DFT calculations. The obtained tight-binding-like Hamiltonian is then included in the open-source device simulator NanoTCAD ViDES [19]. Specifically, we simplify the full 22-band electronic structure model of Fig. 2 into a six-band model, which provides the same results for energies close to the Fermi energy, but with reduced computational requirements (see the Appendix). Then we include the six-band tight-binding-like Hamiltonian in the ViDES framework to compute transport in far-from-equilibrium conditions. In order to connect the two different phases of MoS_2 along the transport direction, the off-diagonal elements of the Hamiltonian are chosen to be equal to the MoS_2-2H elements (details of the method are reported in the Appendix). For all devices, we consider operation at a temperature of 300 K and with fully coherent quantum transport.

The complete multiscale approach is thoroughly discussed in Bruzzone *et al.* [18] and in the Appendix.

III. RESULTS AND DISCUSSION

The band structures of MoS_2-2H and MoS_2-1T are shown in Figs. 2(a) and 2(b), respectively, where dots correspond to DFT calculations, and dashed lines to results using the MLWF basis. As apparent from Fig. 2, MoS_2-2H has a gap of 1.7 eV, whereas the 1T phase shows metallic behavior.

The transfer characteristics (I_{DS}-V_G) of the LH FET are shown in Fig. 3(a) in the linear scale and Fig. 3(b) in the semilogarithmic scale for MoS_2-2H channel and gate lengths ranging from 2.75 to 9.9 nm. The applied

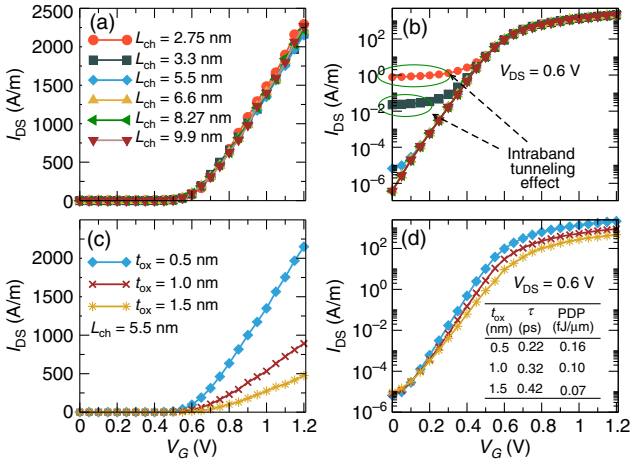

FIG. 3. Transfer characteristics in (a) the linear and (b) the semilogarithmic scale of the devices in Fig. 1(a), for different MoS_2-2H channel lengths and for $V_{DS} = 0.6$ V for an oxide thickness of $t_{ox} = 0.5$ nm, and (c) linear and (d) semilogarithmic for a MoS_2-2H channel length of 5.5 nm, $V_{DS} = 0.6$ V and for different oxide thicknesses. (Inset) τ and PDP values, calculated for a high-performance process, are reported.

drain-to-source voltage V_{DS} is 0.6 V and the oxide thickness t_{ox} is 0.5 nm. In the case of shorter channel lengths (2.75 and 3.3 nm), intraband tunneling dominates the current and imposes a lower limit on the off-state current.

To assess device performance, we use as a benchmark the consensus on the evolution of CMOS technology represented by the 2015 edition of the International Technology Roadmap for Semiconductors (ITRS) [22]. The ITRS considers CMOS processes to be optimized either for high-performance (HP) or for low-power (LP) applications, and they therefore have different threshold voltages. To enable comparison with the ITRS, we consider two main bias conditions for the n-type MOSFET: the off state, corresponding to $V_{GS} = V_{off}$ and $V_{DS} = V_{DD}$, where V_{DD} is the supply voltage, and the *on* state, corresponding to $V_{GS} = V_{off} + V_{DD}$ and $V_{DS} = V_{DD}$. For a HP process, V_{off} is defined as the gate voltage for which the drain current in the *off* state is $I_{off} = 100$ nA/μm. For a LP process, in order to reduce the static power consumption, V_{off} is defined as the gate voltage for which the device current is $I_{off} = 100$ pA/μm. Typically, the transfer characteristics are shifted by properly tuning the gate work function for each process in order to obtain $V_{off} = 0$ V.

For all of the channel lengths of the LH FETs, we consider the same supply voltage $V_{DD} = 0.6$ V and the same oxide thickness t_{ox}. The main figures of merit for the two process optimizations are reported in Table I. The subthreshold swing (SS) is defined as the inverse slope of the $I_{DS} - V_{GS}$ curve in semilogarithmic scale in the subthreshold regime. We also report the I_{on}/I_{off} ratio, where I_{on} is the current in the *on* state. As previously mentioned, the 2.75-nm and 3.3-nm FETs have a large intraband tunneling current in the *off* state, so that I_{off} cannot be defined for the LP case for $L_{ch} = 3.3$ nm, while, for $L_{ch} = 2.75$ nm, I_{off} cannot be defined for both the LP and HP cases. We remark that the band gap calculated through DFT is underestimated: With a GW correction, the band gap could increase to 2.1 eV, slightly reducing the intraband tunneling effects observed in the shortest channels.

In Table I, we also show the intrinsic delay time τ, which is a measure of the switching speed (a rough estimation of the switching time of a CMOS inverter), defined as

$$\tau = \frac{Q_{on} - Q_{off}}{I_{on}} \tag{1}$$

where Q_{on} and Q_{off} represent the total charge in the channel in the *on* and *off* states, respectively. In addition, we show the power-delay product (PDP), which is a measure of energy efficiency (roughly proportional to the energy required to switch a logic gate),

$$\mathrm{PDP} = V_{DD} I_{on} \tau = V_{DD}(Q_{on} - Q_{off}). \tag{2}$$

TABLE I. Figures of merit for different channel lengths of the LH FET and the DG planar barristor for HP and LP.

		High performance					Low power			
		SS (mV/dec)	I_{on}/I_{off}	τ (ps)	PDP (fJ/μm)	f_T (THz)	SS (mV/dec)	I_{on}/I_{off}	τ (ps)	PDP (fJ/μm)
LH FET	$L_{ch} = 3.3$ nm [a]	102	1.0×10^4	0.16	0.10	3				
($V_{DS} = 0.6$ V)	$L_{ch} = 5.5$ nm	69	1.18×10^4	0.22	0.16	2	72	4.38×10^6	0.44	0.12
	$L_{ch} = 6.6$ nm	69	1.20×10^4	0.25	0.18	1.5	70	4.43×10^6	0.49	0.13
	$L_{ch} = 8.27$ nm	69	1.23×10^4	0.30	0.22	1.4	68	4.65×10^6	0.47	0.13
	$L_{ch} = 9.9$ nm	69	1.25×10^4	0.35	0.26	1.0	69	4.41×10^6	0.61	0.16
Planar Barristor	DG	68.5	9.8×10^3	0.14	0.055	3	72.5	3.5×10^5	1.2	0.017
($V_{DS} = 0.4$ V)	SG ($t_{oxb} = 0.5$ nm)	73	4.4×10^3	0.16	0.028	2.8	79	1.5×10^5	1.8	0.011
	SG ($t_{oxb} = 5$ nm)	79	3.7×10^3	0.2	0.029	2.3	85	7.4×10^4	4.4	0.013

[a]For a channel length of 3.3 nm, I_{off} is not defined for the LP case because of the high degradation of the *off* current due to the intraband tunneling effect (see the text for further details).

Finally, we report the cutoff frequency computed for $V_{DS} = V_{DD}$ as

$$f_T = \frac{1}{2\pi}\frac{\partial I_{DS}/\partial V_{GS}}{\partial Q_{\rm tot}/\partial V_{GS}}, \tag{3}$$

which is a relevant quantity for high-frequency analog applications.

From Table I, we can immediately draw that the LH FET exhibits an almost ideal SS = 68–72 mV/dec and $I_{\rm on}/I_{\rm off} > 10^4$ for channel lengths ≥ 5.5 nm for the HP case, and $> 10^6$ for the LP case. As expected, the HP case is optimized for low τ values (reaching 0.22 ps for the 5.5-nm channel length vs 0.44 ps of the LP case), whereas the LP case is optimized for a low PDP (reaching 0.12 fJ/μm for the 5.5-nm channel length vs 0.16 fJ/μm for the HP case).

As the channel length is reduced, we have a monotonic decrease of τ and PDP and an increase of f_T, meaning that both digital and analog performance is improving. However, for channel lengths of 3.3 nm, we observe a significant increase of the intraband tunneling leakage current, which reduces the $I_{\rm on}/I_{\rm off}$ value for the HP process and does not allow us to reach the required $I_{\rm off}$ for the LP case.

For comparison purposes, we also consider the performance of the LH FET for a less-aggressive gate-dielectric thickness (in terms of the equivalent silicon oxide thickness). In Figs. 3(c) and 3(d), we report the transfer characteristics for the LH FET with channel length of 5.5 nm, and for $t_{\rm ox} = 0.5$, 1.0, and 1.5 nm. The intrinsic delay time and the power-delay product for the HP case are reported in the inset of Fig. 3(d). As expected, τ increases and PDP decreases as the oxide thickness increases.

The second transistor concept we investigate is the planar barristor, which is shown in Fig. 1(b). We consider a double-gate (DG) planar device with a top and bottom silicon (or equivalent) oxide thickness $t_{\rm ox} = 0.5$ nm and a single-gate (SG) configuration with bottom oxide thicknesses of $t_{\rm oxb} = 0.5$ nm and $t_{\rm oxb} = 5$ nm.

In Fig. 4, we show the transfer characteristics for a planar barristor with $V_{DS} = 0.4$ V. The SS is reasonably good (SS < 79 mV/dec), and the $I_{\rm on}/I_{\rm off}$ is close to 10^4 when the high-performance case only when the structure is double gated. The same figures of merit computed for the LH FET are calculated for the planar barristor and reported in Table I. The barristor and the LH FET do not differ much in terms of electrostatic control of the channel-semiconductor region, and therefore both the PDP and τ show similar values for both devices when a double-gate geometry is considered. The single-gated barristor shows, however, sightly worse figures of merit for both the HP and LP applications, as compared to the double-gated device, due to the smaller gate-to-channel capacitance.

Finally, in Fig. 5, we compare the τ-vs-PDP data of the MoS_2 FETs studied in this work to predictions from the ITRS 2015 [22] for HP and LP CMOS technology and with simulations for the optimized graphene-based barristor studied in Ref. [16]. The most desirable region of the plot in Fig. 5 is, obviously, the bottom-left corner.

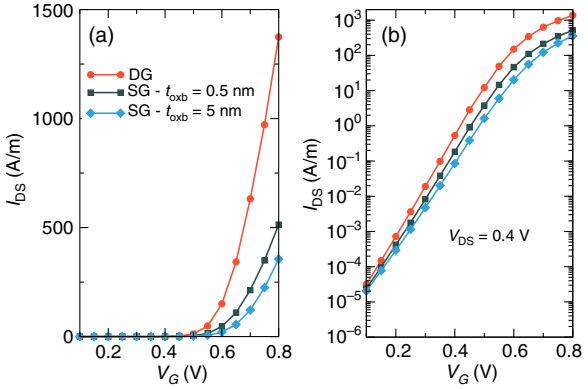

FIG. 4. Transfer characteristics in (a) the linear and (b) the semilogarithmic scale of the DG planar barristor, and of the SG planar barristors with $t_{\rm oxb} = 0.5$ nm and $t_{\rm oxb} = 5$ nm for $V_{DS} = 0.4$ V. The devices are illustrated in Fig. 1(b).

From the comparison, it appears that the LH FET and the planar barristor deliver a competitive expected performance with respect to CMOS technology, for both the HP and LP applications. The graphene vertical barristor misses the required values for the τ and PDP figures of merit by several orders of magnitude. As some of us have already discussed [23], the main problem is that, in the vertical

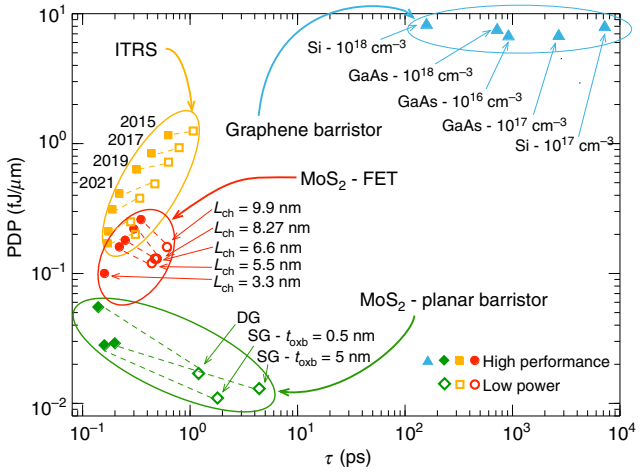

FIG. 5. PDP and τ values of the MoS_2 FETs studied in this work (red circles for the LH FET and green diamonds for the planar barristor) compared with the requirements of the ITRS 2015 [22] until the end of the road map (the yellow squares) and the graphene barristors studied in Ref. [23] (the blue triangles). Filled symbols correspond to figures of merit related to the HP process, empty symbols to the LP process. We assume for the graphene barristor a width of 1 μm. In the case of the graphene barristor of Ref. [16], results for the GaAs and Si substrates are shown for different values of the doping (the concentration is indicated for each device).

barristor, the source (the graphene sheet) is between the control gate and the barrier to be modulated, and it therefore adds a high parasitic capacitance to the gate, degrading the electrostatics—and hence the device performance. In the case of the planar barristor, however, the source is in the plane of the barrier, whereas the control gate is off plane, and therefore the parasitic capacitance is negligible. The proposed results provide an upper limit for the performance of transistors based on heterostructures of MoS_2. The actual device performance can be degraded by both intrinsic unavoidable causes, such as phonon scattering, and technology-dependent factors, such as contact resistance, heterointerface roughness, and other defects. As of now, the latter factors represent the main performance limitation, even if MoS_2 fabrication technology is improving at an impressive pace [11,12,24], whereas phonon scattering has a limited impact in the case with a 5-nm channel length.

IV. CONCLUSION

In this work, we present two different transistor concepts, based on planar heterostructures of $1T$-MoS_2 and $2H$-MoS_2, that exploit the possibility of defining with a top-down technique patterns of metallic $1T$-MoS_2 in a monolayer of semiconducting $2H$-MoS_2. We show with multiscale simulations that the lateral heterostructures, the FET and the planar barristor, exhibit promising performance with respect to the evolution of CMOS technology predicted by the 2015 edition of the ITRS, for both high-performance and low-power applications.

Clearly, our multiscale simulations consider defectless devices with ideal contacts and fully ballistic transport. Therefore, ours is a *via negativa* approach: It can rule out device concepts as good candidates for digital logic only if their (ideal) performance is not sufficiently good. In our case, it signals that the proposed transistor concepts are extremely promising. Further investigation is required to verify the impact of defects and nonidealities on performance.

ACKNOWLEDGMENTS

The authors gratefully acknowledge the support from the EC 7FP through the GRADE project (Agreement No. 317839) and the Graphene Flagship (Agreement No. 696656). The computational resources of nanoHUB are gratefully acknowledged.

APPENDIX: COMPUTATIONAL METHODS

DFT simulations are performed with the Quantum Espresso package [20]. For both materials, MoS_2-$2H$ and MoS_2-$1T$, we consider $8 \times 12 \times 1$ Monkhorst-Pack grid which is evaluated to be sufficiently accurate for the subsequent calculations. We use ultrasoft pseudopotentials with the PBE exchange-correlation functional. A 60-Ry wave-function cutoff, a 600-Ry charge-density cutoff and a vacuum layer of 20 Å are considered. The calculation of the MLWF is performed with Wannier90 [21] using the same grid as the DFT calculations. In Figs. 6(a) and 6(c), we show the bands for MoS_2-$2H$ and MoS_2-$1T$ while considering a varying number of Wannier centers (i.e., bands): 6, 10, and 22. It is evident that six bands provide the same results as the 22-band case (but with a smaller computational cost) if we consider an energy range close to the Fermi level, i.e., the energy range taking part in transport. We also report in Figs. 6(b) and 6(d) the density of states projected on the differing number of Wannier centers. As expected, the density of states of 6, 10, and 22 bands provides the very same results close to the Fermi level.

To validate the multiscale approach, we compare the computed transmission coefficient while considering a small number of bands with that obtained from *ab initio* calculations (by means of the PWCOND suite of Quantum Espresso [20]). We consider a LH FET with a 3.3-nm MoS_2-$2H$ channel, as studied in the main text. The total size of the system is 7.2 nm, the $1T$ parts are 1.9 and 1.3 nm, the $2H$ channel is 3.3 nm, while the remaining length corresponds to the interface between the two phases (see Ref. [14]). The three MLWF Hamiltonians fit the PWCOND result well, thus validating the use of the six-band Hamiltonian (see Fig. 7).

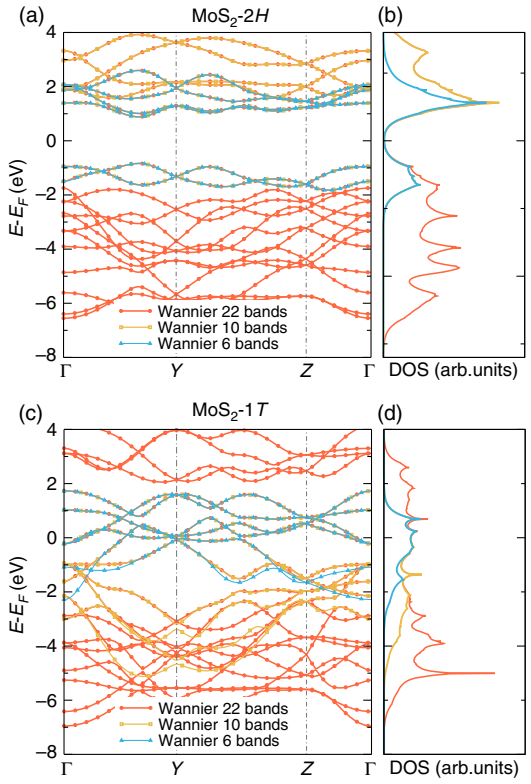

FIG. 6. Bands computed through MLWF for different numbers of Wannier centers (i.e., the number of considered bands) and the corresponding density of states (DOS) for (a),(b) MoS_2-$2H$ and (c),(d) MoS_2-$1T$.

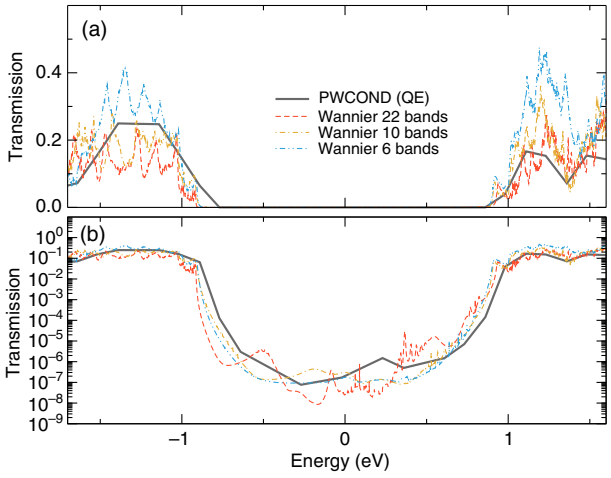

FIG. 7. Transmission coefficient of the LH-FET device in (a) the linear and (b) the semilogarithmic scale, considering a flat potential equal to zero. Comparison between PWCOND [Quantum Espresso (QE)] results and a Wannier Hamiltonian for a differing number of bands using the Wannier Hamiltonian of $2H$-MoS_2 as a coupling between the metallic and semiconducting phases.

In order to build the interface Hamiltonian between the two materials, one has to pay attention to the off-diagonal elements connecting the two different materials. The heterostructure Hamiltonian for the MoS_2-$1T$/MoS_2-$2H$ interface is determined as follows. In Fig. 8, we report a schematic representation of the Wannier Hamiltonian along the transport direction. Specifically, each submatrix in Fig. 8, whose dimension is $N_{\mathrm{Wan}} \times N_{\mathrm{Wan}}$ (where N_{Wan} is the number of Wannier centers), is connected to the other submatrices along the same row (the number of submatrices along the same row is constrained by the Monkhorst-Pack grid used). Then one has to choose how to deal with those elements which connect one material to the other (indicated in red in Fig. 8 as off-diagonal elements). These elements belong to a row where the first element is of the

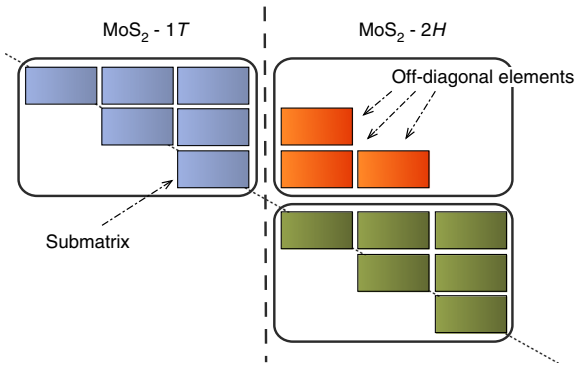

FIG. 8. Schematic representation of the construction of the MoS_2-$1T$/MoS_2-$2H$ interface. The off-diagonal elements, which are displayed in red, are chosen to be equal to the MoS_2-$2H$ elements.

first material (MoS_2-$1T$) and to a column of the second material (MoS_2-$2H$). We decide that these elements should be the same as the ones used with MoS_2-$2H$ for two reasons: First, the results of the transmission coefficient reported in Fig. 7 are in agreement with the PWCOND results, and, second, compared to the other possible choices, the simulations give a better and faster convergence.

[1] F. Capasso, Band-gap engineering: From physics and materials to new semiconductor devices, Science **235**, 172 (1987).

[2] E. Yablonovitch and E. O. Kane, Band structure engineering of semiconductor lasers for optical communications, J. Lightwave Technol. **6**, 1292 (1987).

[3] K. S. Novoselov and A. H. C. Neto, Two-dimensional crystals-based heterostructures: Materials with tailored properties, Phys. Scr. **T146**, 014006 (2012).

[4] A. K. Geim and I. V. Grigorieva, Van der Waals heterostructures, Nature (London) **499**, 419 (2013).

[5] L. Ci, L. Song, C. Jin, D. Jariwala, D. Wu, Y. Li, and P. M. Ajayan, Atomic layers of hybridized boron nitride and graphene domains, Nat. Mater. **9**, 430 (2010).

[6] M. P. Levendorf, C.-J. Kim, L. Brown, P. Y. Huang, R. W. Havener, D. A. Muller, and J. Park, Graphene and boron nitride lateral heterostructures for atomically thin circuitry, Nature (London) **488**, 627 (2012).

[7] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, Single-layer MoS_2 transistors, Nat. Nanotechnol. **6**, 147 (2011).

[8] H. Wang, L. Yu, Y. Lee, Y. Shi, A. Hsu, M. Chin, L. Li, M. Dubey, J. Kong, and T. Palacios, Integrated circuits based on bilayer MoS_2 transistors, Nano Lett. **12**, 4674 (2012).

[9] C.-H. Lee, G.-H. Lee, A. M. van der Zande, W. Chen, Y. Li, M. Han, X. Cui, G. Arefe, C. Nuckolls, T. F. Heinz, J. Guo, J. Hone, and P. Kim, Atomically thin *p-n* junctions with van der Waals heterointerfaces, Nat. Nanotechnol. **9**, 676 (2014).

[10] G. Eda, T. Fujita, H. Yamaguchi, D. Voiry, M. Chen, and M. Chhowalla, Coherent atomic and electronic heterostructures of single-layer MoS_2, ACS Nano **6**, 7311 (2012).

[11] R. Kappera, D. Voiry, S. E. Yalcin, B. Branch, G. Gupta, A. D. Mohite, and M. Chhowalla, Phase-engineered low-resistance contacts for ultrathin MoS_2 transistors, Nat. Mater. **13**, 1128 (2014).

[12] R. Kappera, D. Voiry, S. E. Yalcin, W. Jen, M. Acerce, S. Torrel, B. Branch, S. Lei, W. Chen, S. Najmaei, J. Lou, P. M. Ajayan, G. Gupta, A. D. Mohite, and M. Chhowalla, Metallic 1T phase source/drain electrodes for field effect transistors from chemical vapor deposited MoS_2, APL Mater. **2**, 092516 (2014).

[13] Y.-C. Y. Lin, D. O. Dumcenco, Y.-S. Huang, and K. Suenaga, Atomic mechanism of the semiconducting-to-metallic phase transition in single-layered MoS_2, Nat. Nanotechnol. **9**, 391 (2014).

[14] Y. Katagiri, T. Nakamura, A. Ishii, C. Ohata, M. Hasegawa, S. Katsumoto, T. Cusati, A. Fortunelli, G. Iannaccone, G. Fiori, S. Roche, and J. Haruyama, Gate-tunable atomically

thin lateral MoS_2 Schottky junction patterned by electron beam, Nano Lett. **16**, 3788 (2016).

[15] G. Iannaccone and G. Fiori, Field-effect transistor with two-dimensional channel realized with lateral heterostructures based on hybridized graphene, U.S. Patent No. 2014/0319467 A1 (30 October 2014).

[16] G. Fiori, A. Betti, S. Bruzzone, and G. Iannaccone, Lateral graphene-hBCN heterostructures as a platform for fully two-dimensional transistors, ACS Nano **6**, 2642 (2012).

[17] H. Yang, J. Heo, S. Park, H. J. Song, D. H. Seo, K.-E. Byun, P. Kim, I. Yoo, H.-J. Chung, and K. Kim, Graphene barristor, a triode device with a gate-controlled Schottky barrier, Science **336**, 1140 (2012).

[18] S. Bruzzone, G. Iannaccone, N. Marzari, and G. Fiori, An open-source multiscale framework for the simulation of nanoscale devices, IEEE Trans. Electron Devices **61**, 48 (2014).

[19] For NANOTCAD VIDES code and documentation, see http://vides.nanotcad.com.

[20] P. Giannozzi, S. Baroni, N. Bonini, M. Calandra, R. Car, C. Cavazzoni, D. Ceresoli, G. L. Chiarotti, M. Cococcioni, I. Dabo *et al.*, QUANTUM ESPRESSO: A modular and open source software project for quantum simulations of materials, J. Phys. Condens. Matter **21**, 395502 (2009).

[21] A. A. Mostofi, J. R. Yates, G. Pizzi, Y. S. Lee, I. Souza, D. Vanderbilt, and N. Marzari, An updated version of WANNIER90: A tool for obtaining maximally-localised Wannier functions, Comput. Phys. Commun. **185**, 2309 (2014).

[22] The International Technology Roadmap for Semiconductors 2.0, 2015 edition, is available at http://www.itrs2.net. We recalculate the τ and PDP values from the total gate capacitance ($C_{gate,total}$), the power supply voltage (V_{dd}) and the I_{on} current for the HP and LP cases since the quantities in the original table were computed for a FAN-OUT of 3.

[23] D. Logoteta, G. Fiori, and G. Iannaccone, Graphene-based lateral heterostructure transistors exhibit better intrinsic performance than graphene-based vertical transistors as post-CMOS devices, Sci. Rep. **4**, 1 (2014).

[24] A. Nourbakhsh, A. Zubair, R. N. Sajjad, A. Tavakkoli K. G., W. Chen, S. Fang, X. Ling, J. Kong, M. S. Dresselhaus, E. Kaxiras, K. K. Berggren, D. Antoniadis, and T. Palacios, MoS_2 field-effect transistor with sub-10 nm channel length, Nano Lett. **16**, 7798 (2016).