Nonlinear Contact Effects in Staggered Thin-Film Transistors

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The static and dynamic electrical characteristics of thin-film transistors (TFTs) are often limited by the parasitic contact resistances, especially for TFTs with a small channel length. For the smallest possible contact resistance, the staggered device architecture has a general advantage over the coplanar architecture of a larger injection area. Since the charge transport occurs over an extended area, it is inherently more difficult to develop an accurate analytical device model for staggered TFTs. Most analytical models for staggered TFTs, therefore, assume that the contact resistance is linear, even though this is commonly accepted not to be the case. Here, we introduce a semiphenomenological approach to accurately fit experimental data based on a highly discretized equivalent network circuit explicitly taking into account the inherent nonlinearity of the contact resistance. The model allows us to investigate the influence of nonlinear contact resistances on the static and dynamic performance of staggered TFTs for different contact layouts with a relatively short computation time. The precise extraction of device parameters enables us to calculate the transistor behavior as well as the potential for optimization in real circuits.

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I. INTRODUCTION

Thin-film transistors (TFTs) provide a technological platform for large-area electronics applications, including active-matrix displays, sensors, and logic circuits. TFTs can be fabricated with numerous semiconductors, such as polycrystalline silicon (poly-Si), hydrogenated amorphous silicon (*a*-Si:H), metal chalcogenides, metal oxides, conjugated polymers, and small molecules, and using a wide range of processing techniques, such as physical and chemical vapor deposition, solution processing, inkjet printing, and gravure printing, to name just a few [1–3]. A common trend in TFTs is the miniaturization of the device dimensions, especially of the channel length, with the goal of reducing the carrier transit time and the device capacitance to achieve a higher operation frequency. Indeed, for channel lengths around or below 1 μm, operating frequencies as high as 5 GHz have been reported for poly-Si TFTs, 1 MHz for *a*-Si:H TFTs, 135 MHz for metal-oxide TFTs, 20 MHz for polymer TFTs, and 27.7 MHz for small-molecule TFTs [4–9]. With decreasing channel lengths, the contribution of the channel resistance to the total device resistance decreases and the parasitic contact resistances begin to influence the device behavior. As a result, the current-voltage characteristics of short-channel TFTs are often dominated by the contact properties [10–12]. This situation is particularly pronounced whenever a systematic reduction of the contact resistance by chemical doping of the contact regions is not possible or not practical, which is typically the case in metal-oxide and organic TFTs [13]. As a consequence, the effective (or apparent) carrier mobility extracted from the current-voltage characteristics of short-channel TFTs is often substantially smaller than the carrier mobility in the charge accumulation zone of the semiconductor layer [12]. A large, gate-bias-dependent contact resistance can also lead to an erroneous extraction of an overestimated charge-carrier mobility from the transfer curves of the TFTs [14–16].

When considering the contact resistance and its influence on the current-voltage behavior of the devices, it is necessary to distinguish between the coplanar architecture, in which the gate dielectric and the source and drain contacts are located on the same interface with the semiconductor layer [see Fig. 1(a)], and the staggered architecture, in which the gate dielectric is located on one interface and the source and drain contacts are facing the opposite interface with the semiconductor [see Fig. 1(b)] [17]. For coplanar TFTs, the parasitic contact resistances can be easily incorporated into analytical device models, as they appear mainly at the edges of the contacts close to the channel region [18–22]. By contrast, the charge injection and extraction in staggered TFTs occur across a certain area along the contact-semiconductor interface [23,24] that is characterized by the transfer length L_T [see Fig. 1(b)] [25–27]. Several models have been proposed for staggered

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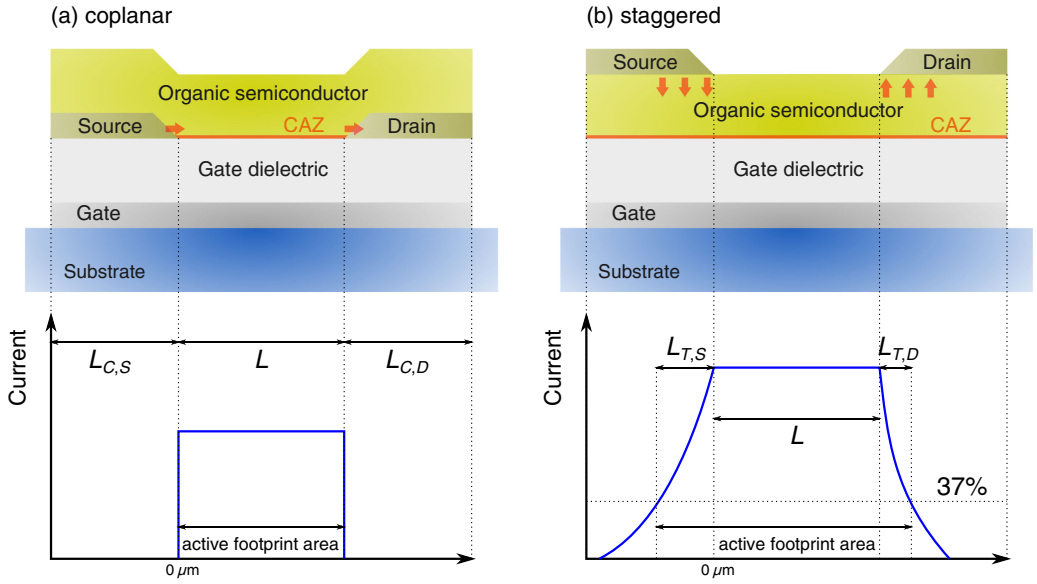

FIG. 1. Comparison of field-effect transistors in (a) the coplanar and (b) the staggered architecture regarding charge injection, transfer length, and active-footprint-area current. The charge accumulation zone (CAZ) located in the semiconductor near the interface to the gate dielectric is shown in orange. L is the channel length. L_C is the contact length, and L_T is the transfer length of the source (S) and the drain (D), respectively.

TFTs in order to describe how the device characteristics are affected when charges are exchanged between the contacts and the semiconductor across a laterally extended area [28–30]. Provided that the contact resistance is approximately linear, reasonable assumptions can indeed be derived, and reasonably accurate models can thus be developed [31].

However, in the absence of contact doping, both the field dependence of the charge injection and the charge transport in the bulk semiconductor (described, for example, by a space-charge-limited current) are generally nonlinear [29,32,33], which means that most of the assumptions required in the derivation of the abovementioned models are only partially valid. As a result, a suitable tool to accurately describe the time-resolved influence of a nonlinear contact resistance on the current-voltage characteristics of the TFTs depending on the contact geometry is still lacking.

One approach to treating this problem is the utilization of numerical drift-diffusion simulations, which are useful for studying the charge flow in three dimensions but require a detailed knowledge of the materials and the interface properties [34–41]. The latter makes it difficult, if not impossible, to adapt the results of such simulations. The reason for this is that the properties of the interfaces between the contacts and the semiconductor, especially in the case of organic semiconductors, critically depend not only on the choice of material but also on a large number of process parameters [42,43]. As an alternative, various analytical models have been developed for treating the injection of charges into organic semiconductors [44–48], but these models are unable to predict the charge flow at the metal-semiconductor interfaces *a priori*. Parameters such as the energy barrier height partially lose their physical meaning and are instead used to adjust resistances to the correct levels during the fitting of experimental data, which means that they become or behave like phenomenological parameters. Besides, charge-injection models do not always reproduce the exact fundamental current-voltage characteristics of metal-semiconductor interfaces, hence making comparisons between modeling results and experimental data impossible for any TFT structure.

To overcome these fundamental limitations of existing modeling and simulation approaches, we introduce a strategy that is based on a circuit simulator in which an equivalent network of multiple ideal transistors, in combination with linear and nonlinear resistors as well as capacitors, is used to accurately model a single transistor device that specifically includes nonlinear contact resistances. This alternative approach makes it possible to use a semiphenomenological description of charge injection into and charge transport inside the contact regions of the device, which perfectly suits the problem and thus minimizes the modeling and computation effort. In combination with laterally resolved contact and channel regions, the interplay between device geometry and device performance can be investigated in great detail, and the critical effect of nonlinear contact resistances becomes apparent. In addition, the short computation time makes it possible to rapidly fit experimental data and thus extract physical parameters, such as the intrinsic charge-carrier mobility as well as the threshold voltage, even for very small channel lengths, which are typically restricted by a parasitic contact resistance.

II. RESULTS

A. Modeling approach

As shown in Fig. 2(a), a single transistor is described by an equivalent network circuit based on a current-crowding model [29,31,49]. This equivalent network circuit is solved using the freely available circuit simulator LTspice [50] (see Fig. S1 of the Supplemental Material [51]). We divide the TFT into three distinct lateral regions: source, channel, and

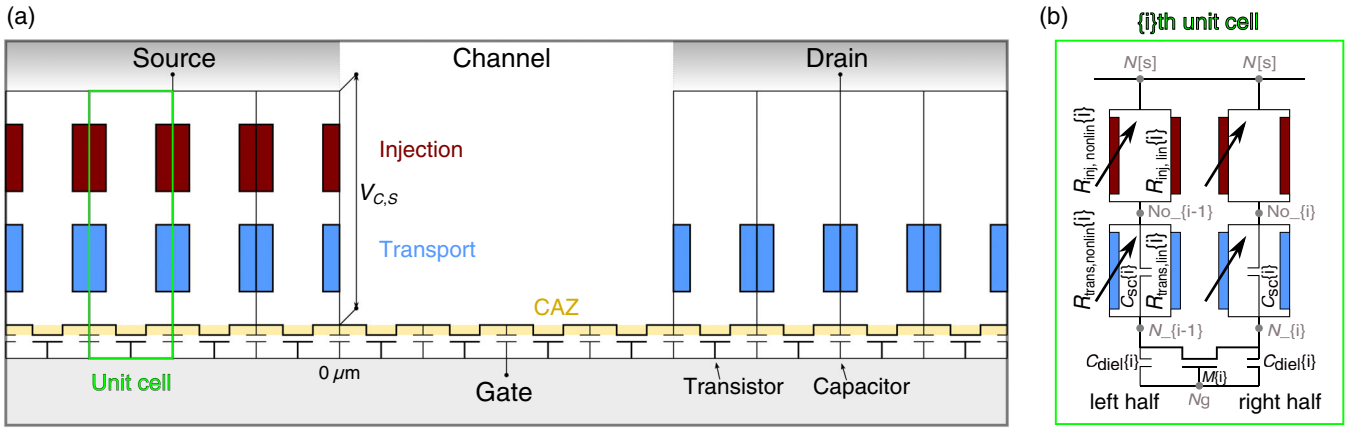

FIG. 2. (a) Equivalent circuit employed for the network simulation. A one-dimensional line of ideal transistors represents the charge accumulation zone (CAZ) that extends from the source region (left) across the channel region (middle) to the drain region (right). The contacts are connected to the CAZ by linear (lin) and nonlinear (nonlin) resistors representing charge injection [red (inj)] and charge transport [blue (trans)]. (b) To allow symmetric discretization for $L = 0$ μm, the boundaries of each unit cell, shown here for the source region, divide the resistors in half. Capacitances parallel to each transistor and parallel to the transport resistors represent the gate-dielectric (C_{diel}) and the semiconductor layer (C_{sc}), respectively.

drain. In each of these regions, charges can accumulate in the semiconductor at the gate-dielectric interface within the charge accumulation zone (CAZ). Please note the difference between the CAZ and the channel. Here, the channel is the region between the source and the drain related to the channel length of the transistor. By contrast, the CAZ is the highly conducting zone close to the gate dielectric that extends laterally into all regions: the source region, the drain region, and the channel region, which are depicted in Fig. 2(a).

In accordance with the principal idea of the gradual channel approximation, the CAZ is modeled as a series of ideal transistors. For that reason, we use the NMOS model of LTspice employing the Shichman-Hodges model for silicon MOSFETs (see Fig. S2 of the Supplemental Material [51]) [52]. All individual transistors of the CAZ are identical, sharing the same parameters: the CAZ mobility μ_{CAZ}, the threshold voltage V_{th}, the channel width W, and the length of the respective unit cell. Thus, the series connection of unit-cell transistors forming the channel region behaves like a single transistor having the channel length L. Because it is implemented as a series of individual transistors, the electrostatic potential distribution along the channel can be resolved provided that the charge transport is dominated by drift, which is the case in all regimes of transistor operation except the subthreshold regime. The resolution is given by the discretization length L_{disc}, which is set to 10 nm for all simulations shown here, although a larger discretization length (e.g., $L_{\mathrm{disc}} = 100$ nm) is found to also produce satisfactory results in many cases (see Fig. S6 of the Supplemental Material for details [51]).

The coupling of the CAZ to the source and drain contacts is realized by a network of resistors representing charge injection [indicated in red and abbreviated as "inj" in Fig. 2(b)] and charge transport [indicated in blue and abbreviated as "trans" in Fig. 2(b)] [53]. Here, we assume that charge injection occurs only from the source contact, not from the drain contact. Charge transport is modeled according to the Mott-Gurney law describing a space-charge-limited current [see Eq. (3)], with the most important parameter being the bulk mobility μ_{bulk} of the semiconductor [32].

Charge injection is usually described using exponential equations [54]. However, the computational effort required to solve exponential equations is substantially greater than for power-law equations. For certain material systems, the current-voltage relation for charge injection can, in fact, be described using a power law [55] and, more generally, a power law can always be employed to simulate curve trends over a certain value range. We therefore use a power law for charge injection, as given by Eq. (1), to phenomenologically adjust the model to the experimental data using two independent parameters: j_0 and α ($V_0 \equiv 1$ V).

These nonlinear contributions [visualized in Fig. 2(b) as variable resistors and abbreviated as "nonlin"] are both power laws with an exponent greater than 1, so that the differential resistance at 0 V tends towards infinity, making it impossible to find the trivial solution for $I = 0$ A. To account for this issue, linear resistors [abbreviated as "lin" in Fig. 2(b)] are introduced in parallel with the nonlinear elements, for both charge injection (red) and charge transport (blue). The introduction of these linear resistors can be rationalized by the fact that metal-insulator-metal devices with efficient charge injection are always characterized by a linear background conductivity resulting from the charge density remaining in the device at zero bias [56] and by the fact that a Taylor expansion of the equations used to describe the charge injection will typically include a linear component. In summary, the linear and nonlinear contributions to

the contact resistance can be seen as the Ohmic and the non-Ohmic part of a resistor, respectively.

All equations pertaining to a single unit cell are summarized by Eq. (1)–(4), corresponding to the linear resistors ($R_{\mathrm{inj,lin}}$, $R_{\mathrm{trans,lin}}$) and the nonlinear resistors ($R_{\mathrm{inj,nonlin}}$, $R_{\mathrm{trans,nonlin}}$) in Fig. 2(b). Note that, in order to permit symmetric discretization for $L = 0$ μm, the resistors are divided in half at the boundaries of each unit cell.

In addition to the static TFT characteristics, circuit simulators like LTspice can also be used to calculate the dynamic device properties. We therefore include capacitors (C_{diel}) in the equivalent circuit network which account for the capacitance of the gate dielectric in the channel region [see Fig. 2(b)]. Likewise, we also include additional capacitors in parallel to the vertical-charge-transport resistors to account for the capacitance of the semiconductor layer, corresponding to their area-normalized geometric capacitance $C_{\mathrm{sc}} = \epsilon_{\mathrm{sc}}\epsilon_0 t_{\mathrm{sc}}^{-1}$. Through simulations, we find that, for the TFTs considered here, the effect of the latter capacitors on the dynamic behavior is insignificant, mainly because the capacitance of the semiconductor layer is substantially smaller than the gate-dielectric capacitance, and because the conductivity of the semiconductor layer is sufficiently large so that it has a mainly resistive character. For other TFT geometries, the influence of the capacitance of the semiconductor layer may be more pronounced. Together with the resistive elements (arbitrary current sources representing charge injection and transport, ideal transistors representing the CAZ), the capacitors form a complex RC network that is efficiently and accurately solved by the circuit simulator. For a detailed implementation, please see the source code in the Supplemental Material [51]:

$$I_{\mathrm{inj,nonlin}}(V) = j_0\left(\frac{V}{V_0}\right)^{\alpha}\frac{A_{\mathrm{unit}}}{2}, \tag{1}$$

$$I_{\mathrm{inj,lin}}(V) = \frac{V}{\rho_{\mathrm{inj}}}\frac{A_{\mathrm{unit}}}{2}, \tag{2}$$

$$I_{\mathrm{trans,nonlin}}(V) = \frac{9}{8}\epsilon_{\mathrm{sc}}\epsilon_0\mu_{\mathrm{bulk}}\frac{V^2}{t_{\mathrm{sc}}^3}\frac{A_{\mathrm{unit}}}{2}, \tag{3}$$

$$I_{\mathrm{trans,lin}}(V) = \frac{V}{\rho_{\mathrm{trans}}}\frac{A_{\mathrm{unit}}}{2}. \tag{4}$$

B. Fitting experimental data

The proposed model is utilized to characterize experimental data from TFTs fabricated in the inverted staggered (bottom-gate, top-contact) architecture using the small-molecule organic semiconductor pentacene as active material [57], although the results are applicable to staggered TFTs based on other material systems as well. The experimental data used to verify the model were published previously by Kraft *et al.* [12]. The parameters taken from the experiment are the gate-to-source overlap $L_{C,S}$ (200 μm), the gate-to-drain overlap $L_{C,D}$ (200 μm), the channel width W (200 μm), the thickness of the semiconductor layer t_{sc} (25 nm), and the unit-area capacitance of the gate dielectric C_{diel} (700 nF/cm^2).

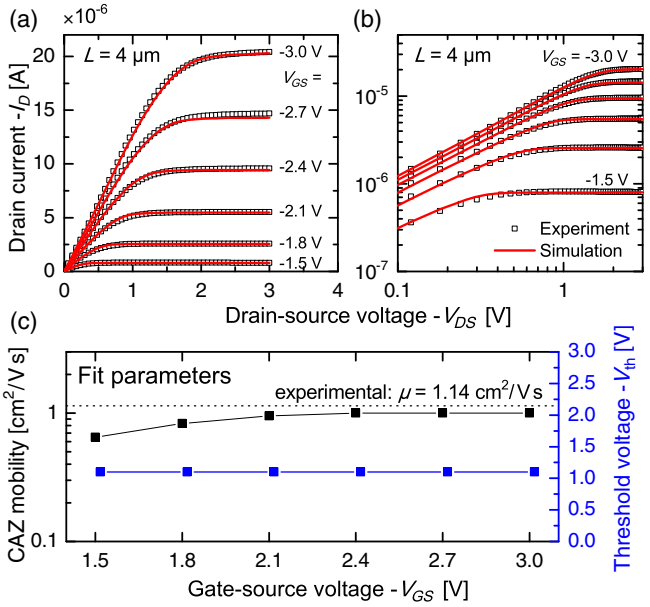

FIG. 3. (a),(b) Simulated and measured output characteristics of a pentacene TFT with a channel length of $L = 4$ μm, plotted using linear and logarithmic scales. In the simulations, all parameters except for the gate-source voltage and the CAZ mobility are kept constant. Excellent agreement between model and experiment is achieved both in the linear and the saturation regimes. (c) Dependence of the fit-parameter CAZ mobility on the gate-source voltage. The dashed line indicates the effective mobility measured for a TFT with a channel length of 100 μm, where the influence of the contact resistance on the current-voltage characteristics—and hence the difference between the effective mobility and the CAZ mobility—is very small. The threshold voltage is kept constant during the simulations.

We begin by modeling the measured data of the TFT with the longest channel length ($L = 100$ μm) in order to extract a first guess of basic parameters. For this purpose, the TFT with the longest channel length is most suitable, due to the fact that the influence of the contact resistance is smallest in this TFT. The CAZ mobility (μ_{CAZ}) and the threshold voltage (V_{th}) obtained from the simulation of this long-channel TFT are then used to investigate a TFT with a channel length of 4 μm by including the contact resistance in the simulation; see Fig. 3. In the first step, the linear contributions to the contact resistance are adjusted in order to achieve the best possible agreement between simulated and measured output characteristics (drain current vs drain-source voltage) for very small drain-source voltages, i.e., in the linear regime of operation. However, this procedure leads to a deviation between model and experiment in the steepness of the curve for absolute drain-source voltages above 0.4 V and in the level of the saturation regime (see Fig. S3 of

the Supplemental Material [51]). We observe that the slope of the curve slightly increases for curves measured with a large overdrive voltage $|V_{GS} - V_{\mathrm{th}}|$, i.e., for gate-source voltages between about −2 and −3 V. Such a behavior leads to an overshoot in differential output conductance, as reported by Liu *et al.* [47]. By contrast, a simulation with purely linear contact resistances produces a continuous decrease of the slope of the output curves towards the saturation regime, consistent with the gradual channel approximation. In order to accurately capture the experimentally observed slight increase of the differential output conductance in the linear operation regime in Fig. 3(a), both the linear and nonlinear contributions to the contact resistance are required in the model, as shown in Fig. 2(b).

This finding raises the question of whether the effects of charge injection and charge transport on the contact resistance can be clearly distinguished. To answer this question, it is necessary to decouple the contributions of charge injection and charge transport. An important difference between charge injection and charge transport is that charge injection occurs only in the source region, whereas charge transport occurs in both the source region and the drain region. Since the electric-potential drop across the source contact part, i.e., the source-sided contact voltage $V_{C,S} = I_D R_{C,S}$ [see Fig. 2(a)], consumes not only part of the applied drain-source voltage but also part of the applied gate-source voltage, the effective overdrive voltage ($|V_{GS} - V_{\mathrm{th}} - V_{C,S}|$) present in the channel is smaller than the difference between the applied gate-source voltage and the threshold voltage (cf. Ref. [39]). This effect implies that the density of charge carriers accumulated in the channel by the applied gate field is smaller than it would be in the absence of a source-sided contact resistance $R_{C,S}$. As a consequence, a source-sided contact resistance causes a reduction of the drain current in the saturation regime, while a drain-sided contact resistance only decreases the drain current in the linear regime (see Fig. S4 of the Supplemental Material [51]). Additionally, a resistance at the drain has been found to smoothen the transition between both regimes, which is required to fit the experimental data correctly (see Fig. S5 of the Supplemental Material [51]). With this knowledge in mind, we are able to adjust the nonlinear contribution of the source-sided contact resistance and the nonlinear contribution of the drain resistances independently in order to achieve the best possible agreement between model and experiment in both the linear and the saturation regime. Please find further explanations of the fitting procedure in the Supplemental Material [51].

All simulation parameters are summarized in Table I as a standard parameter set. The geometry is taken from Ref. [12] and the relative permittivity of pentacene is assumed to be 4, in accordance with the literature [58–61]. For all simulated and fitted curves in this work, the contact resistance according to Eqs. (1)–(4) is always described by the following five constant parameters: The current density j_0 and the exponent α modulate the power law used for the charge injection, whereas the bulk mobility (in the vertical direction) μ_{bulk} is used to adjust the conductivity of the space-charge-limited current describing the charge transport. The area-independent resistances ρ_{inj} and ρ_{trans} specify the linear contribution of charge injection and transport, respectively.

TABLE I. Summary of the standard parameter set for the modeling of the experimental data. The gate dielectric capacitance, the thickness of the semiconductor layer, the channel width, and the gate-to-contact overlaps are taken from Ref. [12]. The relative permittivity of pentacene is taken from the literature [58–61]. L_{disc} and A_{unit} are the discretization length and the unit-cell area ($L_{\mathrm{disc}} W$). The five parameters for the contact resistance are obtained through the initial fitting process and are constant for all experimental variations, and they are then kept constant for all subsequent simulations. The transistor parameters μ_{CAZ} and V_{th} represent the best fit found in Fig. 3 for $V_{GS} = -3$ V, and in Fig. 4 for $L = 4$ μm, and are then used in all subsequent simulations.

Given values	
ϵ_{sc}	4.0
t_{sc}	25 nm
$L_{C,S}$, $L_{C,D}$	200 μm
W	200 μm
C_{diel}	700 nF/cm^2
L_{disc}	10 nm
A_{unit}	2 μm^2
Contact resistance	
j_0	3.9 A/cm^2
α	3.0
ρ_{inj}	1.75 Ω cm^2
μ_{bulk}	6×10^{-3} cm^2/V s
ρ_{trans}	0.0272 Ω cm^2
Transistor parameters	
μ_{CAZ}	1.0 cm^2/V s
V_{th}	−1.1 V

After determining the contact resistance from the output curve measured at the largest gate-source voltage (where the influence of the contact resistance on the overall device resistance is greatest), all remaining output curves are fitted. During this process, the contact resistance and the threshold voltage are kept constant (i.e., independent of the gate-source voltage), while the CAZ mobility is adjusted for each gate-source voltage in order to achieve the best possible agreement between model and experiment. As can be seen in Fig. 3(c), the mobility in the semiconductor channel increases with increasing gate-source voltage, from 0.65 cm^2/V s at a gate-source voltage of −1.5 V to 1.0 cm^2/V s at a gate-source voltage of −2.4 V. Assuming that the carrier density in the CAZ is proportional to the overdrive voltage $|V_{GS} - V_{\mathrm{th}}|$, this observation reflects the dependence of the mobility on the carrier density that is typically observed in organic semiconductors [62,63]. For

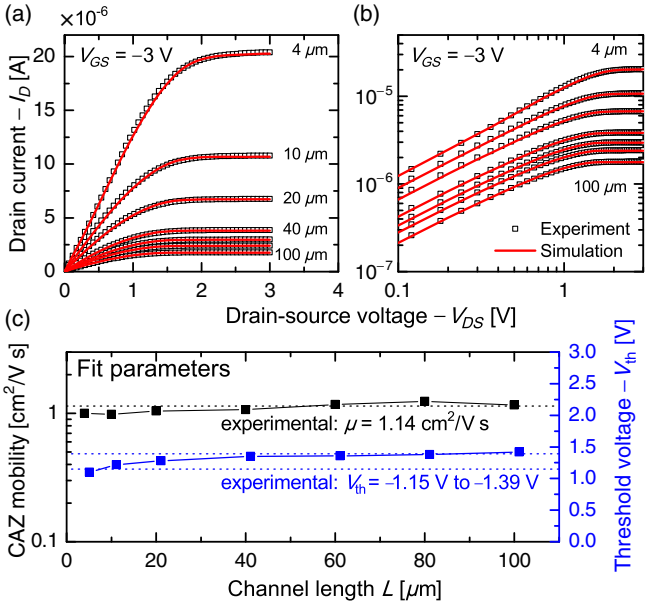

FIG. 4. (a),(b) Simulated and measured output characteristics of pentacene TFTs with channel lengths ranging from 4 to 100 μm at a gate-source voltage of −3 V, plotted using linear and logarithmic scales. In the simulations, all contact-resistance parameters are kept constant, while the CAZ mobility and the threshold voltage are adjusted for each channel length. (c) Dependence of the fit parameters' CAZ mobility and threshold voltage on the channel length. The black dashed line indicates the effective mobility measured for a TFT with a channel length of 100 μm. The blue dashed lines indicate the smallest and largest experimentally determined threshold voltages.

gate-source voltages beyond −2.4 V, Fig. 3(c) indicates that the CAZ mobility saturates (in this case, at a value of 1.0 $\mathrm{cm}^2/\mathrm{V\,s}$). This finding is in agreement with predictions derived from studies of the Gaussian disorder model which show that the charge-carrier mobility saturates when about 5% of the molecules in the channel carry an induced charge [64]. At a gate-source voltage of −2.4 V, the charge-carrier density in the channel of our TFTs is about 5×10^{19} cm^{-3} [$n = C_{\mathrm{diel}}(V_{GS} - V_{\mathrm{th}})/t_{\mathrm{channel}}$, with $C_{\mathrm{diel}} = 700$ nF/cm^2, $V_{\mathrm{th}} = -1.1$ V, and $t_{\mathrm{channel}} \approx 1$ nm], which corresponds to about 5% of the pentacene molecules. Owing to the fact that a variety of critical device and material parameters can be analyzed in detail once the behavior of the contact resistance is known, the semiphenomenological modeling approach presented here is ideally suited to reveal even minor parameter changes.

Figure 4(a) shows the output characteristics of TFTs with channel lengths ranging from 4 to 100 μm, all measured at a gate-source voltage of −3 V. Having determined the contact resistance from the TFT with the smallest fabricated channel length (where the influence of the contact resistance on the current-voltage characteristics is most pronounced), the contact resistance is kept constant when simulating TFTs with all other channel lengths according to Table I. When fitting these experimental data, only the CAZ mobility and the threshold voltage are adjusted, as shown in Fig. 4(b).

The CAZ mobility μ_{CAZ} obtained from the simulations is essentially independent of the channel length and close to the mobility determined experimentally for the TFT with the largest channel length of 100 μm (cf. Ref. [12]). This is the expected result since the mobility of the charge carriers in the semiconductor channel is obviously independent of the channel length as long as individual crystallites of the organic semiconductor are much smaller than the channel length [65]. It is, however, in stark contrast to the effective mobility extracted from the transfer characteristics of the TFTs, which shows a pronounced decrease with decreasing channel length (cf. Ref. [12]) due to the influence of the contact resistance.

As can be seen in Fig. 4(c), the CAZ mobility varies by less than 10% from device to device, which makes it possible to obtain additional insight into the behavior of the TFT. For example, the absolute value of the threshold voltage monotonically decreases with decreasing channel length, and this decrease is most pronounced for the smallest channel lengths. This is known as threshold-voltage roll-off and is commonly observed in inorganic [66–69] as well as organic field-effect transistors [70]. With our alternative simulation approach, we are able to show that the threshold-voltage roll-off also occurs in low-voltage TFTs, where detection tends to be difficult. Besides, we can rule out that it is caused by contact effects, as they are explicitly included in the model.

The good agreement between the simulation results and the experimental data illustrates how well this semiphenomenological approach is able to describe the behavior of thin-film transistors. Among the five parameters used in the model, three are directly related to physical properties: μ_{bulk} represents the carrier mobility in the bulk of the semiconductor, and ρ_{inj} and ρ_{trans} represent fundamental characteristics of the contact resistance. Therefore, only two of the fit parameters (j_0 and α) are somewhat arbitrary, but they are directly related to a physical process, and they are essential to providing an accurate, yet computation-efficient, approximation of the current-voltage relationship by a power law (see Fig. S6 of the Supplemental Material [51]). Often, the exact formula is not known or must be fitted to the experimental data anyway, so the semiphenomenological approach is also most target oriented when it comes to predicting the properties of a particular transistor design or material system. Therefore, the semiphenomenological approach makes it possible to easily adapt the model to any other material system, as it requires no specific assumptions regarding the material properties.

C. Visualization of the contact resistance

To visualize the fitted contact resistance, related to the experimental data, and its various dependencies in more detail, we perform a number of additional simulations and

calculations based on the TFT architecture presented in Ref. [12] and using the parameters given in Table I. The results of these simulations and calculations are presented in this section.

Both the linear and the nonlinear components of the current under the source contact are plotted by inserting the parameters from Table I into Eqs. (1) and (2) for freely chosen voltages. We calculate the current density resulting from the injection of the charges from the source contact into the semiconductor, each as a function of the (vertical) potential drop V_{vert} across the circuit elements that are indicated in red in Fig. 2(b). Since the linear and the nonlinear subelements of the contact resistance are connected in parallel, we calculate the sum of both contributions, giving the total current density j_{inj} resulting from the charge-injection process, and plot it as a function of the potential drop; this is the red curve in Fig. 5(a). Likewise, we calculate the linear and nonlinear components of the charge-transport current density by applying Eqs. (3) and (4) and plot the sum (j_{trans}) as a function of the potential drop across the circuit elements indicated in blue in Fig. 2(b); this is the blue curve in Fig. 5(a). Since charge injection and charge transport occur in series, the total current density is calculated as

$$j_{\mathrm{tot}}(V_{\mathrm{vert}}) = \frac{1}{\frac{1}{j_{\mathrm{inj}}(V_{\mathrm{vert}})} + \frac{1}{j_{\mathrm{trans}}(V_{\mathrm{vert}})}} \tag{5}$$

and plotted as a function of the total voltage drop (i.e., the sum of the two individual voltage drops); this is the black curve in Fig. 5(a). The total vertical voltage is the sum of the vertical voltages needed for charge injection as well as charge transport. It can be understood as the potential drop between the source contact and the CAZ. Furthermore, we define the contact voltage $V_{C,S}$, which is the potential drop between the source contact and the start of the channel region, as indicated in Fig. 2. The total vertical voltage can locally differ within the source region and equals the contact voltage at the start of the channel region.

Given that the fitted bulk mobility (i.e., the carrier mobility in the vertical direction) is so small (6×10^{-3} cm^2/V s; see Table I), one might expect that the contact resistance would be dominated by the resistance associated with the transport of the injected charges through the thickness of the semiconductor layer to the charge accumulation zone. However, Fig. 5(a) shows that, for all voltages up to about 30 V, the contact resistance is instead dominated by the voltage drop associated with the injection of the charges into the semiconductor; only for voltages greater than about 30 V is the contact resistance dominated by the resistance associated with the charge transport through the bulk of the semiconductor. Still, the contribution of the charge transport to the contact resistance is not negligible even at small voltages, as it leads to a smoother transition between the linear regime and the

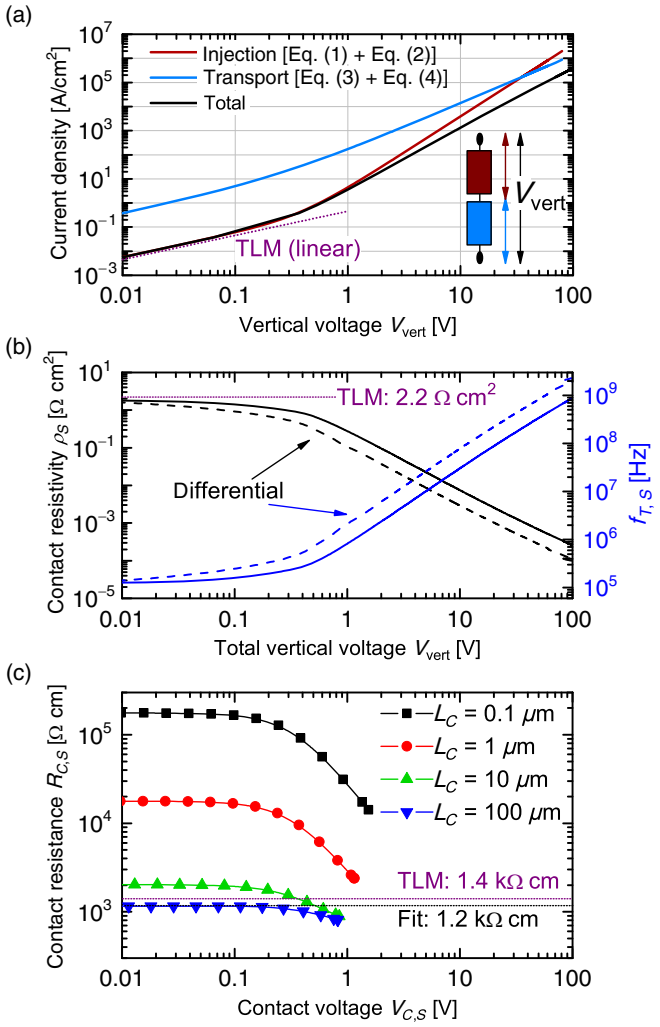

FIG. 5. Visualization of the modeled contact resistance. (a) Current densities due to charge injection (red) and charge transport (blue) at the source contact, calculated using the parameters summarized in Table I, including the linear and nonlinear components, and plotted versus the corresponding vertical voltage (see the inset). The black curve is the total current density, calculated using Eq. (5) and plotted as a function of the sum of the vertical voltages for charge injection and charge transport. (b) From the total current density, the contact resistivity (i.e., the area-normalized resistance) of each unit cell under the source contact is calculated, and both its absolute value ρ_S [the solid black line; calculated using Eq. (6)] and its differential value $\rho_{S,\mathrm{diff}}$ [the dashed black line; calculated using Eq. (7)] are plotted as a function of the total vertical voltage. From the source-sided contact resistivity and the unit-area gate-dielectric capacitance C_{diel}, the transit frequency $f_{T,S}$, as limited by the source contact, can be estimated using Eqs. (8) (the solid blue line) and (9) (the dashed blue line). (c) The simulated resulting source-sided contact resistance (normalized to the channel width W) finally depends on the voltage between the source contact and the beginning of the channel region (the source-sided contact voltage $V_{C,S}$), which depends on the applied drain-source voltage V_{DS}, varying from 0 to −3 V, and the gate-source voltage—here, −3 V.

saturation regime in the output characteristics (see Fig. S5 of the Supplemental Material [51]). Figure 5(a) also shows that the contact resistance is linear for very small voltages but nonlinear for voltages greater than about 1 V, which is consistent with results obtained previously on metal–intrinsic-semiconductor–metal devices and on doped-semiconductor–intrinsic-semiconductor–doped-semiconductor devices [56,71,72].

The fact that the charge-transport curve [the blue curve in Fig. 5(a)] is linear at small voltages is attributed to the residual background conductivity in the intrinsic region of the semiconductor, resulting from the diffusion of charges from the source contact (or from a doped semiconductor region near the contact interface) into the intrinsic semiconductor layer. The fact that the charge-injection curve [the red curve in Fig. 5(a)] is linear at small voltages is attributed to the injection laws, which are generally linear at small voltages, according to a Taylor expansion, e.g., due to a residual number of charge carriers that remain at the metal-semiconductor interface. These linear contributions to the contact resistance are a prerequisite for being able to treat field-effect transistors in a first-order approximation by a linear contact resistance. This assumption is used in the transmission-line method (TLM) to estimate the contact resistance by extrapolating the device resistance for zero channel length [25,26]. Hence, our approach reproduces the result of the TLM in the linear region of the contact resistance (see Fig. 5) as done by Kraft *et al.* using $V_{DS} = -0.1$ V, $V_{GS} - V_{\mathrm{th}} = -1.5$ V) [12].

Dividing the total vertical voltage by the total current density yields the (area-independent) contact resistivity at the source:

$$\rho_S = \frac{V_{\mathrm{vert}}}{j_{\mathrm{tot}}}, \tag{6}$$

which can also be calculated as a differential value:

$$\rho_{S,\mathrm{diff}} = \frac{dV_{\mathrm{vert}}}{dj_{\mathrm{tot}}}. \tag{7}$$

In Fig. 5(b), both the absolute value and the differential value of the source-contact resistivity (ρ_S and $\rho_{S,\mathrm{diff}}$) are plotted as a function of the total vertical voltage. The product of the contact resistivity and the unit-area gate-dielectric capacitance C_{diel} (700 nF/cm^2) is a time constant that describes how rapidly the gate-source capacitance is charged and discharged when the applied gate-source voltage is changed, and since the transistor cannot switch faster than given by this time constant, we can calculate an upper limit for the transit frequency of the transistor:

$$f_{T,S} = \frac{1}{2\pi\rho_S C_{\mathrm{diel}}}, \tag{8}$$

$$f_{T,S,\mathrm{diff}} = \frac{1}{2\pi\rho_{S,\mathrm{diff}} C_{\mathrm{diel}}}. \tag{9}$$

Figure 5(b) shows that the transit frequency is smaller than 1 MHz as long as the transistor operates in the regime in which the contact voltage is small, i.e., in which the contact resistance is linear. This result is valid independent of the contact length. Only when the contact voltage exceeds about 0.5 V, the nonlinear contributions to the charge injection and transport cause a notable decrease of the contact resistance, resulting in an increase of the maximum possible transit frequency beyond 1 MHz.

In Fig. 5(b), we plot both the absolute value of the contact resistivity [see Eq. (6)] and the differential value of the contact resistivity [see Eq. (7)], as well as the transient frequencies calculated from these absolute and differential values of the contact resistivity [see Eqs. (8) and (7)] as a function of the total vertical voltage. In the linear regime (where the vertical voltage is smaller than 0.5 V), the deviation between the two values calculated for the transient frequency is insignificant, but in the nonlinear regime (where the vertical voltage is greater than 0.5 V), the transient frequency calculated from the differential value of the contact resistivity is greater by a factor of about 3 than the transient frequency calculated from the absolute value of the contact resistivity. Considering that the transit frequency relates to the transistors' small-signal behavior, it is the differential—rather than the absolute value of the contact resistivity, and hence the transit frequency calculated from that differential contact resistivity—that is relevant here. Figure 5(b) thus illustrates that the nonlinear contributions to the contact resistance allow the transistor to operate at higher frequencies than would be possible if the contact resistance were strictly linear, due to the decrease of the differential contact resistance at larger vertical voltages.

In Fig. 5(c), the source-sided contact resistance $R_{C,S}$, calculated using Eq. (10), is plotted as a function of the contact voltage $V_{C,S}$ for simulations using four different contact lengths (100, 10, 1, and 0.1 μm), which illustrates how the contact resistance of staggered thin-film transistors is affected by the area available for the injection and transport of the charges. Since the contact voltage depends only on the total current flow at a certain gate-source voltage, the current-voltage characteristics of the source contact $I = I(V_{C,S}, V_{G,S})$ are independent of the channel length and are simulated here for a channel length of 4 μm, a gate-source voltage of -3 V, and drain-source voltages ranging from close to 0 to -3 V. As can be seen, for these applied voltages, the source-sided contact voltage $V_{C,S}$ varies from close to 0 to about 2 V:

$$R_{C,S} = \frac{V_{C,S}}{I_D}. \tag{10}$$

Like the contact resistivity plotted in Fig. 5(b), the source resistance in Fig. 5(c) is linear (i.e., independent of the contact voltage) for contact voltages up to about 0.2 V, but nonlinear (and monotonically decreasing) when the contact

voltage increases beyond about 0.2 V. Reducing the contact length from 100 to 10 μm leads to an increase in source resistance by a factor of only about 2, whereas reducing the contact length from 10 to 1 μm or from 1 to 0.1 μm leads to an increase in source resistance by as much as 1 order of magnitude. The source resistance calculated here for a contact length of 100 μm [the blue curve in Fig. 5(c)] is virtually identical to the source resistance in the experiments (where the contact length is 200 μm). For small contact voltages, we calculate a source resistance of 1.2 kΩ cm, almost identical to the contact resistance obtained experimentally (1.4 kΩ cm) using the TLM, which shows that the TLM is able to produce reliable results for the linear component of the contact resistance but fails whenever the contact resistance has a significant nonlinear contribution [12].

When the contact voltage increases beyond about 0.2 V, the source-sided contact resistance decreases monotonically. Interestingly, this decrease in contact resistance with increasing contact voltage is more pronounced when the contact length is small [the red and black curves in Fig. 5(c)]. This relationship can be understood by considering that a larger contact resistance causes the charges to be injected and transported within a smaller area underneath the source, and, owing to the nonlinear nature of the contact resistance, this is compensated for by a larger contact voltage, which also explains why the same applied drain-source voltage (−3 V) produces a contact voltage of 1 V when the contact length is 100 μm [the blue curve in Fig. 5(c)], but a contact voltage of 2 V when the contact length is 0.1 μm [the black curve in Fig. 5(c)].

D. Influence of contact resistance on TFT performance

To explore the influence of the contact resistance on the TFT performance, we perform additional simulations, again using the parameters given in Table I. We find that the detailed knowledge of the contact resistance obtained through the simulations discussed in the previous sections provides valuable insight into various static and dynamic transistor parameters. For example, in the literature, it is often assumed that the transfer length, i.e., the characteristic length over which 63% of the charge-carrier exchange between the contacts and the semiconductor occurs [25,27], is independent of the channel length. However, our simulations reveal that the transfer length does in fact show a significant dependence on the channel length. This relation can be seen in Fig. 6, where the simulated current that flows laterally in the CAZ underneath the source contact (i.e., in the source region) while collecting the injected charges is plotted as a function of the lateral position underneath the source contact (relative to the contact edge) for TFTs with channel lengths ranging from 200 to 0.1 μm. From these data, the transfer length of the source contact, $L_{T,S}$, has been calculated for each channel length, and the results are plotted in Figs. 6 and 7(a). The results show that when the channel length is large—i.e., when the applied drain-source voltage drops mostly along the channel and thus the vertical contact voltage is small—the source resistivity is linear [see Fig. 5(b)], and the relationship between the lateral current and the position underneath the source contact is exponential. In this case, the calculated transfer length at the source (15 μm) is virtually identical to the transfer length obtained experimentally by the TLM (16 μm; see Ref. [12]). However, in contrast to the TLM, our approach makes it possible to distinguish between a source-sided and a drain-sided transfer length. As the channel length is reduced, the contact voltage increases [see Fig. 5(c)], the contact resistance becomes nonlinear (see Fig. 5), and the transfer length thus decreases significantly, to less than 5 μm for submicron channel lengths. Because this dependence of the transfer length on the channel length is caused by the nonlinear contributions to the contact resistance, it is not captured by the TLM and thus is rarely discussed in the literature. In our TFTs, the transition from purely linear to nonlinear contact resistance occurs when the channel length is smaller than about 50 μm and the channel-width-normalized drain current exceeds about 20 μA/mm at gate-source and drain-source voltages of −3 V.

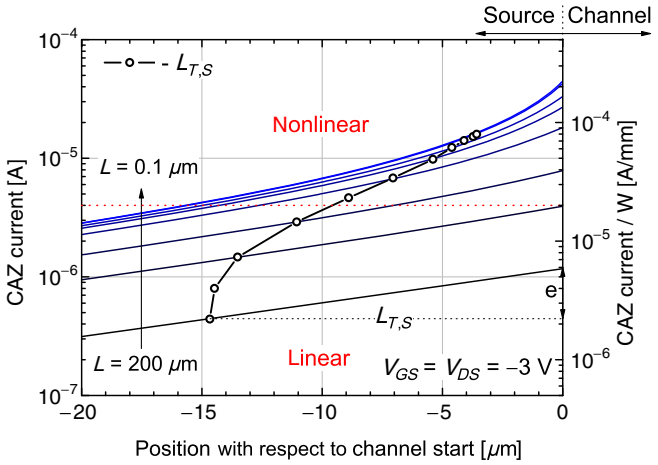

FIG. 6. Simulated current flowing laterally in the charge accumulation zone (CAZ) underneath the source contact, plotted as a function of the lateral position underneath the source contact relative to the contact edge for TFTs with channel lengths ranging from 200 to 0.1 μm. Also plotted is the transfer length of the source contact, $L_{T,S}$, calculated for each channel length. For large channel lengths, i.e., when the contact voltage is small and the source resistance is linear [see Fig. 5(c)], the relationship between the lateral current and the position underneath the source contact is exponential and the transfer length is large (15 μm). However, for smaller channel lengths, the contact resistance is nonlinear and, therefore, the transfer length is smaller.

Another aspect that can be quantitatively assessed through the simulations is the relationship between the effective carrier mobility μ_{eff}, calculated from the drain current in the saturation regime and the threshold voltage

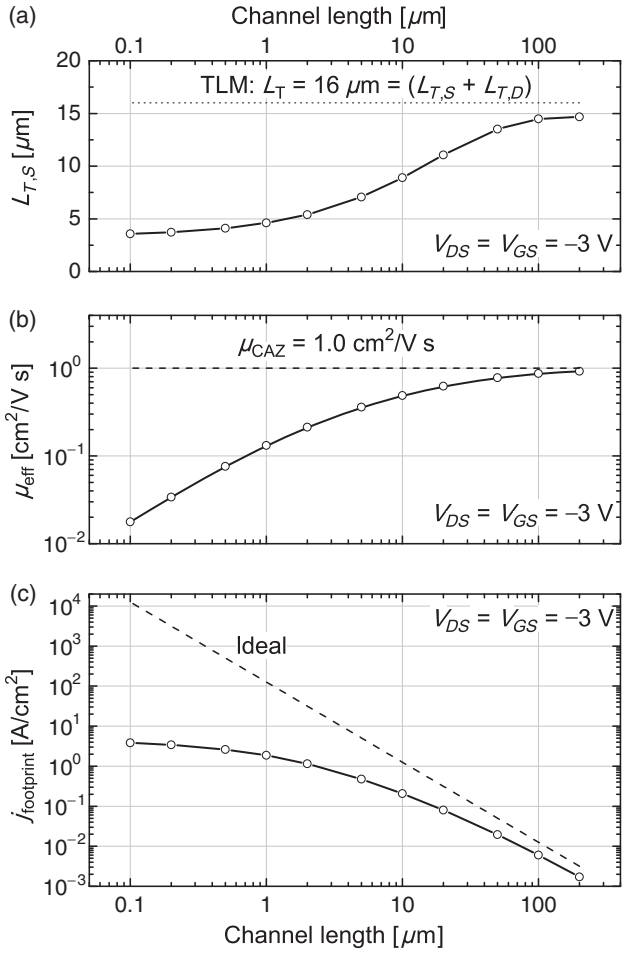

FIG. 7. Simulated dependence of (a) the source-sided transfer length, (b) the effective carrier mobility, and (c) the footprint current density on the channel length. The dashed line (ideal) represents zero contact resistance and zero contact length. The drain-sided transfer length is negligible ($L_{T,D} < 50$ nm) in the saturation regime and is thus neglected in (a).

used for the simulations, and the channel length. Qualitatively, it is well known that the effective mobility is close to the CAZ mobility for large channel lengths but decreases significantly for small channel lengths due to the influence of the contact resistance [12]. With the help of our simulations, the effective mobility that can be expected for extremely small channel lengths can be determined as well [see Fig. 7(b)].

To facilitate meaningful comparisons between the lateral TFTs considered here and some of the vertical TFTs reported in the literature [73–77] in terms of the current per the footprint area, it can be useful to calculate the footprint current density, which we define as the drain current divided by the area occupied by the channel region and the regions underneath the source and drain contacts through which 63% of the drain current is exchanged with the charge accumulation zone, i.e., the areas given by the channel length and the source and drain transfer lengths:

$$j_{\text{footprint}} = \frac{0.63 I_D}{W(L_{T,S} + L + L_{T,D})}. \tag{11}$$

In Fig. 7(c), the footprint current density calculated according to Eq. (11) is plotted as a function of the channel length. As expected, the footprint current density increases with decreasing channel length, but the increase is smaller than it would be in the absence of any contact resistance.

Finally, we use the simulation to illustrate the dependence of the transit frequency on the channel length L and the contact length L_C in the presence of nonlinear contact resistances. We define the transit frequency here as the frequency that is obtained by plotting the current gain versus the frequency in a log-log plot and extrapolating the slope of the curve to unity current gain (see Fig. S7 of the Supplemental Material [51]). Also, we note that the results presented here are valid only for the exact geometry and the exact potentials considered in the simulations. For example, we will only consider TFTs in which the contact lengths of the source and drain contacts are identical; in asymmetric TFTs, the results will obviously be different [78].

The results are shown in Fig. 8. In Fig. 8(a), the simulated transit frequency is plotted as a function of the channel length for four different contact lengths. The dotted line indicates the slope with which the transit frequency would depend on the channel length if the contact resistance and the contact length were both zero ($R_{C,S} = 0$, $R_{C,D} = 0$, $L_C = 0$, and $f_T \propto L^{-2}$). In reality, i.e., in the presence of contact resistances, the slope of the curve f_T vs L is significantly smaller, especially at small channel lengths, due to the influence of the contact resistance and the parasitic gate-to-contact overlap capacitances [79]. Nevertheless, with all else being equal, a smaller channel length always leads to a larger transit frequency, simply because of the smaller intrinsic capacitance.

In Fig. 8(b), the simulated transit frequency is plotted as a function of the contact length for three different channel lengths. As can be seen, the transit frequency increases quite significantly as the contact length is decreased from 100 μm to approximately the transfer length. However, when the contact length is decreased below 1 μm, the contact resistance increases dramatically [see Fig. 5(c)], which reduces and eventually eliminates the benefit of the smaller parasitic overlap capacitance [80]. As a result, there is a channel-length-dependent optimum contact length at which the transit frequency has its maximum and beyond which the transit frequency saturates or may actually decrease. This is an important difference between the coplanar TFT structure, where reducing the contact length always leads to an increase in the transit frequency [81,82], and the staggered TFT structure considered here. However, Fig. 6(a) illustrates a critical and typically overlooked effect of the nonlinearity of the contact resistance: At small channel lengths, the nonlinearity of the contact resistance results in a larger-than-expected drain current and hence a

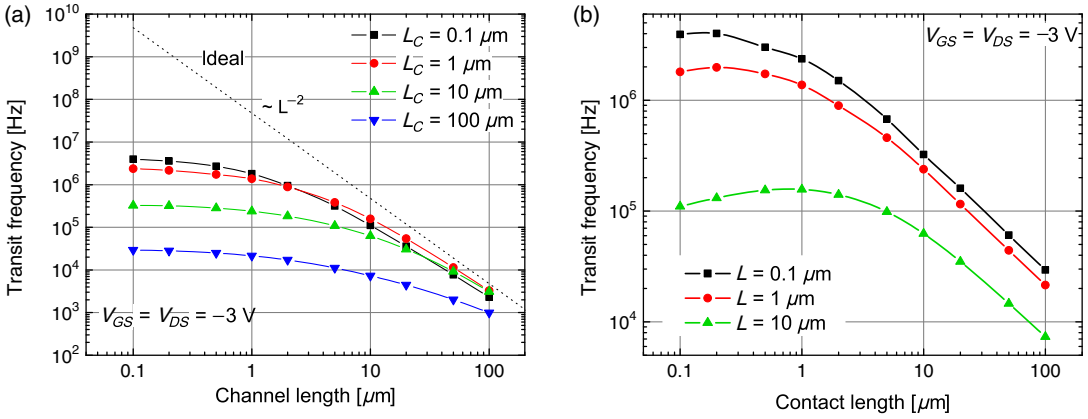

FIG. 8. Simulated transit frequency as a function of (a) the channel length, and (b) the contact length. The dashed line (ideal) in (a) represents zero contact resistance and zero contact length.

smaller-than-expected transfer length (also seen in Fig. 7). Because of this smaller-than-expected transfer length, the benefit of reducing the contact length is extended to significantly smaller contact lengths than would be involved if the contact resistance were purely linear, which is a result that has recently been discussed in the literature [30].

For the pentacene TFTs considered in our simulations, transit frequencies beyond 1 MHz are predicted for a channel length of 1 μm and a contact length of 2 μm at gate-source and drain-source voltages of −3 V. In experiments, frequencies greater than 1 MHz have indeed been measured on TFTs fabricated with the same device structure and the same fabrication process as those considered here, but using a different organic semiconductor, dinaphtho[2,3-*b*:2′,3′-*f*]thieno[3,2-*b*]thiophene [83]. However, Fig. 5(b) clearly shows that the TFTs can operate at this frequency only because the contact resistance is nonlinear at these voltages; if the contact resistance of our TFT were only linear, the maximum transit frequency would be significantly smaller than 1 MHz. This insight into the significance of the nonlinearity of the contact resistance in determining the transit frequency of staggered TFTs is one of the most important results of our study.

III. CONCLUSION

In this work, we introduce a semiphenomenological approach to model the static and dynamic behavior of staggered thin-film transistors that provides excellent agreement with experimental data. The model takes into account the inherent nonlinearity of the contact resistance, which is a property that is not captured by the transmission-line method and hence is usually ignored. The basis for the model is an equivalent network circuit that includes all three regions of the TFTs (source, channel, and drain), describes the linear and nonlinear components of the injection and transport of the charges, takes into account the intrinsic and parasitic capacitances, and can be solved in a relatively short computation time using freely available simulation software.

As all of the critical electrical potentials and currents are readily accessible, the model is ideally suited to analyzing the influence of the TFT geometry and dimensions on the contact resistance and to evaluating hypotheses whenever experiments reveal unexpected behavior. The physically correct description of the contact resistance in the simulations makes it possible to analyze a wide range of device nonidealities, such as threshold-voltage roll-off and carrier-density-dependent mobility. Our approach can be easily implemented into a full compact device model with an integrated simulation level; is able to calculate the static and dynamic performance of various TFT circuits, such as pixel or display drivers, depending on the TFT dimensions; and can thus be helpful in the optimization of the design in terms of real-estate utilization and high-frequency operation.

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[1] S. D. Brotherton, *Introduction to Thin Film Transistors: Physics and Technology of TFTs* (Springer, Dordrecht, 2013).

[2] Henning Sirringhaus, 25th anniversary article: Organic field-effect transistors: The path beyond amorphous silicon, Adv. Mater. **26**, 1319 (2014).

[3] Agnès Tixier-Mita, Satoshi Ihida, Bertrand-David Sgard, Grant A. Cathcart, Takuya Takahashi, Hiroyuki Fujita, and Hiroshi Toshiyoshi, Review on thin-film transistor technology, its applications, and possible new applications to biological cells, Jpn. J. Appl. Phys. **55**, 04EA08 (2016).

[4] S. D. Brotherton, C. Glasse, C. Glaister, P. Green, F. Rohlfing, and J. R. Ayres, High-speed, short-channel polycrystalline silicon thin-film transistors, Appl. Phys. Lett. **84**, 293 (2004).

[5] Isaac Chan, Saeed Fathololoumi, and Arokia Nathan, Nanoscale channel and small area amorphous silicon vertical thin film transistor, J. Vac. Sci. Technol. A **24**, 869 (2006).

[6] K. H. Cherenack, B. Hekmatshoar, J. C. Sturm, and S. Wagner, Self-aligned amorphous silicon thin-film transistors

fabricated on clear plastic at 300 °C, IEEE Trans. Electron Devices **57**, 2381 (2010).

[7] Masatoshi Kitamura and Yasuhiko Arakawa, High current-gain cutoff frequencies above 10 MHz in *n*-channel C_{60} and *p*-channel pentacene thin-film transistors, Jpn. J. Appl. Phys. **50**, 01BC01 (2011).

[8] N. Münzenrieder, L. Petti, C. Zysset, T. Kinkeldei, G. A. Salvatore, and G. Tröster, Flexible self-aligned amorphous InGaZnO thin-film transistors with submicrometer channel length and a transit frequency of 135 MHz, IEEE Trans. Electron Devices **60**, 2815 (2013).

[9] Andrea Perinot, Prakash Kshirsagar, Maria Ada Malvindi, Pier Paolo Pompa, Roberto Fiammengo, and Mario Caironi, Direct-written polymer field-effect transistors operating at 20 MHz, Sci. Rep. **6**, 38941 (2016).

[10] Anita Risteska, Kris Myny, Sören Steudel, Masakazu Nakamura, and Dietmar Knipp, Scaling limits of organic digital circuits, Org. Electron. **15**, 461 (2014).

[11] Niko Münzenrieder, Giovanni A. Salvatore, Luisa Petti, Christoph Zysset, Lars Büthe, Christian Vogt, Giuseppe Cantarella, and Gerhard Tröster, Contact resistance and overlapping capacitance in flexible sub-micron long oxide thin-film transistors for above 100 MHz operation, Appl. Phys. Lett. **105**, 263504 (2014).

[12] Ulrike Kraft, John E. Anthony, Emilie Ripaud, Marsha A. Loth, Edwin Weber, and Hagen Klauk, Low-voltage organic transistors based on tetraceno[2, 3-*b*]thiophene: Contact resistance and air stability, Chem. Mater. **27**, 998 (2015).

[13] Björn Lüssem, Chang-Min Keum, Daniel Kasemann, Ben Naab, Zhenan Bao, and Karl Leo, Doped organic transistors, Chem. Rev. **116**, 13714 (2016).

[14] Emily G. Bittle, James I. Basham, Thomas N. Jackson, Oana D. Jurchescu, and David J. Gundlach, Mobility overestimation due to gated contacts in organic field-effect transistors, Nat. Commun. **7**, 10908 (2016).

[15] Takafumi Uemura, Cedric Rolin, Tung-Huei Ke, Pavlo Fesenko, Jan Genoe, Paul Heremans, and Jun Takeya, On the extraction of charge carrier mobility in high-mobility organic transistors, Adv. Mater. **28**, 151 (2016).

[16] C. Liu, G. Li, R. Di Pietro, J. Huang, Y. Y. Noh, X. Liu, and T. Minari, Device Physics of Contact Issues for the Overestimation and Underestimation of Carrier Mobility in Field-Effect Transistors, Phys. Rev. Appl. **8**, 034020 (2017).

[17] Hagen Klauk, Organic thin-film transistors, Chem. Soc. Rev. **39**, 2643 (2010).

[18] Dario Natali, Luca Fumagalli, and Marco Sampietro, Modeling of organic thin film transistors: Effect of contact resistances, J. Appl. Phys. **101**, 014501 (2007).

[19] A. Hoppe, D. Knipp, B. Gburek, A. Benor, M. Marinkovic, and V. Wagner, Scaling limits of organic thin film transistors, Org. Electron. **11**, 626 (2010).

[20] O. Simonetti, L. Giraudet, T. Maurel, J.-L. Nicolas, and A. Belkhir, Organic transistor model with nonlinear injection: Effects of uneven source contact on apparent mobility and threshold voltage, Org. Electron. **11**, 1381 (2010).

[21] C. H. Kim, Y. Bonnassieux, and G. Horowitz, Charge distribution and contact resistance model for coplanar organic field-effect transistors, IEEE Trans. Electron Devices **60**, 280 (2013).

[22] Fabrizio Torricelli, Matteo Ghittorelli, Luigi Colalongo, and Zsolt-Miklos Kovacs-Vajna, Single-transistor method for the extraction of the contact and channel resistances in organic field-effect transistors, Appl. Phys. Lett. **104**, 093303 (2014).

[23] Chang Hyun Kim, Y. Bonnassieux, and Gilles Horowitz, Fundamental benefits of the staggered geometry for organic field-effect transistors, IEEE Electron Device Lett. **32**, 1302 (2011).

[24] Brijesh Kumar, Brajesh Kumar Kaushik, and Yuvraj Singh Negi, Modeling of top and bottom contact structure organic field effect transistors, J. Vac. Sci. Technol. B **31**, 012401 (2013).

[25] H. H. Berger, Contact resistance and contact resistivity, J. Electrochem. Soc. **119**, 507 (1972).

[26] G. K. Reeves and H. B. Harrison, Obtaining the specific contact resistance from transmission line model measurements, IEEE Electron Device Lett. **3**, 111 (1982).

[27] R. Rödel, F. Letzkus, T. Zaki, J. N. Burghartz, U. Kraft, U. Zschieschang, K. Kern, and H. Klauk, Contact properties of high-mobility, air-stable, low-voltage organic *n*-channel thin-film transistors based on a naphthalene tetracarboxylic diimide, Appl. Phys. Lett. **102**, 233303 (2013).

[28] Keum-Dong Jung, Yoo Chul Kim, Byeong-Ju Kim, Byung-Gook Park, Hyungcheol Shin, and Jong Duk Lee, An analytic current-voltage equation for top-contact organic thin film transistors including the effects of variable series resistance, Jpn. J. Appl. Phys. **47**, 3174 (2008).

[29] M. Nurul Islam and B. Mazhari, An analytical model for current crowding and source contact resistance in top-contact organic thin-film transistors, Semicond. Sci. Technol. **23**, 125027 (2008).

[30] Dario Natali, Jiaren Chen, Francesco Maddalena, Francisco García Ferré, Fabio Di Fonzo, and Mario Caironi, Injection length in staggered organic thin film transistors: Assessment and implications for device downscaling, Adv. Electron. Mater. **2**, 1600097 (2016).

[31] Marko Marinkovic, Dagmawi Belaineh, Veit Wagner, and Dietmar Knipp, On the origin of contact resistances of organic thin film transistors, Adv. Mater. **24**, 4005 (2012).

[32] Nevill. F. Mott and Ronald W. Gurney, *Electronic Processes in Ionic Crystals*, 2nd ed. (Clarendon Press, Oxford, 1953).

[33] M. Schwoerer and C. H. Wolf, *Organische Molekulare Festkrper—Einfhrung in die Physik von π-Systemen*, 1st ed. (Wiley-VCH, Weinheim, 2005).

[34] N. Tessler and Y. Roichman, Two-dimensional simulation of polymer field-effect transistor, Appl. Phys. Lett. **79**, 2987 (2001).

[35] I. G. Hill, Numerical simulations of contact resistance in organic thin-film transistors and Appl, Phys. Lett. **87**, 163505 (2005).

[36] P. Gaucci, A. Valletta, L. Mariucci, G. Fortunato, and S. D. Brotherton, Numerical simulation of parasitic resistance effects in polycrystalline silicon TFTs, IEEE Trans. Electron Devices **53**, 573 (2006).

[37] Susanne Scheinert and Gernot Paasch, Interdependence of contact properties and field- and density-dependent mobility in organic field-effect transistors, J. Appl. Phys. **105**, 014509 (2009).

[38] J. J. Brondijk, W. S. C. Roelofs, S. G. J. Mathijssen, A. Shehu, T. Cramer, F. Biscarini, P. W. M. Blom, and D. M. de Leeuw, Two-Dimensional Charge Transport in Disordered Organic Semiconductors, Phys. Rev. Lett. **109**, 056601 (2012).

[39] M. Gruber, F. Schürrer, and K. Zojer, Relation between injection barrier and contact resistance in top-contact organic thin-film transistors, Org. Electron. **13**, 1887 (2012).

[40] Manfred Gruber, Egbert Zojer, Ferdinand Schürrer, and Karin Zojer, Impact of materials versus geometric parameters on the contact resistance in organic thin-film transistors, Adv. Funct. Mater. **23**, 2941 (2013).

[41] M. Nurul Islam and B. Mazhari, Organic thin film transistors with asymmetrically placed source and drain contact, Org. Electron. **14**, 862 (2013).

[42] N. J. Watkins, Li Yan, and Yongli Gao, Electronic structure symmetry of interfaces between pentacene and metals, Appl. Phys. Lett. **80**, 4384 (2002).

[43] S. D. Wang, T. Minari, T. Miyadera, K. Tsukagoshi, and Y. Aoyagi, Contact-metal dependent current injection in pentacene thin-film transistors, Appl. Phys. Lett. **91**, 203508 (2007).

[44] J. Campbell Scott and George G. Malliaras, Charge injection and recombination at the metal-organic interface, Chem. Phys. Lett. **299**, 115 (1999).

[45] Dario Natali and Mario Caironi, Charge injection in solution-processed organic field-effect transistors: Physics, models and characterization methods, Adv. Mater. **24**, 1357 (2012).

[46] Anita Risteska, Sören Steudel, Masakazu Nakamura, and Dietmar Knipp, Structural ordering versus energy band alignment: Effects of self-assembled monolayers on the metal/semiconductor interfaces of small molecule organic thin-film transistors, Org. Electron. **15**, 3723 (2014).

[47] Chuan Liu, Gunel Huseynova, Yong Xu, Dang Xuan Long, Won-Tae Park, Xuying Liu, Takeo Minari, and Yong-Young Noh, Universal diffusion-limited injection and the hook effect in organic thin-film transistors, Sci. Rep. **6**, 29811 (2016).

[48] Hamidreza Karimi-Alavijeh and Alireza Katebi-Jahromi, An analytical solution for contact resistance of staggered organic field-effect transistors, J. Appl. Phys. **121**, 105501 (2017).

[49] Hamidreza Karimi-Alavijeh, Modeling the gate-bias dependence of contact resistance in staggered organic field effect transistors based on carrier-concentration dependent mobility, J. Appl. Phys. **119**, 105501 (2016).

[50] See http://link.aps.org/supplemental/10.1103/PhysRevApplied.000.000000.

[51] See Supplemental Material at http://link.aps.org/supplemental/10.1103/PhysRevApplied.8.054012 for a comparison of further parameters and a guide to our fitting procedure.

[52] H. Shichman and D. A. Hodges, Modeling and simulation of insulated-gate field-effect transistor switching circuits, IEEE J. Solid-State Circuits **3**, 285 (1968).

[53] T. J. Richards and H. Sirringhaus, Analysis of the contact resistance in staggered, top-gate organic field-effect transistors, J. Appl. Phys. **102**, 094510 (2007).

[54] J. Campbell Scott, Metal-organic interface and charge injection in organic electronic devices, J. Vac. Sci. Technol. A **21**, 521 (2003).

[55] B. N. Limketkai and M. A. Baldo, Charge injection into cathode-doped amorphous organic semiconductors, Phys. Rev. B **71**, 085207 (2005).

[56] G. A. H. Wetzelaer and P. W. M. Blom, Ohmic current in organic metal-insulator-metal diodes revisited, Phys. Rev. B **89**, 241201 (2014).

[57] C. D. Dimitrakopoulos and P. R. L. Malenfant, Organic thin film transistors for large area electronics, Adv. Mater. **14**, 99 (2002).

[58] Jiyoul Lee, D. K. Hwang, C. H. Park, S. S. Kim, and Seongil Im, Pentacene-based photodiode with Schottky junction, Thin Solid Films **451–452**, 12 (2004).

[59] Sieu D. Ha, Yabing Qi, and Antoine Kahn, Relative permittivity and Hubbard u of pentacene extracted from scanning tunneling microscopy studies of p-doped films, Chem. Phys. Lett. **495**, 212 (2010).

[60] Chang Hyun Kim, Omid Yaghmazadeh, Denis Tondelier, Yong Bin Jeong, Yvan Bonnassieux, and Gilles Horowitz, Capacitive behavior of pentacene-based diodes: Quasistatic dielectric constant and dielectric strength, J. Appl. Phys. **109**, 083710 (2011).

[61] Paul Pahner, Hans Kleemann, Lorenzo Burtone, Max L. Tietze, Janine Fischer, Karl Leo, and Björn Lüssem, Pentacene Schottky diodes studied by impedance spectroscopy: Doping properties and trap response, Phys. Rev. B **88**, 195205 (2013).

[62] Heinz Bässler and Anna Köhler, in *Unimolecular and Supramolecular Electronics I*, Topics in Current Chemistry Vol. 312, edited by Robert M. Metzger (Springer, Berlin, 2012), p. 1.

[63] A. Sharma, F. W. A. van Oost, M. Kemerink, and P. A. Bobbert, Dimensionality of charge transport in organic field-effect transistors, Phys. Rev. B **85**, 235302 (2012).

[64] M. Bouhassoune, S. L. M. van Mensfoort, P. A. Bobbert, and R. Coehoorn, Carrier-density and field-dependent charge-carrier mobility in organic semiconductors with correlated Gaussian disorder, Org. Electron. **10**, 437 (2009).

[65] Ulrike Kraft, Kazuo Takimiya, Myeong Jin Kang, Reinhold Rödel, Florian Letzkus, Joachim N. Burghartz, Edwin Weber, and Hagen Klauk, Detailed analysis and contact properties of low-voltage organic thin-film transistors based on dinaphtho[2, 3-b:2′, 3′-f]thieno[3, 2-b]thiophene (DNTT) and its didecyl and diphenyl derivatives, Org. Electron. **35**, 33 (2016).

[66] S. Chamberlain and S. Ramanan, Drain-induced barrier-lowering analysis in VSLI MOSFET devices using two-dimensional numerical simulations, IEEE Trans. Electron Devices, **33**, 1745 (1986).

[67] S. Jain, Measurement of threshold voltage and channel length of submicron MOSFETs, IEE Proc., Part I: Solid-State Electron Devices **135**, 162 (1988).

[68] K. Goto, Y. Tagawa, H. Ohta, H. Morioka, S. Pidin, Y. Momiyama, H. Kokura, S. Inagaki, N. Tamura, M. Hori, T. Mori, M. Kase, K. Hashimoto, M. Kojima, and T. Sugii, High performance 25 nm gate CMOSFETs for 65 nm node high speed MPUs, in *Proceedings of the International Electron Devices Meeting (IEDM '03), Washington, DC,*

2003 (IEEE, New York, 2003), p. 27.1.1, http://ieeexplore.ieee.org/document/1269358/.

[69] Chun-Hsing Shih, Yi-Min Chen, and Chenhsin Lien, An analytical model of short-channel effect for metal-oxide-semiconductor field-effect transistor with insulated shallow extension, Jpn. J. Appl. Phys. **43**, 12 (2004).

[70] Joshua N. Haddock, Xiaohong Zhang, Shijun Zheng, Qing Zhang, Seth R. Marder, and Bernard Kippelen, A comprehensive study of short channel effects in organic field-effect transistors, Org. Electron. **7**, 45 (2006).

[71] Alrun A. Günther, Johannes Widmer, Daniel Kasemann, and Karl Leo, Hole mobility in thermally evaporated pentacene: Morphological and directional dependence, Appl. Phys. Lett. **106**, 233301 (2015).

[72] Axel Fischer, Paul Pahner, Björn Lüssem, Karl Leo, Reinhard Scholz, Thomas Koprucki, Jürgen Fuhrmann, Klaus Gärtner, and Annegret Glitzky, Self-heating effects in organic semiconductor crossbar structures with small active area, Org. Electron. **13**, 2461 (2012).

[73] M. Uno, Y. Hirose, T. Uemura, K. Takimiya, Y. Nakazawa, and J. Takeya, High-power and high-speed organic three-dimensional transistors with submicrometer channels, Appl. Phys. Lett. **97**, 013301 (2010).

[74] Mitchell A. McCarthy, Bo Liu, and Andrew G. Rinzler, High current, low voltage carbon nanotube enabled vertical organic field effect transistors, Nano Lett. **10**, 3467 (2010).

[75] Michael Greenman, Ariel J. Ben-Sasson, Zhihua Chen, Antonio Facchetti, and Nir Tessler, Fast switching characteristics in vertical organic field effect transistors, Appl. Phys. Lett. **103**, 073502 (2013).

[76] Markus P. Klinger, Axel Fischer, Felix Kaschura, Reinhard Scholz, Björn Lüssem, Bahman Kheradmand-Boroujeni, Frank Ellinger, Daniel Kasemann, and Karl Leo, Advanced organic permeable-base transistor with superior performance, Adv. Mater.**27**, 7734 (2015).

[77] Björn Lüssem, Alrun Günther, Axel Fischer, Daniel Kasemann, and Karl Leo, Vertical organic transistors, J. Phys. Condens. Matter **27**, 443003 (2015).

[78] Tarek Zaki, Reinhold Rödel, Florian Letzkus, Harald Richter, Ute Zschieschang, Hagen Klauk, and Joachim N. Burghartz, AC characterization of organic thin-film transistors with asymmetric gate-to-source and gate-to-drain overlaps, Org. Electron. **14**, 1318 (2013).

[79] N. Münzenrieder, P. Voser, L. Petti, C. Zysset, L. Buthe, C. Vogt, G. A. Salvatore, and G. Tröster, Flexible self-aligned double-gate IGZO TFT, IEEE Electron Device Lett. **35**, 69 (2014).

[80] Frederik Ante, Daniel Kälblein, Tarek Zaki, Ute Zschieschang, Kazuo Takimiya, Masaaki Ikeda, Tsuyoshi Sekitani, Takao Someya, Joachim N. Burghartz, Klaus Kern, and Hagen Klauk, Contact resistance and megahertz operation of aggressively scaled organic transistors, Small **8**, 73 (2012).

[81] Stuart G. Higgins, Beinn V. O. Muir, Jessica Wade, Jiaren Chen, Bernd Striedinger, Herbert Gold, Barbara Stadlober, Mario Caironi, Ji-Seon Kim, Joachim H. G. Steinke, and Alasdair J. Campbell, Self-aligned megahertz organic transistors solution-processed on plastic, Adv. Electron. Mater. **1**, 1500024 (2015).

[82] S. G. Higgins, B. V. O. Muir, G. Dell'Erba, A. Perinot, M. Caironi, and A. J. Campbell, Self-aligned organic field-effect transistors on plastic with picofarad overlap capacitances and megahertz operating frequencies, Appl. Phys. Lett. **108**, 023302 (2016).

[83] T. Zaki, S. Scheinert, I. Hörselmann, R. Rödel, F. Letzkus, H. Richter, U. Zschieschang, H. Klauk, and J. N. Burghartz, Accurate capacitance modeling and characterization of organic thin-film transistors, IEEE Trans. Electron Devices **61**, 98 (2014).