Gate-Driven Pure Spin Current in Graphene

Xiaoyang Lin,[1] Li Su,[1,2,3] Zhizhong Si,[1] Youguang Zhang,[1] Arnaud Bournel,[2,3] Yue Zhang,[1] Jacques-Olivier Klein,[2,3] Albert Fert,[1,4] and Weisheng Zhao[1,*]

[1]*Fert Beijing Research Institute, School of Electrical and Information Engineering, BDBC, Beihang University, Beijing 100191, China*

[2]*Centre for Nanoscience and Nanotechnology (C2N), Université Paris-Sud, Université Paris-Saclay, F-91405 Orsay, France*

[3]*UMR 8622, CNRS, F-91405 Orsay, France*

[4]*Unité Mixte de Physique CNRS-Thales, F-91767 Palaiseau, France*

(Received 26 September 2016; revised manuscript received 21 June 2017; published 11 September 2017)

The manipulation of spin current is a promising solution for low-power devices beyond CMOS. However, conventional methods, such as spin-transfer torque or spin-orbit torque for magnetic tunnel junctions, suffer from large power consumption due to frequent spin-charge conversions. An important challenge is, thus, to realize long-distance transport of pure spin current, together with efficient manipulation. Here, the mechanism of gate-driven pure spin current in graphene is presented. Such a mechanism relies on the electrical gating of carrier-density-dependent conductivity and spin-diffusion length in graphene. The gate-driven feature is adopted to realize the pure spin-current demultiplexing operation, which enables gate-controllable distribution of the pure spin current into graphene branches. Compared with the Elliott-Yafet spin-relaxation mechanism, the D'yakonov-Perel spin-relaxation mechanism results in more appreciable demultiplexing performance. The feature of the pure spin-current demultiplexing operation will allow a number of logic functions to be cascaded without spin-charge conversions and open a route for future ultra-low-power devices.

DOI: 10.1103/PhysRevApplied.8.034006

I. INTRODUCTION

The manipulation of spin current is considered a promising solution to build up low-power devices beyond CMOS (complementary metal-oxide semiconductor) technology for nonvolatile memory and logic computation [1–4]. The development in magnetic-tunnel-junction (MTJ) devices for small magnetic field sensing through the tunneling magnetoresistance effect has led to the rapid progress of hard-drive capacity and the emergence of magnetic random-access memory in the past 20 years [1,5]. For nanoscale MTJ devices, spin current can be utilized as efficient switching methods through the spin-transfer-torque or spin-orbit-torque effect, allowing low-power memory operations without magnetic fields [6–10]. However, further integrations of these spintronic devices with CMOS transistors for logic applications consume much higher power due to the fact that frequent spin-charge conversions are required to cascade the logic gates [11], as limited by the short spin-current transport distance.

In recent years, graphene has attracted considerable attention for logic applications. However, the semimetal property (i.e., the lack of an energy gap) of graphene becomes a vital impediment for graphene-based transistors [12,13]. Thanks to its superior features like high electronic mobility, weak spin-orbit coupling, and weak hyperfine interactions [14–16], graphene shows the longest spin-diffusion length (SDL) at room temperature [17–21] and becomes the best spin-current transport channel to realize spin logic [3,4]. A number of graphene-based spintronic devices have been proposed, such as spin transistors [22], magnetologic devices [23], and all-spin-logic devices [24,25]. However, these devices often suffer from high-power issues due to frequent conversions between spin signals and charge signals limited by the poor ability to manipulate spin current [3]. Thereby, the realization of both long-distance spin transport and efficient spin-current manipulation is the key issue for ultra-low-power spin logic [1–4].

Here, we describe the mechanism of gate-driven pure spin current in graphene to fill in this gap. Such a mechanism can be adopted to construct a graphene spin-current demultiplexer (GSDM), which can realize the demultiplexing operation to build up a fundamental block of spin logic. It is important to mention that spin current can be pure spin current or spin-polarized charge current; here, we use only pure spin current to retain the Joule-heat-free and ultra-low-power features. In a GSDM with a Y-shaped graphene channel, we demonstrate that such a mechanism relies on electrical gating of carrier-density-dependent conductivity and SDL in graphene.

*weisheng.zhao@buaa.edu.cn

Depending on the type of spin relaxation in graphene, e.g., the Elliott-Yafet (EY) mechanism [26] and D'yakonov-Perel (DP) mechanism [27,28], different performance of the demultiplexing operation can be achieved. Two typical cases are discussed in this paper, i.e., single-layer graphene (SLG) with the EY mechanism and bilayer graphene (BLG) with the DP mechanism. In particular, BLG with the DP mechanism is found to achieve a more appreciable gate-driven performance, which also implies the possibility to figure out spin-relaxation mechanisms in graphene using a structure similar to our GSDM. The unique feature of the pure spin-current demultiplexing operation allows a number of logic functions to be cascaded without spin-charge conversions and opens a route for the future low-power devices.

II. CONCEPT AND CALCULATION METHOD

A. Gate-driven pure spin current for demultiplexing operation in graphene

The Y-shaped GSDM with gate voltages ($V_{G,1}$ and $V_{G,2}$) applied on both branches of the graphene channel is schematically illustrated in Figs. 1(a) and 1(b) (top gates and/or back gates can be designed for practical applications). Pure spin currents are injected into these two branches through diffusion of the spin accumulation $\Delta\mu_s(x=0)$ at the bifurcation. This spin accumulation can be created by different spin-injection methods, e.g., electrical injection [14,29,30] or spin pumping [31,32], etc. The spin current density in branch i at a distance x from the bifurcation can be expressed as [33–35]

$$j_{s,i}(x, V_{G,i}) = \frac{\sigma_i}{e\lambda_{s,i}} \Delta\mu_s(x=0) e^{-x/\lambda_{s,i}}, \tag{1}$$

where σ_i is the conductivity, and $\lambda_{s,i}$ is the SDL of branch i. The ratio $\lambda_{s,i}/\sigma_i$ behaving like a "spin resistance," thus, dominates the distribution of pure spin current $j_{s,i}(x=0, V_{G,i})$ at the bifurcation ($x=0$) into the left and/or right branches, and the SDL $\lambda_{s,i}$ describes the propagation of the pure spin current in each branch (with a form of exponential decay $e^{-x/\lambda_{s,i}}$). Both σ_i and $\lambda_{s,i}$ can be controlled using the gate voltage $V_{G,i}$ via the corresponding carrier density n_i. As a result, the gate-voltage control

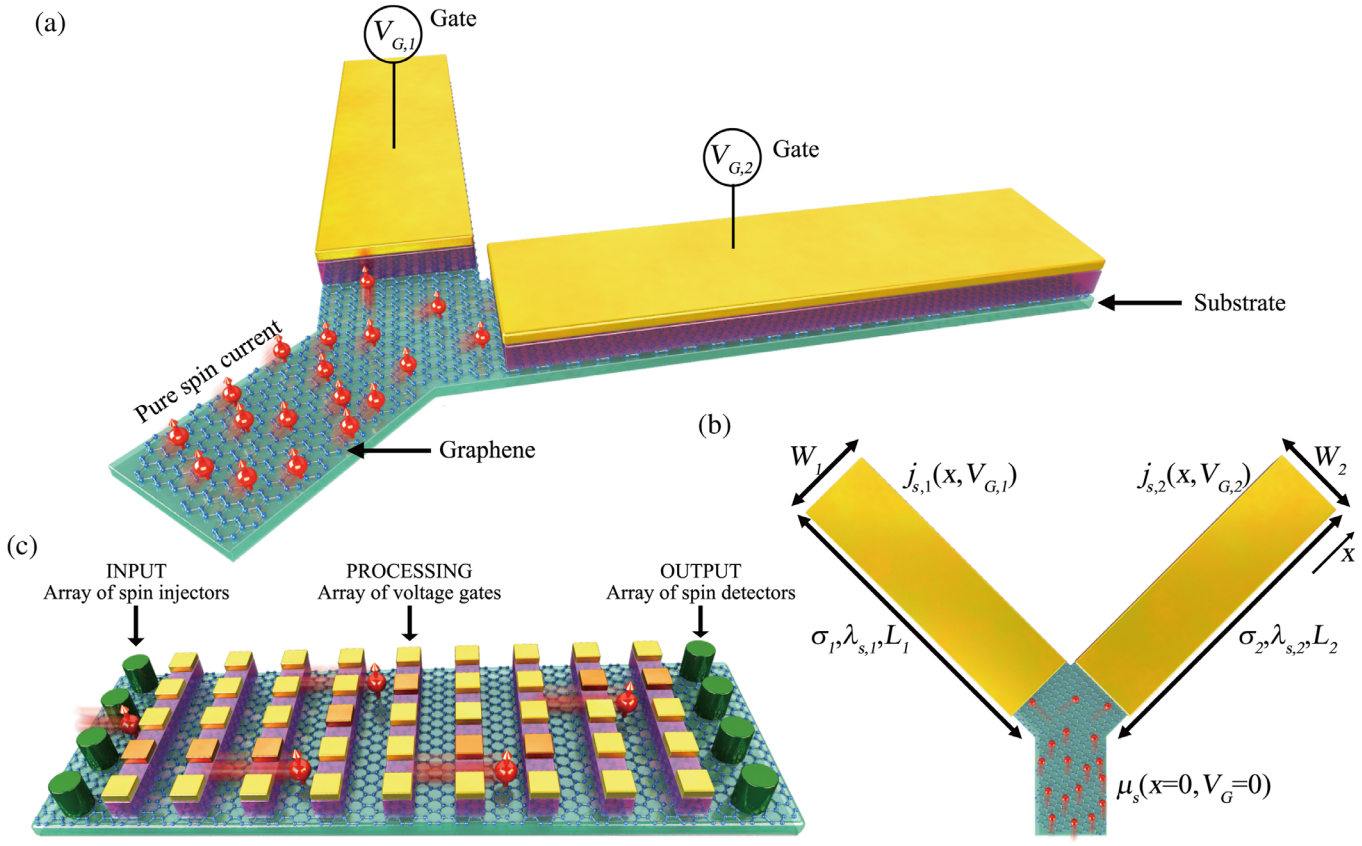

FIG. 1. Schematics of a GSDM for a reconfigurable spin-logic circuit. (a) A Y-shaped GSDM with gate voltages $V_{G,i}$ for voltage control of pure spin currents. (b) Top view of the Y-shaped GSDM with voltage control. Significant parameters are labeled in the figure, such as material characteristics [conductivity σ_i, spin-diffusion length $\lambda_{s,i}$, spin chemical potential $\mu_s(x=0)$, and spin current density $j_{s,i}(x, V_{G,i})$] and geometrical parameters (width W_i and distance x). A symmetric structure is considered, that is, $L_1 = L_2$ and $W_1 = W_2$. (c) Reconfigurable spin-logic circuit based on gate-driven pure spin current in graphene, with inputs (outputs) by spin injectors (detectors) and pure spin-current signal processing by voltage gates.

of the carrier density n_i, conductivity $\sigma_i(n_i)$, and SDL $\lambda_{s,i}(n_i)$ can be adopted to realize the demultiplexing operation, i.e., redirection or distribution of the pure spin current into specific branch(es). Notably, such a demultiplexing operation can realize magnetic-field-free pure spin-current reconfigurations for logic applications [Fig. 1(c)]. The input states of the spin injectors [denoted as "INPUT" in Fig. 1(c)] and the voltages of gates [denoted as "PROCESSING" in Fig. 1(c)] determine how the spin current flows from the INPUT through the PROCESSING region to the "OUTPUT," thus, resulting in exact output states of the spin detectors [denoted as OUTPUT in Fig. 1(c)]. As a result, it can work as a spin majority gate with fixed gate voltages but tunable input signals [25,35–37]. Through flexible designs of the gate voltages, it can also be programmable spin-logic circuits with certain logic functions or even neuromorphic spin-logic circuits [35–38]. To this end, the gate-driven demultiplexing operation of pure spin current in graphene is favorable to low-power spintronic circuits and energy-efficient architectures.

B. Dependence of conductivity and spin-diffusion length on carrier density

The conductivity σ can be expressed as $\sigma = \sigma(n) + \sigma_{\min}$, where the first term is proportional to the global carrier density n and mobility μ, while $\sigma_{\min}$ is the minimum conductivity induced by inhomogeneous charge distribution in the small-n limit [39,40]. We consider only the regime with sufficiently large n (typically $n > 10^{12}$ cm^{-2}), in which case, σ can be simplified as

$$\sigma = ne\mu. \tag{2}$$

In Eq. (2), the mobility μ turns out to be approximately independent of n for relatively large n in most experiments [40]. In this work, we use a typical high mobility of 15 000 cm^2/Vs for SLG (Ref. [40]) and a smaller mobility 10 000 cm^2/Vs for BLG (Refs. [41,42]). The second parameter in Eq. (1) is the SDL

$$\lambda_s = v_F(\tau_s\tau_p/2)^{1/2}, \tag{3}$$

where v_F is the Fermi velocity, τ_p is the momentum-relaxation time, and τ_s is the spin-relaxation time.

In graphene, the spin-relaxation mechanism can be the EY mechanism [21,43,44] or DP mechanism [43,45]. Recent theoretical and experimental results further indicate that the spin relaxation in SLG and BLG can be driven by the magnetic impurity [46–50] or the pseudospin [51]. For all types, it has been shown that the gate voltage can tune the spin-relaxation time. For the spin relaxation by magnetic impurities, it can be either EY-like [49] or DP-like [50] depending on the magnetic impurity level. For the spin relaxation by pseudospin, its behavior is similar to EY-like [51]. For simplicity, we investigate the gate-driven spin current in graphene with the EY mechanism or DP mechanism in this work.

1. Single-layer graphene

Considering the Einstein relation for electrons with linear dispersion, the conductivity in SLG is proportional to $\tau_{p,\mathrm{SLG}}n^{1/2}$, where $\tau_{p,\mathrm{SLG}}$ is the momentum-relaxation time in SLG. Consequently, the approximate n-independent mobility obtained in experiments corresponds to $\tau_{p,\mathrm{SLG}} \sim n^{1/2}$ [according to Eq. (2); see the complete expression of $\tau_{p,\mathrm{SLG}}$ and other parameters in Table I]. The variation of the spin-relaxation time on n depends on the type of spin-relaxation mechanism.

For the EY mechanism [26], $\tau_{s,\mathrm{EY}} \approx (E_F^2/\Delta_{\mathrm{EY}}^2)\tau_p$, where the spin-orbit energy is denoted as Δ_{EY}, and the Fermi

TABLE I. Carrier-density-dependent electronic and spin-relaxation parameters of GSDM.

	Single-layer graphene		Bilayer graphene	
E_F	$E_F = \hbar v_F\sqrt{(4\pi n/g_sg_v)}$		$E_F = (2\pi\hbar^2 n/m^* g_sg_v)$	
σ	$\sigma = \sigma(n) + \sigma_{\min} = ne\mu + \sigma_{\min}$			
τ_p	$\tau_p^{\mathrm{SLG}}(n) = (\sigma/e^2)(2\pi\hbar/v_F\sqrt{g_vg_s\pi n})$		$\tau_p^{\mathrm{BLG}}(n) = (m^*\sigma/e^2 n)$	
Spin relaxation	$\tau_{s,\mathrm{EY}} \approx (E_F^2/\Delta_{\mathrm{EY}}^2)\tau_p$	$\tau_{s,\mathrm{DP}} \approx (\hbar^2/4\Delta_{\mathrm{DP}}^2)(1/\tau_p)$	$\tau_{s,\mathrm{EY}} \approx (E_F^2/\Delta_{\mathrm{EY}}^2)\tau_p$	$\tau_{s,\mathrm{DP}} \approx (\hbar^2/4\Delta_{\mathrm{DP}}^2)(1/\tau_p)$
τ_s	$[8\pi^{3/2}\hbar^3 v_F\sqrt{n\sigma}]/[\Delta_{\mathrm{EY}}^2(g_vg_s)^{3/2}e^2]$	$(e^2\hbar v_F\sqrt{g_vg_s}/8\sqrt{\pi}\Delta_{\mathrm{DP}}^2)(\sqrt{n}/\sigma)$	$[4\pi\hbar^4 n\sigma]/[m^*\Delta_{\mathrm{EY}}^2(g_vg_s)^2e^2]$	$(\hbar^2e^2/4\Delta_{\mathrm{DP}}^2m^*)(n/\sigma)$
λ_s	$(\pi v_F\hbar^2\sqrt{8}/\Delta_{\mathrm{EY}}g_vg_s)\sigma$	$(\hbar v_F/\sqrt{8}\Delta_{\mathrm{DP}})$	$(2\pi\hbar^2 v_F/\Delta_{\mathrm{EY}}g_vg_se^2)\sigma$	$(\hbar v_F/\sqrt{8}\Delta_{\mathrm{DP}})$

Expressions of the Fermi energy E_F, conductivity σ, momentum-relaxation time τ_p, spin-relaxation time τ_s, and spin-diffusion length λ_s as a function of carrier density n for SLG (left) and BLG (right) dominated by the EY or DP spin-relaxation mechanism are listed. The calculations in the text are performed with $g_v = 2$ and $g_s = 2$ (the valley and spin degeneracies, respectively), $v_F \approx 10^6$ m s^{-1} for the Fermi velocity of SLG, and $m^* \approx 0.033m_e$ for effective mass of carriers in BLG.

energy is $E_F^2 \sim k_F^2 \sim n$ for Dirac electrons [52]. These parameters result in $\tau_{s,\mathrm{EY}} \sim n^{3/2}$. From Eq. (3) with $\tau_{p,\mathrm{SLG}} \sim n^{1/2}$, we can get

$$\lambda_{s,\mathrm{SLG,EY}} \sim n, \tag{4}$$

and, based on Eqs. (2) and (4), the prefactor of Eq. (1) λ_s/σ will be independent of n. According to Eq. (1) and the gate-tunable carrier density in graphene, the features of λ_s/σ and $\lambda_{s,\mathrm{SLG,EY}}$, thus, indicate that the pure spin-current demultiplexing operation can be realized in SLG with the EY mechanism based on the gate-driven feature: the distribution of pure spin current into the left and/or right branch at the bifurcation ($x = 0$) determined by λ_s/σ is not gate tunable; however, the decay of pure spin current in each branch away from the bifurcation ($x > 0$) determined by $\lambda_{s,\mathrm{SLG,EY}}$ is gate tunable.

For the DP mechanism [53], $\tau_{s,\mathrm{DP}} \approx (\hbar^2/4\Delta_{\mathrm{DP}}^2)(1/\tau_p)$. As a result, the SDL $\lambda_{s,\mathrm{SLG,DP}}$ of Eq. (3) is independent of n. Whereas, from Eq. (2),

$$\lambda_{s,\mathrm{SLG,DP}}/\sigma \sim n^{-1}. \tag{5}$$

Therefore, a pure spin-current demultiplexing operation can be realized in SLG with the DP mechanism based on the gate-driven feature: the distribution of pure spin current into the left and/or right branch at the bifurcation ($x = 0$) determined by λ_s/σ is gate tunable; however, the decay of pure spin current in each branch away from the bifurcation ($x > 0$) determined by $\lambda_{s,\mathrm{SLG,DP}}$ is not gate tunable.

2. Bilayer graphene

For BLG with quadratic dispersion, the mobility independent of n indicates a momentum-relaxation time independent of n. For the EY mechanism, $\tau_{s,\mathrm{EY}} \approx (E_F^2/\Delta_{\mathrm{EY}}^2)\tau_p$. Considering the relationship that $E_F \sim n$, $\tau_{s,\mathrm{EY}}$ is, thus, proportional to n^2. According to Eq. (3), we can get the SDL,

$$\lambda_{s,\mathrm{BLG,EY}} \sim n. \tag{6}$$

From Eqs. (2) and (6), λ_s/σ is independent of n. Thus, a pure spin-current demultiplexing operation can be realized in BLG with the EY mechanism utilizing the gate-driven feature: the distribution of pure spin current into the left and/or right branch at the bifurcation ($x = 0$) determined by λ_s/σ is not gate tunable; however, the decay of pure spin current in each branch away from the bifurcation ($x > 0$) determined by $\lambda_{s,\mathrm{BLG,EY}}$ is gate tunable.

Finally, for BLG with the DP mechanism, similarly, $\tau_s\tau_p$ and λ_s can be calculated to be independent of n and

$$\lambda_{s,\mathrm{BLG,DP}}/\sigma \sim n^{-1}. \tag{7}$$

Similar to SLG with the DP mechanism, a pure spin-current demultiplexing operation can be realized in BLG with the DP mechanism thanks to the gate-driven feature: the distribution of pure spin current into the left and/or right branch at the bifurcation ($x = 0$) determined by λ_s/σ is gate-tunable; however, the decay of pure spin current in each branch away from the bifurcation ($x > 0$) determined by $\lambda_{s,\mathrm{BLG,DP}}$ is not gate tunable.

C. CALCULATION METHOD

The performance of the pure spin-current demultiplexing operation is then evaluated quantitatively considering the gate-voltage-dependent carrier density [35]

$$n_i(V_{G,i}) = \epsilon_0\epsilon_G(V_{G,i} - V_{G,0})/(t_G e), \tag{8}$$

where n_i is the carrier density in branch i of the device with a gate voltage $V_{G,i}$, ϵ_0 is the dielectric constant, ϵ_G is the dielectric constant of the gates, t_G is the dielectric thickness, and $V_{G,0}$ is the voltage required at the charge neutrality point. We calculate the ratio $j_{s,1}(x, V_{G,1})/j_{s,2}(x, V_{G,2})$ between the pure spin currents in the two branches of our device for different values of effective gate voltages $v_{G,i} = V_{G,i} - V_{G,0}$. The calculation is performed for two typical cases, i.e., SLG with the EY mechanism (demultiplexing operation based on gate-driven propagations of pure spin current in each branch) and BLG with the DP mechanism (demultiplexing operation based on gate-driven distribution of pure spin current at the bifurcation). More complicated cases, for example, the case of a mixed EY and DP mechanism observed by Zomer *et al.* [54] or the spin relaxation driven by the magnetic impurity [46–50] or pseudospin [51], can also be processed as a straightforward extension of our approach.

III. RESULTS AND DISCUSSION

An appreciable demultiplexing operation of pure spin current should result in low-loss distribution of the input pure spin current into specific output ends. In this sense, a strategy based on the DP spin-relaxation mechanism is preferred, which enables a distinct distribution of pure spin current at the bifurcation and avoids unnecessary leakages of the pure spin current. Figures 2 and 3 present the performance of the pure spin-current demultiplexing operation of the GSDM based on the aforementioned mechanism. For the case of SLG with the EY mechanism, no difference in pure spin-current distribution into the left and/or right branch at the bifurcation can be found at any applied gate voltages [that is, $j_{s,1}/j_{s,2}(x = 0) = 1$; see Figs. 2(a) and 3(a)–3(d)]; however, the gate-driven propagation feature can be adopted to realize the demultiplexing operation of pure spin currents when x gets closer to or larger than the SDL in the branch

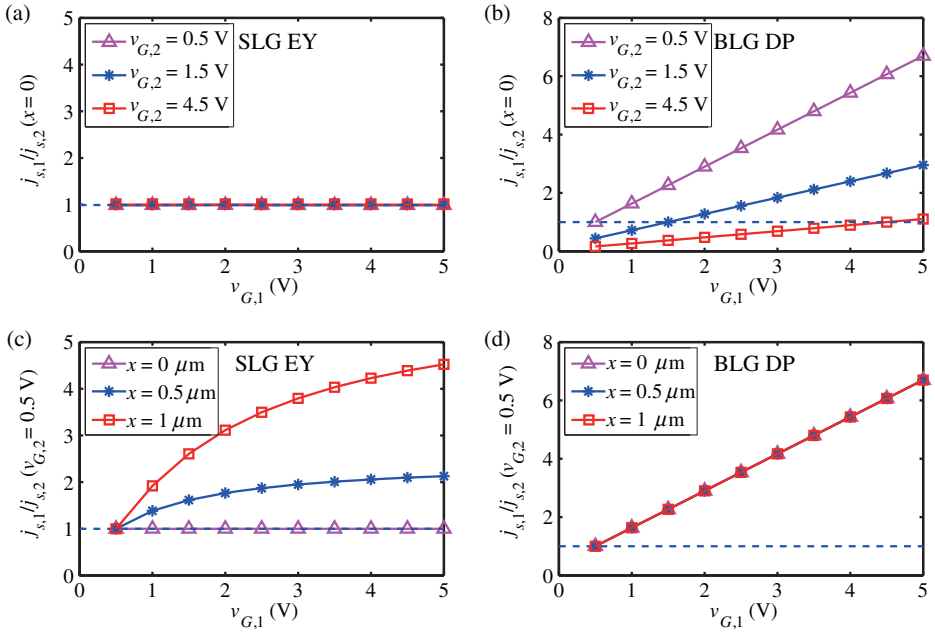

FIG. 2. Pure spin-current ratio of Y-shaped GSDM. The ratio between the pure spin current in the two branches $j_{s,1}/j_{s,2}$ is plotted as a function of $v_{G,1}$ for different values of $v_{G,2}$ or different distances x from the bifurcation of SLG with the EY mechanism (SLG EY) and BLG with the DP mechanism (BLG DP). The blue dashed line represents $j_{s,1}/j_{s,2} = 1$. (a),(b) $j_{s,1}/j_{s,2}$ at the bifurcation ($x = 0$) as a function of the effective gate voltage $v_{G,1} = V_{G,1} - V_{G,0}$ for $v_{G,2} = V_{G,2} - V_{G,0} = 0.5$, 1.5, and 4.5 V. (c),(d) $j_{s,1}/j_{s,2}$ at distances $x = 0$, 0.5, and 1 μm as a function of the effective gate voltage $v_{G,1}$ when $v_{G,2}$ is fixed at 0.5 V. The calculations are performed with $\epsilon_G \approx 3.9$ and $t_G = 50$ nm for the dielectric gate.

with shorter SDL [Figs. 2(c) and 3(b)–3(d)]. For example, by calculating the SDLs from the corresponding expression in Table I with $\Delta_{\mathrm{EY}} = 10$ meV (derived from Refs. [54,55]), we obtain $\lambda_{s,1} = 3.4$ μm for $v_{G,1} = 5$ V in branch 1 and $\lambda_{s,2} = 0.6$ μm for $v_{G,2} = 0.5$ V in branch 2. As a result, a considerable ratio of pure spin current dependent on the distance away from the bifurcation can be achieved [e.g., $j_{s,1}/j_{s,2} = 4.5$ for $x = 1$ μm; see Figs. 2(c) and 3(d)]. When x gets closer to or even larger the SDL in branch 1, $j_{s,1}/j_{s,2}$ is even larger, but this is compensated by a severely decayed spin current in both branches.

For BLG with the DP mechanism, appreciable demultiplexing operations can be achieved: the ratio between the pure spin currents can be as large as approximately 7, when the gate voltages are 0.5 and 5 V on the left or right branches [Fig. 2(b)]. This ratio of pure spin current does not depend on the distance from the bifurcation [Figs. 2(d) and 3(e)–3(h)] because the distribution of pure spin current at the bifurcation rather than the decay of pure spin-current propagation in each branch is gate driven. As shown in Fig. 3, this gate-driven distribution feature also avoids unnecessary leakages of pure spin current into the other branch.

Such a gate-driven strategy enables efficient manipulation of pure spin current. The performance of the demultiplexing operation is found to depend on the spin-relaxation mechanism of the graphene channel (Figs. 2 and 3; also see Table I). Graphene channels with the EY mechanism feature a gate-tunable spin-diffusion length, which indicates a gate-driven propagation of pure spin current in the graphene channel. However, a strategy based on the EY mechanism may not be applicable for practical demultiplexing operations considering the fact that there is always approximately 50% leakage of the pure spin current into the other branch at the bifurcation. The channels with the DP mechanism feature a gate-tunable ratio of conductivity and spin-diffusion length, which results in gate-driven distribution of pure spin current at the bifurcation of the device. Compared with the case of SLG with the EY mechanism, a more appreciable performance of pure spin-current demultiplexing can be achieved in the device with the BLG channel dominated by the DP mechanism. Such a strategy, free of unnecessary pure spin-current leakages, can be a good choice for a pure spin demultiplexing operation. The difference in the performance also implies the possibility to distinguish the dominant spin-relaxation mechanism of the graphene channel using a similar device structure, which is a primary objective of graphene spintronics [3,4,14].

Utilizing the superior ability of graphene in pure spin-current transport (with a SDL longer than 10 μm; see Refs. [17,18]), this gate-driven strategy with the efficient spin-current manipulation capability can eliminate frequent spin-charge conversions for the cascade of logic functions, which paves a way for ultra-low-power logic devices. To realize corresponding real applications based on this strategy, there are some limitations and requirements deserving further attention. For example, (i) a spin-charge conversion method with high efficiency is highly desired for the generation and detection of pure spin current [4]; (ii) graphene channels with longer spin-diffusion length allow more gate modulations to be applied between spin-charge conversions and are appealing for real device applications; (iii) the operation speed of the as-developed spin-logic device may be limited by the spin-diffusion

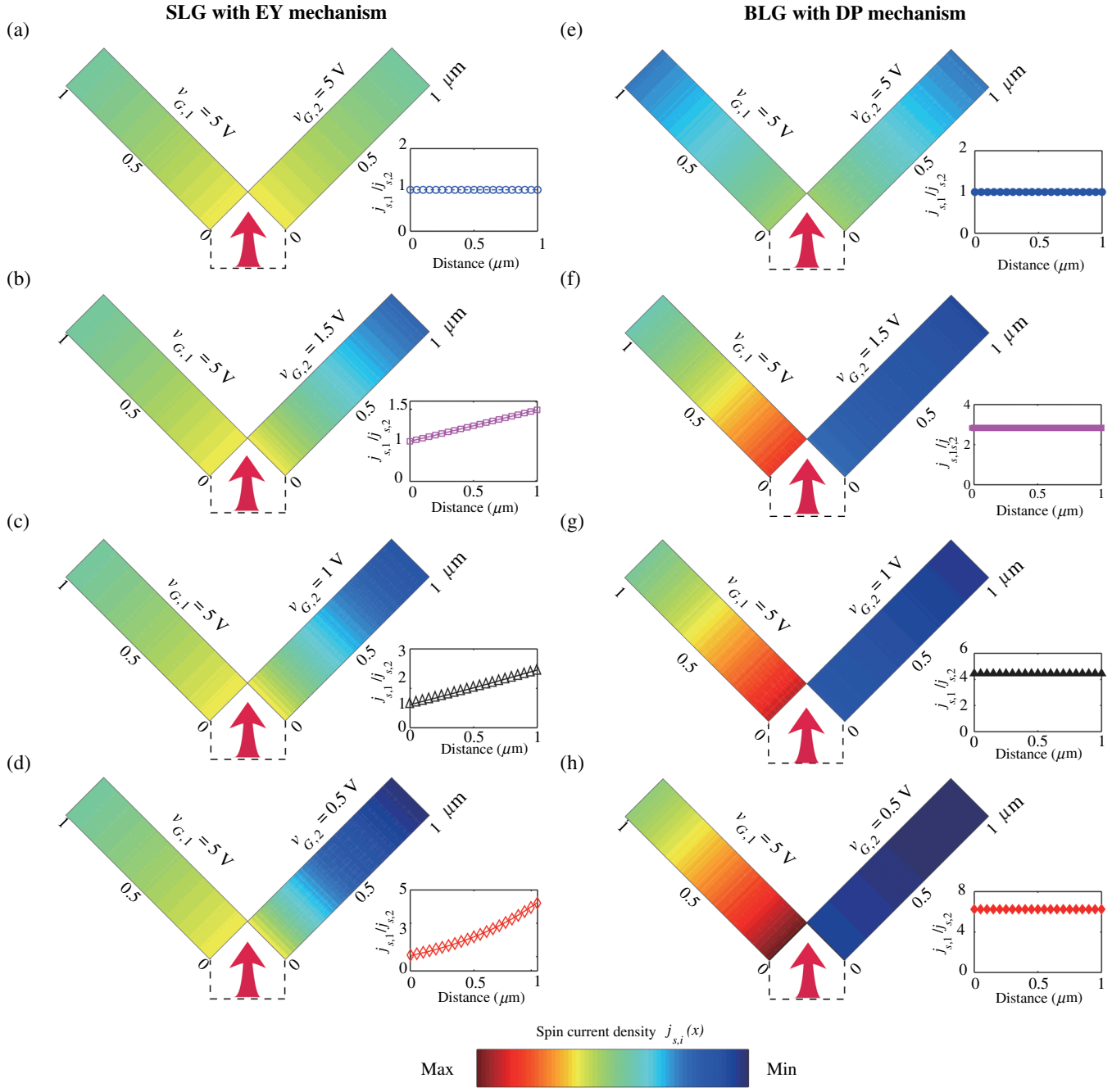

FIG. 3. Performance of the demultiplexing operation in Y-shaped GSDM. Two-dimensional mappings of the pure spin-current distribution at bifurcation ($x = 0$) and the propagation in each branch are plotted. The pure spin-current ratio $j_{s,1}/j_{s,2}$ as a function of distance x is displayed in the inserts. (a)–(d) Pure spin-current demultiplexing of SLG with the EY mechanism at different gate voltages $v_{G,i}$. (e)–(h) Pure spin-current demultiplexing of BLG with the DP mechanism at different gate voltages $v_{G,i}$.

process [56]; (iv) spin-relaxation mechanisms other than the as-considered EY mechanism and DP mechanism may also be applicable for the gate-driven strategy through the gate tuning of the spin-relaxation time [47–51].

IV. CONCLUSION

In summary, we show that gate-driven pure spin current in graphene can be realized utilizing the gate tuning of the conductivity and spin-diffusion length in graphene. We further demonstrate the demultiplexing operation of pure spin current in a Y-shaped graphene spin-current demultiplexer, which can be a fundamental block of spin logic. The performance of the gate-tunable demultiplexing operation is found to depend on the spin-relaxation mechanism of the graphene channel. More appreciable performance can be achieved in the device with a bilayer

graphene channel dominated by a DP spin-relaxation mechanism compared with the case of single-layer graphene with an EY spin-relaxation mechanism. Such a gate-driven strategy enabling efficient spin-current manipulations and eliminating frequent spin-charge conversions for the cascade of logic functions, will pave a way for ultra-low-power spin logic beyond CMOS.

ACKNOWLEDGMENTS

This work is supported by the National Natural Science Foundation of China (Grants No. 61571023, No. 51602013, No. 61627813, and No. 61504006), the International Collaboration 111 Project from the Ministries of Education and Foreign Experts (Grant No. B16001), and Beijing Natural Science Foundation (Grant No. 4162039). This work is also supported by the Innovation Foundation of Beihang University for Ph.D. Graduates. We thank Professor Wei Han, Professor Jianlei Yang, Professor Zhaohao Wang, and Dr. Jun Jiang for helpful discussions.

X. L. and L. S. contributed equally to this work.

[1] C. Chappert, A. Fert, and F. N. Van Dau, The emergence of spin electronics in data storage, Nat. Mater. **6**, 813 (2007).
[2] S. A. Wolf, D. D. Awschalom, R. A. Buhrman, J. M. Daughton, S. Von Molnar, M. L. Roukes, A. Y. Chtchelkanova, and D. M. Treger, Spintronics: A spin-based electronics vision for the future, Science **294**, 1488 (2001).
[3] A. C. Ferrari *et al.*, Science and technology roadmap for graphene, related two-dimensional crystals, and hybrid systems, Nanoscale **7**, 4598 (2015).
[4] S. Roche, J. Åkerman, B. Beschoten, J. Charlier, M. Chshiev, S. Prasad Dash, B. Dlubak, J. Fabian, A. Fert, M. Guimarães, F. Guinea, I. Grigorieva, C. Schönenberger, P. Seneor, C. Stampfer, S. O. Valenzuela, X. Waintal, and B. van Wees, Graphene spintronics: The European Flagship perspective, 2D Mater. **2**, 030202 (2015).
[5] G. Miao, M. Münzenberg, and J. S. Moodera, Tunneling path toward spintronics, Rep. Prog. Phys. **74**, 036501 (2011).
[6] J. C. Slonczewski, Current-driven excitation of magnetic multilayers, J. Magn. Magn. Mater. **159**, L1 (1996).
[7] J. Z. Sun, Spin-current interaction with a monodomain magnetic body: A model study, Phys. Rev. B **62**, 570 (2000).
[8] J. A. Katine, F. J. Albert, R. A. Buhrman, E. B. Myers, and D. C. Ralph, Current-Driven Magnetization Reversal and Spin-Wave Excitations in Co/Cu/Co Pillars, Phys. Rev. Lett. **84**, 3149 (2000).
[9] I. Mihai Miron, G. Gaudin, S. Auffret, B. Rodmacq, A. Schuhl, S. Pizzini, J. Vogel, and P. Gambardella, Current-driven spin torque induced by the Rashba effect in a ferromagnetic metal layer, Nat. Mater. **9**, 230 (2010).
[10] L. Liu, C. F. Pai, Y. Li, H. W. Tseng, D. C. Ralph, and R. A. Buhrman, Spin-torque switching with the giant spin Hall effect of tantalum, Science **336**, 555 (2012).
[11] T. Hanyu, T. Endoh, D. Suzuki, H. Koike, Y. Ma, N. Onizawa, M. Natsui, S. Ikeda, and H. Ohno, Standby-power-free integrated circuits using MTJ-based VLSI computing, Proc. IEEE **104**, 1844 (2016).
[12] F. Schwierz, Graphene transistors, Nat. Nanotechnol. **5**, 487 (2010).
[13] M. Peplow, Graphene: The quest for supercarbon, Nature (London) **503**, 327 (2013).
[14] W. Han, R. K. Kawakami, M. Gmitra, and J. Fabian, Graphene spintronics, Nat. Nanotechnol.. **9**, 794 (2014).
[15] S. Das Sarma, S. Adam, E. H. Hwang, and E. Rossi, Electronic transport in two-dimensional graphene, Rev. Mod. Phys. **83**, 407 (2011).
[16] A. K. Geim and K. S. Novoselov, The rise of graphene, Nat. Mater. **6**, 183 (2007).
[17] M. Drögeler, C. Franzen, F. Volmer, T. Pohlmann, L. Banszerus, M. Wolter, K. Watanabe, T. Taniguchi, C. Stampfer, and B. Beschoten, Spin lifetimes exceeding 12 ns in graphene nonlocal spin valve devices, Nano Lett. **16**, 3533 (2016).
[18] J. Ingla-Aynés, M. H. D. Guimarães, R. J. Meijerink, P. J. Zomer, and B. J. van Wees, 24-μm spin relaxation length in boron nitride encapsulated bilayer graphene, Phys. Rev. B **92**, 201410(R) (2015).
[19] M. V. Kamalakar, C. Groenveld, A. Dankert, and S. P. Dash, Long distance spin communication in chemical vapour deposited graphene, Nat. Commun.. **6**, 6766 (2015).
[20] B. Dlubak, M. Martin, C. Deranlot, B. Servet, S. Xavier, R. Mattana, M. Sprinkle, C. Berger, W. A. De Heer, F. Petroff, A. Anane, P. Seneor, and A. Fert, Highly efficient spin transport in epitaxial graphene on SiC, Nat. Phys.. **8**, 557 (2012).
[21] N. Tombros, C. Jozsa, M. Popinciuc, H. T. Jonkman, and B. J. van Wees, Electronic spin transport and spin precession in single graphene layers at room temperature, Nature (London) **448**, 571 (2007).
[22] S. Cho, Y. Chen, and M. S. Fuhrer, Gate-tunable graphene spin valve, Appl. Phys. Lett. **91**, 123105 (2007).
[23] H. Dery, P. Dalal, Ł. Cywiński, and L. J. Sham, Spin-based logic in semiconductors for reconfigurable large-scale circuits, Nature (London) **447**, 573 (2007).
[24] L. Su, Y. Zhang, J. Klein, Y. Zhang, A. Bournel, A. Fert, and W. Zhao, Current-limiting challenges for all-spin logic devices, Sci. Rep. **5**, 14905 (2015).
[25] B. Behin-Aein, D. Datta, S. Salahuddin, and S. Datta, Proposal for an all-spin logic device with built-in memory, Nat. Nanotechnol. **5**, 266 (2010).
[26] R. J. Elliott, Theory of the effect of spin-orbit coupling on magnetic resonance in some semiconductors, Phys. Rev. **96**, 266 (1954).
[27] M. I. D'yakonov and V. I. Perel, Spin relaxation of conduction electrons in noncentrosymmetric semiconductors, Sov. Phys. Solid State **13**, 3023 (1972).
[28] M. I. D'yakonov and V. I. Perel, Possibility of orienting electron spins with current, Sov. JETP Lett. **13**, 467 (1971).
[29] J. C. R. Sánchez, L. Vila, G. Desfonds, S. Gambarelli, J. P. Attané, J. M. De Teresa, C. Magén, and A. Fert, Spin-to-charge conversion using Rashba coupling at the interface between non-magnetic materials, Nat. Commun. **4**, 2944 (2013).

[30] J. Sinova, S. O. Valenzuela, J. Wunderlich, C. H. Back, and T. Jungwirth, Spin Hall effects, Rev. Mod. Phys. **87**, 1213 (2015).
[31] Z. Tang, E. Shikoh, H. Ago, K. Kawahara, Y. Ando, T. Shinjo, and M. Shiraishi, Dynamically generated pure spin current in single-layer graphene, Phys. Rev. B **87**, 140401 (2013).
[32] A. K. Patra, S. Singh, B. Barin, Y. Lee, J. H. Ahn, E. Del Barco, E. R. Mucciolo, and B. Özyilmaz, Dynamic spin injection into chemical vapor deposited graphene, Appl. Phys. Lett. **101**, 162407 (2012).
[33] I. Žutić, J. Fabian, and S. Das Sarma, Spintronics: Fundamentals and applications, Rev. Mod. Phys. **76**, 323 (2004).
[34] S. Takahashi and S. Maekawa, Spin injection and detection in magnetic nanostructures, Phys. Rev. B **67**, 052409 (2003).
[35] See Supplemental Material at http://link.aps.org/supplemental/10.1103/PhysRevApplied.8.034006 for details of the derivation and the reconfigurable spin-logic circuit based on gate-driven pure spin current in graphene.
[36] D. E. Nikonov and I. A. Young, Overview of beyond-CMOS devices and a uniform methodology for their benchmarking, Proc. IEEE **101**, 2498 (2013).
[37] J. Kim, A. Paul, P. A. Crowell, S. J. Koester, S. S. Sapatnekar, J. Wang, and C. H. Kim, Spin-based computing: Device concepts, current status, and a case study on a high-performance microprocessor, Proc. IEEE **103**, 106 (2015).
[38] C. Mead, Neuromorphic electronic systems, Proc. IEEE **78**, 1629 (1990).
[39] J. H. Chen, C. Jang, S. Adam, M. S. Fuhrer, E. D. Williams, and M. Ishigami, Charged-impurity scattering in graphene, Nat. Phys. **4**, 377 (2008).
[40] Y. W. Tan, Y. Zhang, K. Bolotin, Y. Zhao, S. Adam, E. H. Hwang, S. Das Sarma, H. L. Stormer, and P. Kim, Measurement of Scattering Rate and Minimum Conductivity in Graphene, Phys. Rev. Lett. **99**, 246803 (2007).
[41] B. E. Feldman, J. Martin, and A. Yacoby, Broken-symmetry states and divergent resistance in suspended bilayer graphene, Nat. Phys. **5**, 889 (2009).
[42] M. Drögeler, F. Volmer, M. Wolter, B. Terrés, K. Watanabe, T. Taniguchi, G. Güntherodt, C. Stampfer, and B. Beschoten, Nanosecond spin lifetimes in single- and few-layer graphene-hBN heterostructures at room temperature, Nano Lett. **14**, 6050 (2014).
[43] W. Han and R. K. Kawakami, Spin Relaxation in Single-Layer and Bilayer Graphene, Phys. Rev. Lett. **107**, 047207 (2011).
[44] N. Tombros, S. Tanabe, A. Veligura, C. Jozsa, M. Popinciuc, H. T. Jonkman, and B. J. van Wees, Anisotropic Spin Relaxation in Graphene, Phys. Rev. Lett. **101**, 046601 (2008).
[45] T. Y. Yang, J. Balakrishnan, F. Volmer, A. Avsar, M. Jaiswal, J. Samm, S. R. Ali, A. Pachoud, M. Zeng, M. Popinciuc, G. Güntherodt, B. Beschoten, and B. Özyilmaz, Observation of Long Spin-Relaxation Times in Bilayer Graphene at Room Temperature, Phys. Rev. Lett. **107**, 047206 (2011).
[46] B. Raes, A. W. Cummings, F. Bonell, M. V. Costache, J. F. Sierra, S. Roche, and S. O. Valenzuela, Spin precession in anisotropic media, Phys. Rev. B **95**, 085403 (2017).
[47] A. Avsar, I. J. Vera-Marun, J. Y. Tan, G. K. W. Koon, K. Watanabe, T. Taniguchi, S. Adam, and B. Özyilmaz, Electronic spin transport in dual-gated bilayer graphene, NPG Asia Mater. **8**, e274 (2016).
[48] B. Raes, J. E. Scheerder, M. V. Costache, F. Bonell, J. F. Sierra, J. Cuppens, J. Van de Vondel, and S. O. Valenzuela, Determination of the spin-lifetime anisotropy in graphene using oblique spin precession, Nat. Commun. **7**, 11444 (2016).
[49] D. Kochan, M. Gmitra, and J. Fabian, Spin Relaxation Mechanism in Graphene: Resonant Scattering by Magnetic Impurities, Phys. Rev. Lett. **112**, 116602 (2014).
[50] D. Kochan, S. Irmer, M. Gmitra, and J. Fabian, Resonant Scattering by Magnetic Impurities as a Model for Spin Relaxation in Bilayer Graphene, Phys. Rev. Lett. **115**, 196601 (2015).
[51] D. V. Tuan, F. Ortmann, D. Soriano, S. O. Valenzuela, and S. Roche, Pseudospin-driven spin relaxation mechanism in graphene, Nat. Phys. **10**, 857 (2014).
[52] D. Huertas-Hernando, F. Guinea, and A. Brataas, Spin-Orbit-Mediated Spin Relaxation in Graphene, Phys. Rev. Lett. **103**, 146801 (2009).
[53] P. Zhang and M. W. Wu, Electron spin relaxation in graphene with random Rashba field: Comparison of the D'yakonov-Perel' and Elliott-Yafet-like mechanisms, New J. Phys. **14**, 033015 (2012).
[54] P. J. Zomer, M. H. D. Guimarães, N. Tombros, and B. J. van Wees, Long-distance spin transport in high-mobility graphene on hexagonal boron nitride, Phys. Rev. B **86**, 161416(R) (2012).
[55] S. Jo, D. Ki, D. Jeong, H. Lee, and S. Kettemann, Spin relaxation properties in graphene due to its linear dispersion, Phys. Rev. B **84**, 075453 (2011).
[56] J. Ingla-Aynés, R. J. Meijerink, and B. J. van Wees, Eighty-eight percent directional guiding of spin currents with 90 μm relaxation length in bilayer graphene using carrier drift, Nano Lett. **16**, 4825 (2016).