Nonvolatile Multilevel Memory and Boolean Logic Gates Based on a Single $Ni/[Pb(Mg_{1/3}Nb_{2/3})O_3]_{0.7}[PbTiO_3]_{0.3}/Ni$ Heterostructure

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Memtranstor that correlates charge and magnetic flux via nonlinear magnetoelectric effects has a great potential in developing next-generation nonvolatile devices. In addition to multilevel nonvolatile memory, we demonstrate here that nonvolatile logic gates such as NOR and NAND can be implemented in a single memtranstor made of the Ni/PMN-PT/Ni heterostructure. After applying two sequent voltage pulses (X_1, X_2) as the logic inputs on the memtranstor, the output magnetoelectric voltage can be positive high (logic 1), positive low (logic 0), or negative (logic 0), depending on the levels of X_1 and X_2. The underlying physical mechanism is related to the complete or partial reversal of ferroelectric polarization controlled by inputting selective voltage pulses, which determines the magnitude and sign of the magnetoelectric voltage coefficient. The combined functions of both memory and logic could enable the memtranstor as a promising candidate for future computing systems beyond von Neumann architecture.

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I. INTRODUCTION

In electric circuit theory, the three well-known fundamental elements (resistor, capacitor, and inductor) are defined from the linear relationship between two of the four basic circuit variables (charge q, current i, voltage v, and magnetic flux φ), as schematically illustrated in Fig. 1(a). The fourth fundamental linear element that is defined directly from the q-φ relationship has been under debate for many years [1–4]. As Mathur noted and we demonstrate explicitly, the fourth element can be realized by employing the magnetoelectric (ME) effects [2,4,5], i.e., magnetic field control of electric polarization (P) and electric field control of magnetization (M) [6–9], because a direct relationship between q and φ is built up in a simple two-terminal passive device via the ME coupling, as illustrated in Fig. 1(b). The fourth fundamental element based on the ME effects is termed transtor. Corresponding to the linear elements, there are four nonlinear memelements [10], namely, memristor, memcapacitor, meminductor, and memtranstor. These memelements provide a great potential to broaden electric circuit functionality for next-generation electronic devices. For instance, the memristor is attracting tremendous interest because of its substantial technological applications [11–18]. Similarly, the memtranstor also has great promise in the development of advanced electronic devices.

The memtranstor is characterized by nonlinear hysteresis loops shown in Figs. 1(c) and 1(d). Either the butterfly-shaped or the pinched hysteresis loops, depending on the magnitude of external stimulus, provide the basis of a concept of nonvolatile memory. The principle is to utilize the different states of transtance $T = dq/d\varphi$, or equivalently, the ME voltage coefficient $\alpha_E = dE/dH$, varying from positive to negative [Fig. 1(c)] or high to low [Fig. 1(d)], to store binary information. In our recent works [19,20], both two-level and multilevel nonvolatile memory devices have been demonstrated based on the PMN-PT/Terfenol-D memtranstor. In this work, we show that the functionality of the memtranstor can be further exploited to implement nonvolatile logic gates.

II. EXPERIMENTS

The memtranstor used in this study is made of the $Ni/0.7Pb(Mg_{1/3}Nb_{2/3})O_3$-$0.3PbTiO_3$ (PMN-PT)/Ni heterostructure with in-plane M and out-of-plane P, as illustrated in Fig. 2(a). In this kind of multiferroic heterostructure, the ME coupling is mainly due to the interfacial strain between magnetic and ferroelectric layers. Therefore, materials with large magnetoelastic and piezoelectric effects are preferred to make the ME devices. Here, we use PMN-PT as the ferroelectric layer because of its large piezoelectric coefficient. Although its magnetostrictive coefficient is relatively lower than typical magnetostrictive alloys such as Terfenol-D or metglass, we select the simple metal Ni in this study because it is cheap and easy to fabricate—qualities which are in favor of commercial applications. As high-quality PMN-PT films are not available to us, we use single crystals of PMN-PT (110) with a thickness of 200 μm instead. The multiferroic heterostructure is prepared by magneton sputtering two Ni layers

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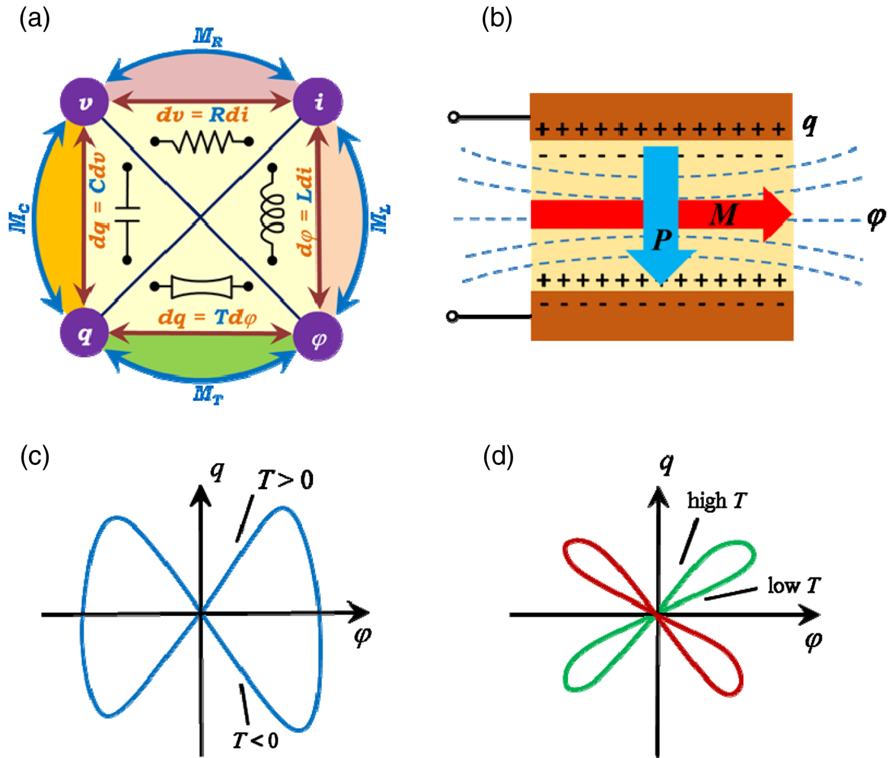


FIG. 1. The Principle of the memtranstor. (a) The full diagram of fundamental circuit elements. The four linear elements (resistor, capacitor, inductor, and transtor) are defined by the linear relationships between two of four basic variables (v, i, q, φ), respectively. The four memelements (memristor, memcapacitor, meminductor, and memtranstor) are defined by the nonlinear relationships between two variables, respectively. (b) The typical structure of a memtranstor. The q-φ relationship is realized via the ME coupling between magnetization (M) and polarization (P). (c),(d) The characteristics of memtranstors. Either butterfly-shaped or pinched hysteresis loops can be observed, depending on the magnitude of external stimulus. The different states of transtance, $T = dq/d\varphi$, or equivalently, the ME voltage coefficient $\alpha_E = dE/dH$, ranging from positive to negative and high to low, are used to implement both nonvolatile memory and logic functions.

on the surfaces of the PMN-PT (110) crystal. In this way, the top and bottom Ni layers act as not only the magnetic components of the memtranstor but also the electrodes. Each Ni layer is 1 μm in thickness.

A conventional dynamic technique is employed to measure the ME voltage coefficient (α_E). A Keithley 6221 ac source is used to supply an ac current to a solenoid to generate a small ac magnetic field h_{ac} at a frequency of 10 kHz. In response, a synchronized 10-kHz ac ME voltage, $V_{ac} = x + yi$, across the electrodes is measured by a lock-in amplifier (Stanford Research SR830). The ME voltage coefficient α_E is calculated by $\alpha_E = x/(h_{ac}t)$,

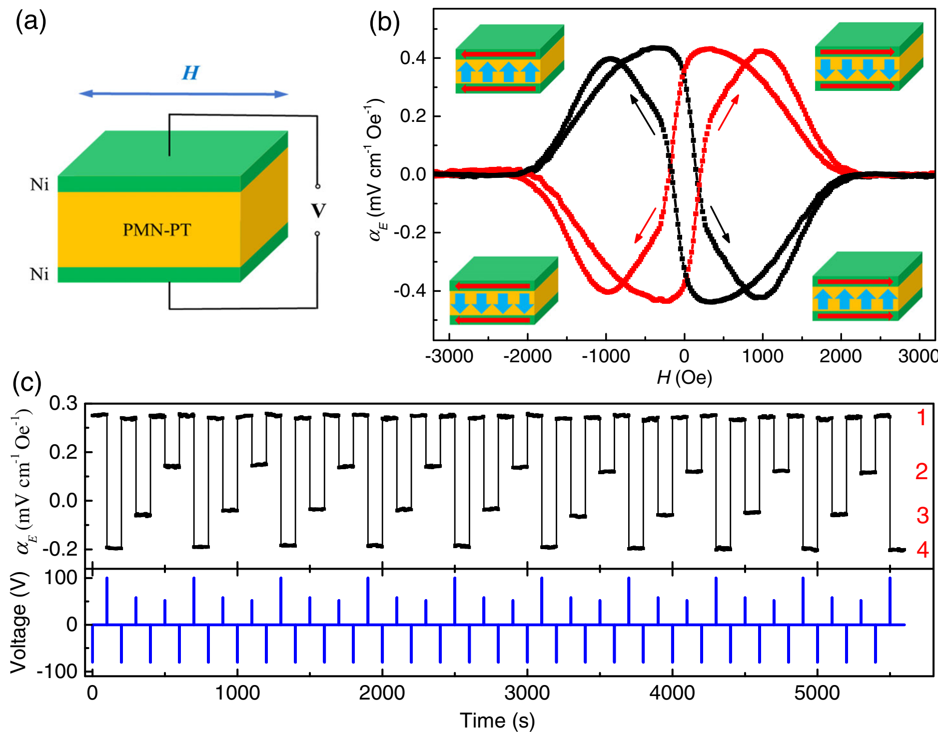


FIG. 2. Multilevel nonvolatile memory based on the Ni/PMN-PT/Ni memtranstor. (a) The structure of the device and the measurement configuration. Two layers of Ni are deposited on the surfaces of the PMN-PT(110) single crystal. The electric field is applied vertically to switch the ferroelectric domains and the magnetic field is applied in plane to control magnetic domains. (b) The ME voltage coefficient α_E as a function of dc magnetic field with the PMN-PT layer prepoled to $+P_s$ and $-P_s$, respectively. The states of α_E depend on the relative orientation between magnetic and ferroelectric domains. The large hysteresis with a high remnant α_E at zero dc bias is beneficial for practical applications. (c) Repeatable multilevel switch of α_E by applying selective voltage pulses (−80, 100, 58, and 52 V), in the zero-dc-bias magnetic field. After each voltage pulse (10 ms) α_E is measured for 100 s.

where t is the thickness of the ferroelectric layer (200 μm). To switch or prepole the electric polarization of PMN-PT, a Keithley 6517B electrometer is used to apply voltage pulse across the electrodes. The device is loaded in an Oxford TeslatronPT superconducting magnet system to apply the dc-bias magnetic field (H_{dc}). All the measurements are performed at room temperature.

III. RESULTS AND DISCUSSION

Figure 2(b) shows the ME voltage coefficient α_E of the Ni/PMN-PT/Ni memtranstor as a function of in-plane dc magnetic field. Before measuring α_E, the memtranstor is prepoled to set the direction of saturation polarization P_s pointing upward or downward. The magnitude and sign of α_E depend on the relative orientation between magnetic and ferroelectric domains: when the direction of P_s is fixed, α_E can be controlled by reversing magnetic domains with in-plane magnetic field; when the magnetic domains remain unchanged, the states of α_E can be controlled by fully or partially reversing ferroelectric domains with vertical electric fields. The latter case is employed to implement both nonvolatile memory and logic functions.

Compared with that of the PMN-PT/Terfenol-*D* memtranstor [19], α_E of the Ni/PMN-PT/Ni memtranstor exhibits a broader hysteresis loop and a higher remanence at zero bias field. These features are favorable for practical applications because no dc-bias magnetic field is required. As seen in Fig. 2(c), the states of α_E can be well controlled by applying selective voltage pulses (−80, 100, 58, and 52 V) to fully or partially reverse ferroelectric domains. Consequently, four clearly separated states of α_E ranging from positive to negative are obtained repeatedly for many cycles, demonstrating a multilevel nonvolatile memory based on the Ni/PMN-PT/Ni memtranstor. As we discussed in our previous papers [19,20], the nonvolatile memory based on the memtranstors retains all the advantages of ferroelectric memory (simple structure, fast speed, low power consumption), but overcomes the drawback of the destructive reading of P. In contrast, the readout of α_E (or simply the ME voltage) is nondestructive and highly efficient in a parallel mode.

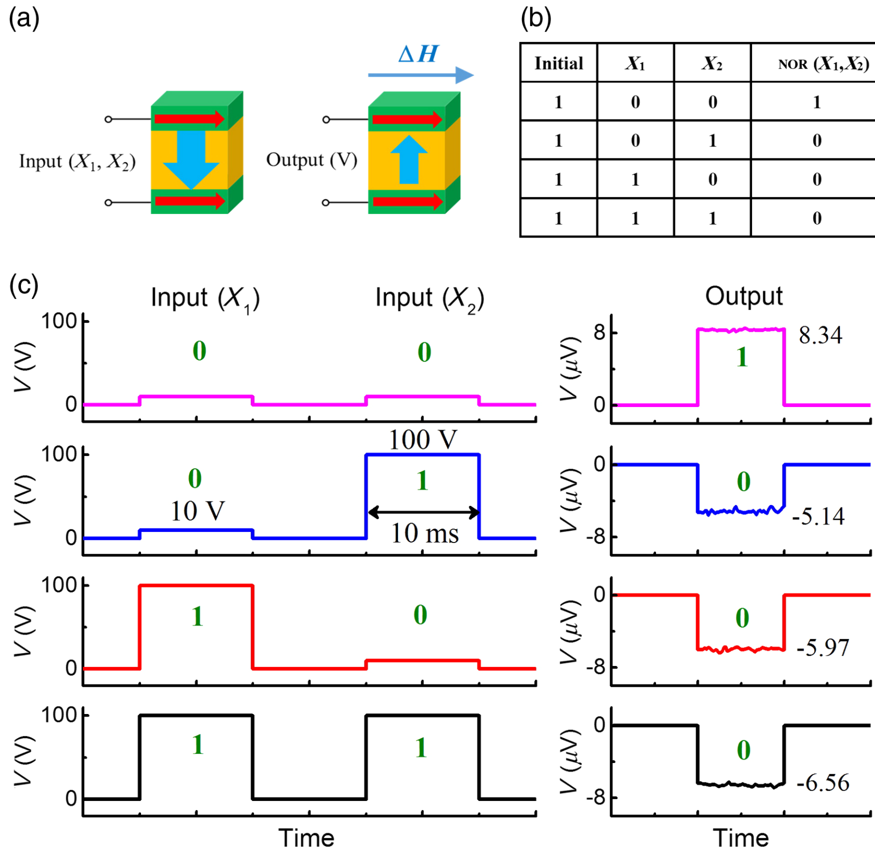
Furthermore, the memtranstor also provides the opportunity to build up novel computing systems beyond classical von Neumann architecture. In the past decade, many efforts have been devoted to developing future computing systems with logic-in-memory architecture where memory and logic gates are tightly integrated. Various nonvolatile devices including memristors, magnetic tunneling junctions, phase-change memories, *etc.*, have been employed to implement nonvolatile logic functions [21–27]. In the following, we propose and demonstrate that the memtranstor also has the potential to implement nonvolatile logic gates.

Figures 3(a)–3(c) illustrate how to implement the NOR logic function using a single memtranstor. NOR is a universal Boolean logic function of two binary inputs, where the output is always logic 0, except for the inputs being both logic 0, in which case the output is logic 1. The logic operation is accomplished by three stages: initialization, computation, and readout. First, the initializing operation prepares the memtranstor in the positive high α_E state. Then, the computing stage consists of inputting a sequence of two voltage pulses X_1 and X_2, carrying the input logic signals. The input voltage pulses with high and low magnitude are defined as logic 1 and logic 0, respectively. Last, the computation is read out by applying a small magnetic field to generate the output voltage via the ME effect, $\alpha_E = (dE/dH) = (1/t)(dV/dH)$, where t is the thickness of the ferroelectric layer.

As shown in Fig. 3(c), the experimental results obtained on the Ni/PMN-PT/Ni memtranstor confirm the NOR logic function. For X_1 and X_2 being both low, no change occurs in the memtranstor because the low inputs (10 V) do not alter the ferroelectric domains. Thus, α_E remains positive high, i.e., the output ME voltage is positive high. When either X_1 or X_2 are high, the majority of ferroelectric domains are reversed by the high input (100 V) so that α_E becomes negative. When both X_1 and X_2 are high, the ferroelectric domains are nearly fully reversed and α_E becomes negative high. In this case, we can define the positive and negative output ME voltage as logic 1 and logic 0, respectively, and the computations fulfill the truth table of the NOR logic [Fig. 3(b)].

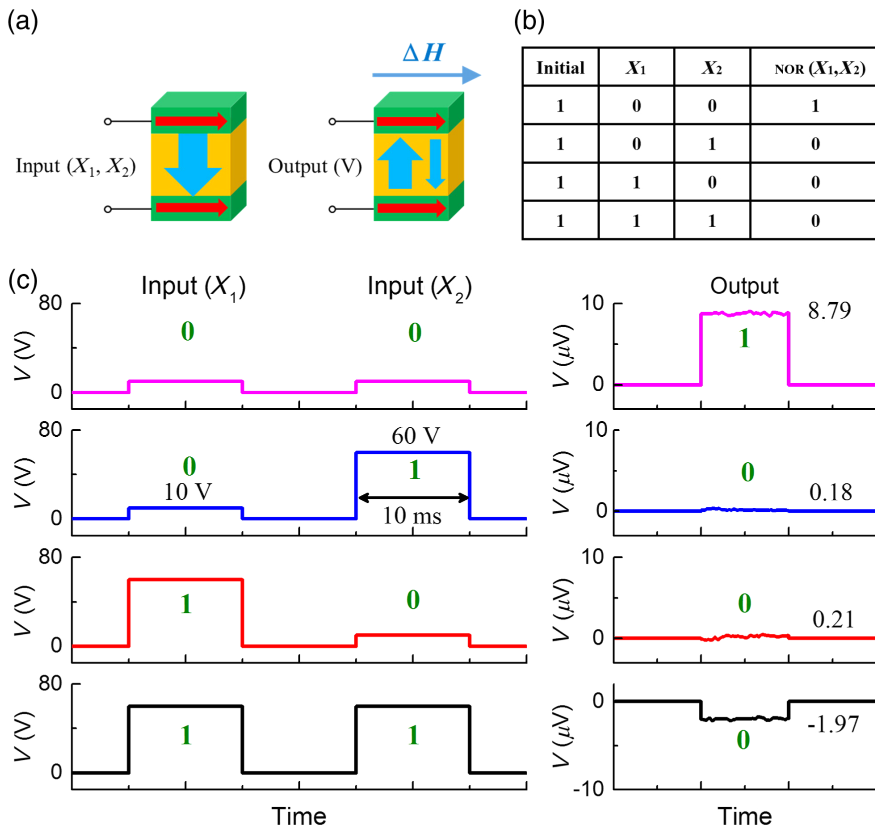
Alternatively, the NOR logic can be implemented by another mode with lower input voltages. As shown in Fig. 4, after initialization, when both X_1 and X_2 are low (10 V), the output ME voltage remains positive high because no change occurs in the memtranstor. When one of X_1 and X_2 is high (60 V), a large proportion of ferroelectric domains are reversed so that α_E is reduced from positive high to positive low. When both X_1 and X_2 are high (60 V), the majority of ferroelectric domains are reversed and α_E becomes negative. In this scenario, the high output ME voltage is defined as logic 1, and the low or negative output ME voltage is defined as logic 0.

In addition, we demonstrate the NAND logic function based on a single memtranstor. NAND is another universal Boolean logic function of two binary inputs, where the output is always logic 1, except for the inputs being both logic 1, in which case the output is logic 0. The principle and experimental results are shown in Fig. 5. After initialization, two sequent voltage pulses X_1 and X_2 are inputted into the device to do the computation. The low input (10 V) is set as logic 0 and the high input (58 V) as logic 1. The output positive ME voltage is set as logic 1 and negative as logic 0. Inputting low voltage does not alter the ferroelectric domains so that the output ME voltage remains positive high (logic 1). Inputting a single 58 V partially reverses the ferroelectric domains so that the output ME voltage reduces but still retains positive voltage (logic 1). Only after



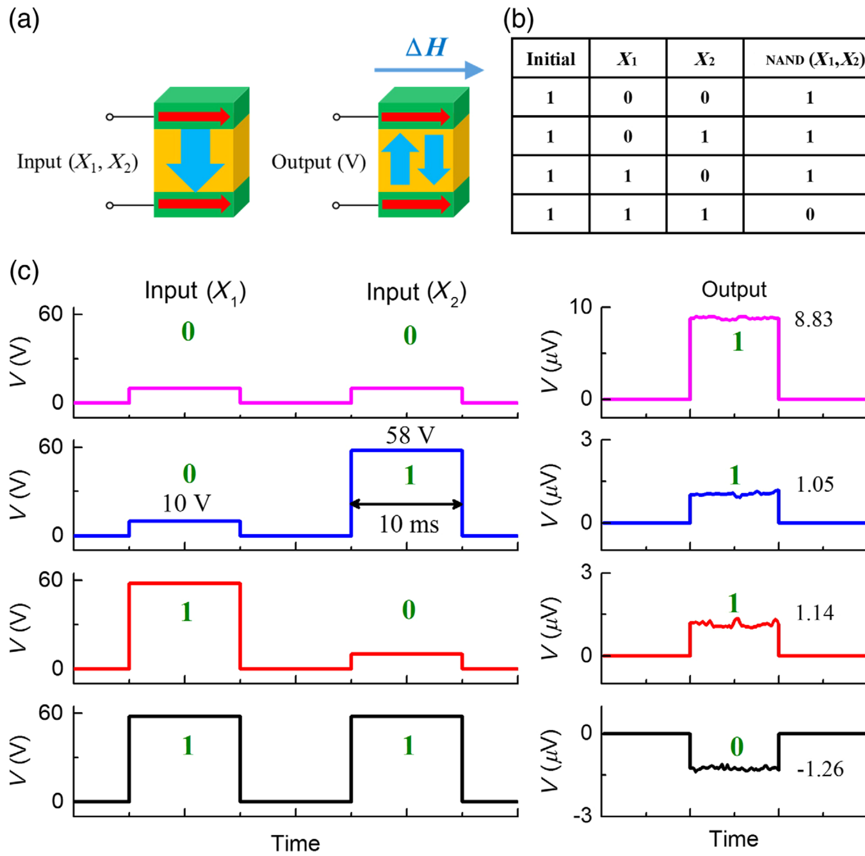
Initial	X_1	X_2	NOR (X_1,X_2)
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

FIG. 3. Nonvolatile NOR logic based on a single memtranstor—the first mode. (a) The schematic of the device structure and operations. After initialization, two sequent voltage pulses X_1 and X_2 are inputted into the device to do the computation. The low input (10 V) is set as logic 0 and the high input (100 V) as logic 1. The result is read out by applying a small in-plane magnetic field (ΔH) to generate the output voltage via the ME effect. (b) The truth table of NOR operation. (c) Experimental results obtained on the Ni/PMN-PT/Ni memtranstor demonstrating the NOR operation. The output positive ME voltage is set as logic 1 and negative as logic 0. Inputting logic 0 does not alter the ferroelectric domains so that the output ME voltage remains positive high. Inputting logic 1 fully reverses the ferroelectric domains so that the output ME voltage becomes negative.



Initial	X_1	X_2	NOR (X_1,X_2)
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

FIG. 4. Nonvolatile NOR logic based on a single memtranstor—the second mode. (a) The schematic of the device structure and logic operations. After initialization, two sequent voltage pulses X_1 and X_2 are inputted into the device to do the computation. The low input (10 V) is set as logic 0 and the high input (60 V) as logic 1. The result is read out by applying a small in-plane magnetic field (ΔH) to generate the output voltage via the ME effect. (b) The truth table of NOR operation. (c) Experimental results obtained on the Ni/PMN-PT/Ni memtranstor demonstrating the NOR operation. The output high ME voltage is set as logic 1 and low or negative as logic 0. Inputting logic 0 does not alter the ferroelectric domains so that the output ME voltage remains positive high. Inputting logic 1 partially reverses the ferroelectric domains so that the output ME voltage becomes low.



Initial	X_1	X_2	NAND (X_1,X_2)
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

FIG. 5. Nonvolatile NAND logic based on a single memtranstor. (a) The schematic of the device structure and logic operations. After initialization, two sequent voltage pulses X_1 and X_2 are inputted into the device to do the computation. The low input (10 V) is set as logic 0 and the high input (58 V) as logic 1. (b) The truth table of NAND operation. (c) Experimental results obtained on the Ni/PMN-PT/Ni memtranstor demonstrating the NAND operation. The output positive ME voltage is set as logic 1 and negative as logic 0. Inputting logic 0 does not alter the ferroelectric domains so that the output ME voltage remains positive high. Inputting a single logic 1 partially reverses the ferroelectric domains so that the output ME voltage reduces but still retains positive voltage. Only after inputting two logic 1s, the majority of ferroelectric domains are reversed so that the output ME voltage becomes negative.

inputting two high voltages (58 V), the majority of ferroelectric domains are reversed so that the output ME voltage becomes negative (logic 0). In this way, the computations fulfill the true table of the NAND logic [Fig. 5(b)].

The above experimental results successfully demonstrate that nonvolatile logic gates such as NOR and NAND can be implemented by using a single memtranstor. As NOR and NAND are universal logic gates, other logic functions can be realized based on them. Compared with conventional CMOS logic gates, the logic operations in the memtranstors are quite different. First, the memtranstor-based logic gates are nonvolatile, whereas the CMOS logic gates are volatile. Nonvolatile behavior could greatly suppress the static power dissipation, which is a key concern in CMOS logic due to the subthreshold leakage of transistors. The second difference is the sequential operation in the memtranstor logic, instead of the usually parallel operation in CMOS where one or more inputs are applied to a logic gate within the same clock pulse. Sequential operation is also adopted in several memristor-based logic devices [17,23,24,26,27]. Though sequential operation may take a longer time to complete a single logic operation, on the other hand, it is balanced by a significant reduction of occupied area, namely, a single memtranstor as opposed to two or more CMOS transistors. Just like the memristors that could enable memory and computing integrated on the same chip to reduce interconnect delays due to the transfer of data from the memory circuit to the logic circuit, the memtranstor employing the nonlinear ME effects opens another promising way toward the logic-in-memory computing system. It is worthy to note that there have been diverse proposals of logic gates based on the ME effects [28–30], where the logic functions are usually based on the resistance state controlled by external fields. We employ the states of the ME coefficient (or transtance) to do logic and memory. This strategy is more efficient in reducing power consumption because the resistor is more energy dissipating than the highly insulating transtor.

IV. CONCLUSIONS

The memtranstor that directly correlates charge and magnetic flux via the nonlinear ME effects is considered as the fourth memelement in addition to memristor, memcapacitor, and meminductor. It provides another promising candidate for developing nonvolatile devices. In this work, both multilevel nonvolatile memory and nonvolatile logic gates have been successfully demonstrated based on a single memtranstor made of the Ni/PMN-PT/Ni heterostructure. The combined functions of both memory and logic could enable the memtranstor as elements for computing systems beyond von Neumann architecture.

In practical applications, high-quality ferroelectric films are required to make the sandwich structure in order to miniaturize the device, reduce the operation voltage, as well as release the clamping effect of substrates. Moreover, to optimize the ME coefficient in the heterostructure, the

thickness of magnetic layers should be comparable with that of the ferroelectric layer. To improve the speed of reading, a pulse magnetic field instead of ac magnetic field could be applied through an independent coil. Meanwhile, all the memory and logic cells can share a single read coil [19,20], called parallel reading or output. In the future, the potential of the memtranstor employing the nonlinear ME effects in generating advanced electronic devices deserves an extensive study.

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