Bandlike Transport in Ferroelectric-Based Organic Field-Effect Transistors

A. Laudari and S. Guha*

Department of Physics and Astronomy, University of Missouri, Columbia, Missouri 65211, USA

(Received 10 March 2016; revised manuscript received 15 July 2016; published 17 October 2016)

The dielectric constant of polymer-ferroelectric dielectrics may be tuned by changing the temperature, offering a platform for monitoring changes in interfacial transport with the polarization strength in organic field-effect transistors (FETs). Temperature-dependent transport studies of FETs are carried out from a solution-processed organic semiconductor, 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene), using both ferroelectric- and nonferroelectric-gate insulators. Nonferroelectric dielectric-based TIPS-pentacene FETs show a clear activated transport, in contrast to the ferroelectric dielectric polymer, poly (vinylidene fluoride-trifluoroethylene), where a negative temperature coefficient of the mobility is observed in the ferroelectric temperature range. The current-voltage (I-V) characteristics from TIPS-pentacene diodes signal a space-charge-limited conduction (SCLC) for a discrete set of trap levels, suggesting that charge injection and transport occurs through regions of ordering in the semiconductor. The carrier mobility extracted from temperature-dependent I-V characteristics from the trap-free SCLC region shows a negative coefficient beyond 200 K, similar to the trend observed in FETs with the ferroelectric dielectric. At moderate temperatures, the polarization-fluctuation-dominant transport inherent in a ferroelectric dielectric, in conjunction with the nature of traps, results in an effective detrapping of the shallow-trap states into more mobile states in TIPS-pentacene.

DOI: 10.1103/PhysRevApplied.6.044007

I. INTRODUCTION

The general mechanism of transport in organic field-effect transistors (FETs) constituting molecular or polymeric semiconductors has mainly been addressed within the framework of hopping between disordered-localized states. The process, however, is more complex since there are several competing factors that result in extended band states in organic semiconductors, and factors that result in localized states such as the off-diagonal thermal disorder [1]. Electronic-polarization effects—short- and long-range lattice fluctuations—play an inherent role in FET transport. The polaronic nature of the charge carriers is heavily masked by disorder effects; both local and nonlocal forms of electron-phonon coupling are required for a comprehensive theoretical model [2]. In single-crystal organic FETs such as rubrene, the disorder is significantly reduced, enabling the realization of intrinsic polaronic transport, including the observation of the Hall effect in the accumulation layer [3]. The Hall voltage is a sensitive probe that measures the extent of delocalized adiabatic transport. The presence of the normal Hall effect in organic FETs is, therefore, a signature that the surface charge is similar to a two-dimensional hole or an electron-gas system rather than a hopping of carriers [4].

There have been several recent works that show bandlike transport, characterized by negative coefficient of the charge-carrier mobility (μ) with respect to temperature (T) ($d\mu/dT < 0$), in solution-processable small-molecule- and polymer-based FETs. In 6,13-bis (triisopropylsilylethynyl)pentacene (TIPS-pentacene), a negative coefficient of the carrier mobility at high electric fields was attributed to localized transport limited by thermal-lattice fluctuation [5]. In a few acene-based solution-processable small-molecule FETs, charge delocalization induced by the dynamic disorder as a function of temperature has been probed by charge-modulation spectroscopy, shedding light on the nature of shallow traps [6]. By incorporating large thermal-lattice fluctuations with weak van der Waals intermolecular bonding, theoretical models have explained the bandlike motion observed at high temperatures from highly conducting organic semiconductors [1]. In such materials, the carriers diffuse incoherently in the presence of the large thermal fluctuations, resulting in a weakly metallic behavior. Bandlike transport in TIPS-pentacene FETs has also been observed by time-resolved optical second-harmonic-generation imaging [7].

In high-mobility donor-acceptor-type diketopyrrolopyrrole (DPP) conjugated polymers, a low degree of disorder and a negative coefficient of the carrier mobility (with respect to temperature) were found to be consistent with Hall-voltage measurements [8]. A benzotriazole-based DPP system exhibits a bandlike temperature dependence of the FET mobility when transport is, preferably, along the polymer-chain-alignment direction [9]. In benzothiadiazole-copolymer-based FETs, charge-transport properties have been shown to approach disorder-free limits where all molecular sites are accessible [10].

*guhas@missouri.edu

 © 2016 American Physical Society

The low degree of disorder, a much-wanted feature in polymeric semiconductors, is a combination of the coplanar structure supporting wave-function delocalization and other macroscopic attributes of the material. A common feature for $d\mu/dT < 0$ to occur beyond a certain temperature, as seen across a variety of organic semiconductors, is that the FET carrier mobility should be larger than $\mu_{\min} = er^2/2\hbar$, where r is the intermolecular distance, e is the electronic charge, and $\hbar$ is the Planck's constant [11]. Typically, this condition translates to FET mobilities being greater than 1 to 2 $\mathrm{cm}^2/\mathrm{V\,s}$, ensuring that the energy bandwidth is larger than the energy change involved in the scattering. Recently, ac Hall effect measurements have shed light on the coexistence of both bandlike and hopping charge carriers in the accumulation region of organic FETs. Because of this mixed transport regime, even when FET carrier mobilities are less than 1 $\mathrm{cm}^2/\mathrm{V\,s}$, a Hall voltage is measurable [12,13]. We later show that the coexistence of bandlike and hopping carriers may be attributed to the nature of the shallow traps—discrete traps or a distribution of trap energies.

At this point, it may be prudent to point out that bandlike transport in molecular semiconductors, which mainly occurs in narrow bands, is somewhat different from true band transport, where the latter occurs through extended states in perfect crystals. In pure organic crystals such as naphthalene, band transport for electrons was observed below 150 K [14]. Subsequently, first-principles calculations involving inter- and intramolecular vibrations and electron-phonon coupling constants (both local and nonlocal) have shed light into the band-to-hopping transition in naphthalene as a function of temperature [15]. This transition can be understood on the basis of a localization of charge carriers in the absence of any thermal disorder. Furthermore, at the transition where the charge may be more delocalized, raising the temperature destroys the translational symmetry and reduces the charge transport efficiency, and thus its mobility [16]. The apparent bandlike transport observed as $d\mu/dT < 0$ in organic and polymeric FETs may be mediated by extrinsic mechanisms. As we see in this work, depending on the nature of the dielectric used, a negative or a positive coefficient of μ with respect to temperature is observed in TIPS-pentacene FETs, and this behavior is further correlated to the nature of the shallow traps.

The semiconductor-dielectric interface plays a major role in dictating the transport properties in FETs. One aspect in FET transport arises from polarization fluctuations, especially when polar dielectrics are used. The dynamic coupling of charge carriers to the electronic polarization at the semiconductor-dielectric interface arises mainly from two effects: the image force due to the polarization discontinuity at the interface and the Coulomb interaction of the charge carriers with the surface phonons of the dielectric [17,18]. It has been shown that Fröhlich surface polarons are formed if the gate dielectric is sufficiently polar in molecular systems [19]. The Fröhlich polarons arise due to a long-range interaction between the charge carriers and the longitudinal-optical phonons [20]. These interactions result in a renormalization of the transfer integral and decrease the charge-carrier mobility.

Ferroelectric dielectrics, permitting access to nearly an order of magnitude range of dielectric constants with temperature as the tuning parameter, offer a neat platform to monitor the changes in interfacial transport in organic FETs as the polarization strength is tuned. Temperature-dependent transport studies from pentacene FETs using the ferroelectric copolymer poly(vinylidene fluoride-co-trifluoroethylene) (PVDF-TrFE) showed a suppressed hole mobility in the ferroelectric phase of the dielectric [21]; similar characteristics were also observed in poly(3-hexylthiophene) (P3HT) and PVDF-TrFE FETs [22].

In this work, we explore the influence of both ferroelectric and nonferroelectric dielectrics on the transport mechanism in TIPS-pentacene FETs using top-gate and bottom-gate architectures. Unlike nonferroelectric dielectrics, the temperature-dependent mobility when using PVDF-TrFE shows a negative coefficient beyond 200 K, similar to a weakly metallic behavior. Interestingly, the current-voltage characteristics from TIPS-pentacene diodes signal a space-charge-limited conduction (SCLC) for a discrete set of trap levels, suggesting that charge injection and transport occur through regions of ordering in the semiconductor. The carrier mobility extracted from temperature-dependent current-voltage characteristics from the trap-free SCLC region shows a negative coefficient beyond 200 K, similar to the trend observed in FETs with the ferroelectric dielectric.

II. EXPERIMENTAL DETAILS

A. Materials

6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) is procured from Sigma Aldrich, Inc., and used without any purification. Pentacene is procured from Tokyo Chemical Industry. The dielectric PVDF-TrFE (75:25) is obtained from Measurement Specialties, Inc. Poly-4-vinyl phenol (PVP) with average molecular weight (MW) 25 000 g/mol, propylene glycol monomethyl ether acetate (PGMEA) with MW 132.16 g/mol, and cross-linking agent poly(melamine-coformaldehyde)methylated 84% solution in 1 butane (PMMF) are procured from Sigma Aldrich, Inc. The solvents *N*, *N*-dimethylformamide and anhydrous toluene are procured from Sigma Aldrich, Inc. CYTOP (CTL-809M) is bought from Asahi Glass Co., Ltd., Japan. Glass substrates and SiO_2 on Si^{++} wafers are obtained from Fisher Scientific and Silicon Quest International, respectively.

B. Device fabrication

Bottom-gate top-contact and top-gate bottom-contact FETs are fabricated by evaporating 60-nm aluminum as

TABLE I. Thickness of the dielectric layers and average carrier mobilities from TIPS-pentacene FETs with different dielectrics at room temperature.

	PVDF-TrFE	SiO_2	PVP	CYTOP
Dielectric thickness (nm)	430	200	120	180
Average mobility ($cm^2/V\,s$)	0.003 ± 0.001	0.073 ± 0.014	0.13 ± 0.010	0.17 ± 0.02

a gate using a shadow mask. The PVDF-TrFE dielectric layer on glass substrates are obtained as described in a prior work [21]. The ferroelectric phase occurs in the all-trans phase or the β phase of the copolymer. Unlike PVDF, the copolymer PVDF-TrFE has the advantage of being ferroelectric directly after solution processing of the film [23]. Annealing the film at 135 °C further enhances the β phase of the copolymer. X-ray diffraction and Raman scattering from our annealed PVDF-TrFE films confirmed the presence of the β phase. The PVP layer on Al-coated glass slides are printed using ink-jet printing (Diamtix Materials Printer 2831). A 5 wt % solution of PVP in PGMEA with 2 wt % of the cross-linking agent PMMF is heated at 60 °C for 1 h before printing. This solution is filtered through a 0.45-μm polytetrafluorethylene filter. A substrate temperature of 60 °C and a 50-μm drop spacing improved the jetting of PVP and minimized the number of pinholes in the film. The PVP layer is printed twice to improve the capacitance of the device. After printing, the substrates are moved to a nitrogen environment and are annealed at 180 °C for 1 h.

TIPS-pentacene is dissolved in anhydrous toluene and stirred on a hot plate with a magnetic stirrer at 60 °C. The TIPS-pentacene film is obtained through slow crystallization growth in a solvent-saturated atmosphere. The orientation of the crystal axes is achieved by positioning the substrate inside a Petri dish at a 2° angle with respect to the horizontal. Substrates are placed inside the Petri dish in a manner such that the length of the channel is parallel to the receding direction of the drying solution. Drop casting is carried out using a pipette with the substrate kept at 50 °C; the lid is put back immediately afterwards to trap the solvent vapor and create a vapor-saturated condition inside the Petri dish. Pentacene films (60 nm) are obtained via a thermal-evaporation process (0.3 Å/s, 10^{-5} mbar) for the fabrication of diodes. All organic semiconducting films are followed by 50-nm thermally evaporated gold electrodes. For top-gate bottom-contact FETs, CYTOP is spin coated on top of TIPS-pentacene, which is followed by 60-nm aluminum as the top gate. The dielectric-film thicknesses are inferred from capacitance measurements of metal-insulating-semiconducting (MIS) devices (in the accumulation region) and are further confirmed with a reflectometer. The thicknesses of the dielectric layers are listed in Table I.

C. Device characterization

Room-temperature dc electrical characterizations are performed using two source meters, Keithley 2400 and Keithley 236, using a customized LabVIEW program. For temperature-dependent electrical measurements, a dual source meter Keithley 2612B is used. The FETs are kept inside a closed-cycle helium cryostat (APD Cryogenics) where the temperature may be varied from 11 to 480 K. The temperature is measured using a Lakeshore 330 temperature controller. The temperature dependence of both TIPS-pentacene and pentacene diodes are also measured with the APD cryostat.

The capacitance measurements from the MIS diodes are carried out with an HP 4284A precision *LCR* meter. During the measurement, a dc voltage is applied to the capacitor with a small ac-voltage signal superimposed over the dc signal. Capacitance is recorded as the dc bias is swept. The magnitude of the ac signal is 200 mV and the frequency of the signal is 5 kHz for all measurements. The dc signal is swept from both positive to negative bias and vice versa.

III. RESULTS AND DISCUSSIONS

Figure 1 shows a schematic of FET architectures used in this work. All PVDF-TrFE and PVP-based FETs are fabricated as bottom-gate structures, with aluminum as the gate electrode. The SiO_2-based FETs are fabricated as bottom-gate and bottom-contact structures. Bilayer SiO_2/PVDF-TrFE dielectrics [Fig. 1(b)] are also used. For the CYTOP dielectric, TIPS-pentacene is grown on SiO_2/Si^{++} substrates as shown in Fig. 1(c), which has the advantage that the same TIPS-pentacene film can be probed using two different dielectrics. This approach is also used for another batch of FETs, with PVDF-TrFE as the bottom gate (with bottom contacts) and CYTOP as the top gate. Figure 1(e) shows an optical image of TIPS-pentacene on the PVDF-TrFE layer. The crystalline grains grow more or less parallel to the source and drain contacts in the direction of the charge flow. The parallel growth of TIPS-pentacene is further seen in a scanning electron microscope (SEM) image [Fig. 1(d)].

A. FET characteristics

1. Room-temperature FET characteristics

Typical current-voltage output and transfer characteristics of TIPS-pentacene FETs on SiO_2 and PVDF-TrFE dielectric layers are shown in Figs. 2(a)–2(d). The FET properties are found to be strongly dependent upon the nature of the dielectric used; SiO_2-based FETs show a better performance than PVDF-TrFE–based FETs. This result is not surprising

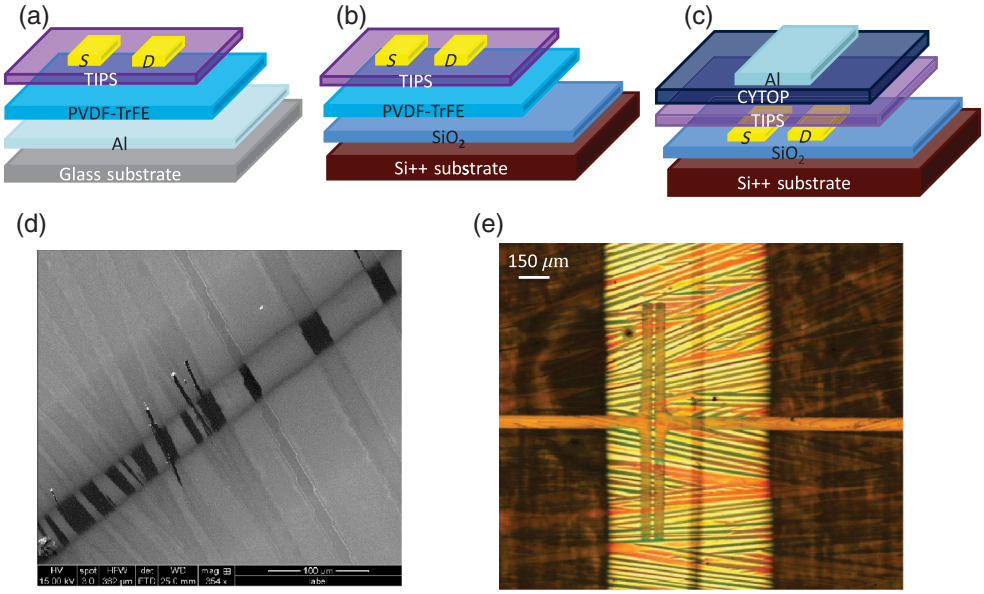

FIG. 1. FET device structures. (a) Bottom gate, top contact with PVDF-TrFE. (b) Bilayer bottom gate with top contact. (c) Dual FET with SiO_2 as the bottom gate and CYTOP as the top gate. (d) TIPS-pentacene on SiO_2 (SEM image). (e) TIPS-pentacene on PVDF-TrFE (optical image).

since PVDF-based dielectrics have a higher surface roughness [24] and are better conducting than other polymer and oxide dielectrics, resulting in a lower on:off ratio. There have been several strategies for improving the surface roughness and morphology of PVDF-based films by adding thin insulting layers, micropatterning, and optimization of annealing conditions [25–27].

The FET mobility is obtained from the saturation regime by using $\mu = (2L/WC_i)[(\partial\sqrt{I_{DS}})/\partial V_G]^2$, where C_i is the dielectric capacitance, W is the channel width, L is the channel length, V_G is the gate voltage, I_{DS} is the drain current, and μ is the field-effect mobility. For the transfer characteristics, the gate voltage is swept up to V_{DS}, which is selected in the saturation regime. By applying a linear fit to the saturation region, the hole mobilities are extracted for all sets of FETs. Several devices are measured, and the results shown in Fig. 2 are typical for a set of five to six devices. The on:off ratios are $> 10^5$ for the SiO_2/TIPS-pentacene FETs and slightly lower for other dielectric-based devices. Some of the best-performing devices resulted in $\mu = 0.2$ $cm^2/V\,s$ for CYTOP/TIPS-pentacene and 0.3 $cm^2/V\,s$ for the PVP dielectric. The average values of FET mobilities at room temperature, with their standard deviation for the different dielectrics, are shown in Table I. The average values of the carrier mobilities at 300 K as a function of the dielectric constant are found in Fig. S1 of

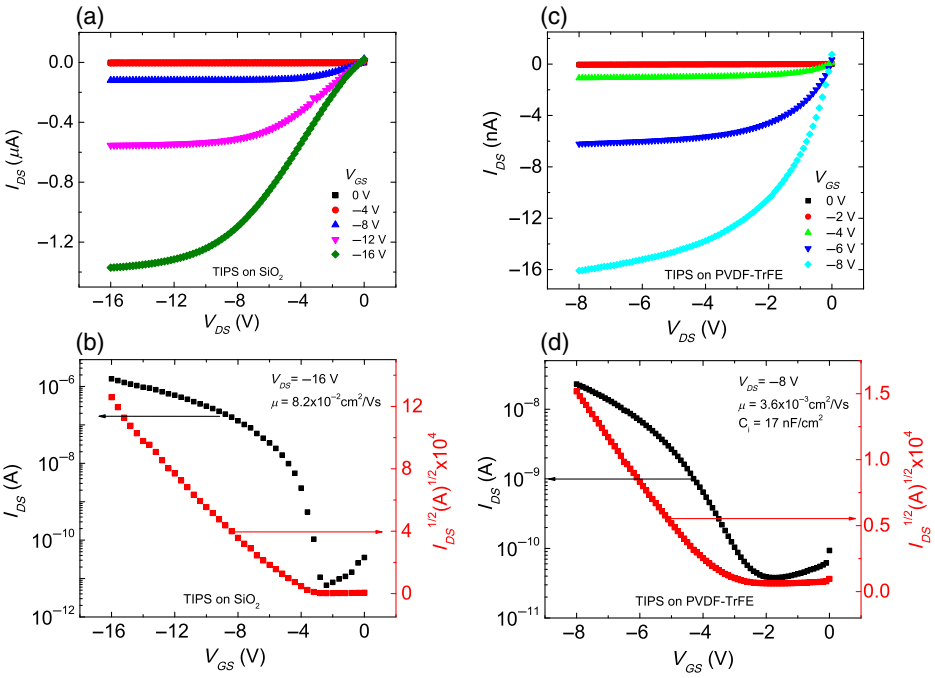

FIG. 2. (a),(b) Output and transfer characteristics of TIPS-pentacene on a SiO_2 FET. (c),(d) Output and transfer characteristics of TIPS-pentacene on a PVDF-TrFE FET.

the Supplemental Material [28]. There is a clear trend of reduced mobility with an increase in the dielectric constant of the insulating layer. It is not surprising that, although PVP and SiO_2 have similar dielectric constants, FETs with SiO_2 as the dielectric layer show a lower carrier mobility. Oxide dielectrics are known to trap more charges at the interface compared to polymer dielectrics.

2. *Temperature-dependent FET characteristics*

The temperature-dependent FET characteristics of TIPS-pentacene are measured from several devices with different dielectrics. We first focus on the difference between PVDF-TrFE and SiO_2. Since TIPS-pentacene films have been known to develop cracks above 340 K [29], our measurements are performed till approximately 320 K. This approach adds a constraint for the ferroelectric dielectric, as the FET measurements could not be performed till the ferroelectric-paraelectric transition, which occurs at approximately 390 K in PVDF-TrFE [22,30]. The transconductance curves at different temperatures are plotted for TIPS-pentacene FETs on SiO_2 and PVDF-TrFE in Figs. 3(a) and 3(c), respectively. In TIPS-pentacene/SiO_2, the slope of the transconductance curve is seen to increase with temperature, whereas in the TIPS-pentacene/PVDF-TrFE FET, the slope of the transconductance decreases beyond approximately 240 K [see the inset in Fig. 3(c)]. The extracted mobilities shown in Fig. 3(d) clearly show this trend. The FET mobilities for the SiO_2 device are plotted in Fig. 3(b); the trapped charge density (N_{trap}) obtained from the subthreshold swing of the transfer characteristics as a function of temperature is shown in the inset. We point out that other analytical methods yield more accurate values of trap densities [31]. With PVDF-TrFE, however, N_{trap} is seen to be discontinuous at the transition temperature, which is shown in P3HT- [22] and pentacene-based FETs [21].

The channel lengths of our FETs are 50–100 μm. As observed in many works, the contact resistance for such long-channel devices is negligible compared to the channel resistance [8,32]. The transistor performance is usually contact limited for channel lengths ≤ 10 μm [33]. For SiO_2, PVP, and CYTOP, the contact resistances of TIPS-pentacene FETs are a few orders of magnitude smaller than the channel resistance. For the PVDF-TrFE devices, the contact resistance is roughly 2 orders of magnitude smaller than the channel resistance. The slightly higher contact resistance with PVDF-TrFE has been attributed to the polarization fluctuation at the semiconductor-ferroelectric interface, which broadens the trap-charge distribution in the contact region of the semiconductor [34]. Furthermore, the contact resistance does not change much in the (100–300)-K range [35]—the temperature range used in this work. Given the long channel length of our devices and some of the established work showing the virtual temperature independence of Au contacts, the contact resistance does not significantly affect the transport measurements.

The leakage (gate) current is 3 orders of magnitude smaller than the drain current for PVDF-TrFE–and PVP-based FETs and did not change very much with temperature [28], which ensures that the extracted carrier mobilities at different temperatures, especially for PVDF-TrFE, are not affected by the gate current. The gate current for CYTOP and SiO_2 is slightly higher than in PVP and PVDF-TrFE,

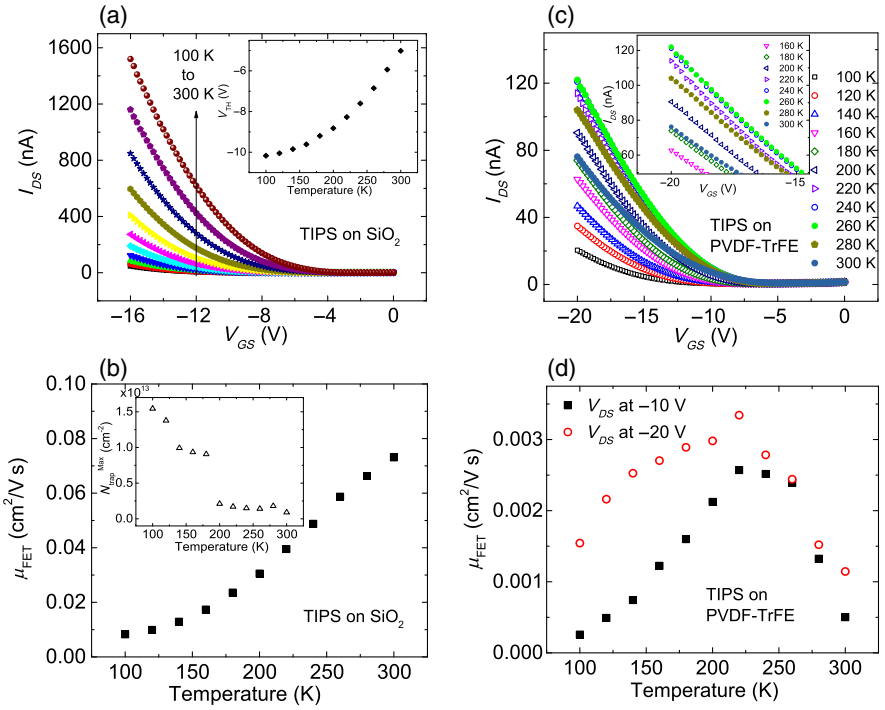

FIG. 3. Temperature-dependent transconductance curves as a function of temperature from TIPS-pentacene FETs with (a) SiO_2 and (c) PVDF-TrFE dielectric layers. [Inset in (a)] The change in the threshold voltage as a function of temperature. (b),(d) μ_{FET} mobilities as a function of temperature for the SiO_2 and PVDF-TrFE dielectrics, respectively. [Inset in (b)] Trap density as a function of temperature, which is extracted from the subthreshold swing values. The carrier mobilities in (d) are extracted from two different transconductance curves, swept at $V_{DS} = -10$ V and -20 V.

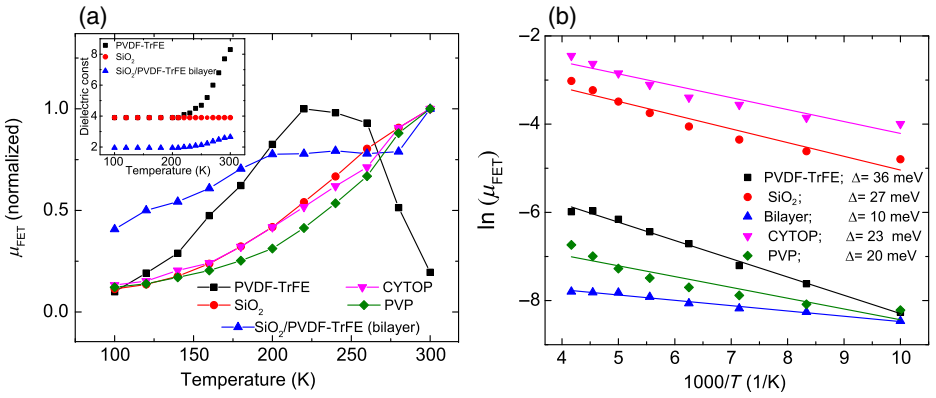

FIG. 4. (a) Normalized (to the maximum value) mobilities of TIPS-pentacene FETs as a function of temperature. The lines are a guide for the eye. (Inset) Variation of the dielectric constant of a few dielectrics as a function of temperature. (b) Arrhenius plots of TIPS-pentacene FET mobilities for various dielectric layers. The symbols are the experimental data and the lines are the fits. The bilayer refers to SiO_2/PVDF-TrFE.

although the ratio of the drain to the gate current—even for these FETs—is comparable to that found in other works [36].

Variable-temperature studies of organic FETs typically reveal thermally activated transport where the carrier mobility is attributed to an energetic disorder described in terms of thermally assisted hopping. This result can be fitted with an Arrhenius-type behavior with activation energy (Δ), on the order of tens to hundreds of meV, arising from polaron relaxation or from models based on multiple trap levels [37–39]. In such a mechanism, the carrier mobility is given by $\mu = \mu_0 \exp(-\Delta/k_B T)$, where μ_0 is the mobility in the absence of any traps and k_B is the Boltzmann constant. Thermally activated transport in TIPS-pentacene has been observed by other groups with some nuances of temperature regimes [40] and dependence on the geometry of the device [5]. The above model is obviously more complex when the polarization field of the dielectric interface needs to be considered. As shown in Fig. 3(b), the SiO_2-based FET exhibits an enhanced mobility in the entire temperature range, whereas the PVDF-TrFE–based FET shows decreased carrier mobility beyond approximately 220 K. When the same PVDF-TrFE–based device is swept at a higher voltage (till $V_{DS} = V_G = -20$ V), the extracted mobilities are higher [Fig. 3(d)], but the trend is the same as with the −10 V data: namely, a decrease in the carrier mobility beyond 220 K is observed.

In order to understand the differences in transport mechanism in TIPS-pentacene FETs with a nonferroelectric dielectric versus a ferroelectric dielectric, we measure the temperature dependence of the carrier mobility in TIPS-pentacene FETs with a variety of dielectrics and architectures. We also use a bilayer dielectric SiO_2/PVDF-TrFE, shown in Fig. 1(b), where the interface property between TIPS-pentacene and the PVDF-TrFE layer is similar to the single layer PVDF-TrFE FET, except that, in the bilayer device, the PVDF-TrFE layer does not act as a ferroelectric layer.

For a better visualization of FET carrier mobilities as a function of temperature, we plot the normalized values in Fig. 4(a). See Ref. [28] for the actual values of extracted mobilities as a function of temperature for the various dielectrics. In the temperature range of our measurements, the dielectric constant (k) of PVDF-TrFE changes from roughly 4 at 100 K to 8 at 300 K, as shown in the inset. Except for the PVDF-TrFE dielectric-based FET, which reaches a maximum at around 220 K, all other FETs show their highest mobility at 300 K. These features are reversible. Cycling the temperature few times results in a slight decrease of the carrier mobilities, but the trends remain the same. A clear distinction is seen between bilayer (SiO_2/PVDF-TrFE) and single-layer PVDF-TrFE FETs. It is important to realize that, in the bilayer device, since the SiO_2 layer is gated, PVDF-TrFE is not an active ferroelectric layer; the combined k is much smaller than for either of the dielectrics. Although in both FETs the interface between TIPS-pentacene and PVDF-TrFE is identical, the bilayer device does not show $d\mu/dT < 0$, suggesting that the ferroelectric nature of PVDF-TrFE is responsible for the negative coefficient of mobility beyond 220 K. Figure 4(b) shows the Arrhenius plots of the FET mobilities in a temperature range of 100–220 K, where the activation energies vary between 10 and 40 meV for the various dielectrics. We note that the activation energy reported for a printed PVP (TIPS-pentacene) FET is slightly higher than in Fig. 4(b), as the temperature range over which the measurements are conducted is more restrained (160–320 K) [41]. The data shown here for SiO_2 and CYTOP refer to the same TIPS-pentacene layer where the geometries are either top gate or bottom gate [Fig. 1(c)].

Prior work on ferroelectric FETs has shown that charge transport is strongly influenced by polarization fluctuation [21]. In the presence of a ferroelectric dielectric, the two competing effects as a function of temperature are a suppression of the charge-carrier mobility in the ferroelectric phase (as a result of the coupling of the carrier to the dielectric polarization of the gate insulator) and an activated hopping transport responsible for enhancing μ_{FET}. Because of the constraints with temperatures above 320 K for TIPS-pentacene films, the full polarization effect of PVDF-TrFE cannot be explored in this work. The dielectric constant of PVDF-TrFE is greatly enhanced beyond 300 K, reaching close to 25 at approximately 400 K [22]. The slightly higher activation energy of PVDF-TrFE compared to other

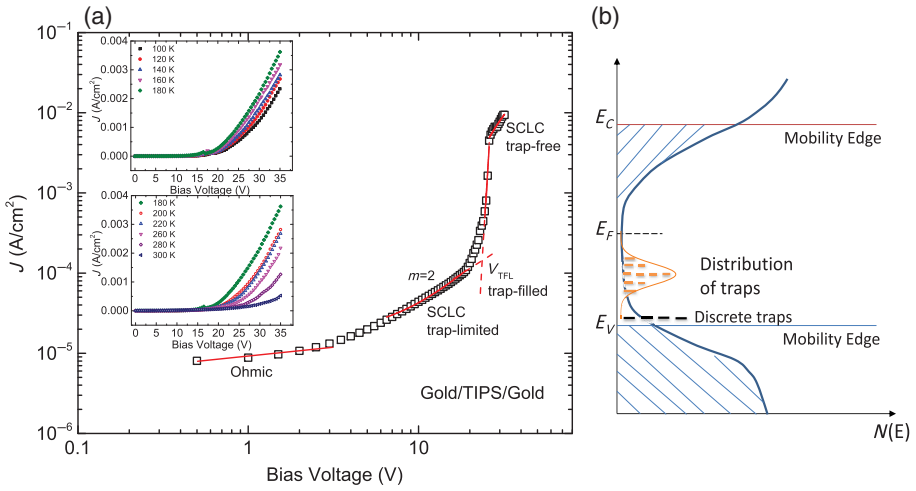

FIG. 5. (a) Current density versus voltage plot for TIPS-pentacene diode at room temperature. The J versus V sweep shows all four distinct regions, characteristic of SCLC with discrete trap levels. (Inset) Temperature-dependent J-V curves from 100 to 180 K, and from 180 to 300 K. (b) Schematic of the density of states in TIPS-pentacene.

dielectrics [seen in Fig. 4(b)] may be explained on the basis of a higher dynamic coupling between the charge carriers to the electronic polarization. Overall, the activation energies seen here in the low-temperature range for the various dielectrics are similar to high-mobility TIPS-pentacene FETs [6].

Several PVDF-TrFE single-layer FETs are fabricated, and they all show a similar behavior in the carrier mobilities seen in Fig. 3(d). Another batch of FETs is fabricated with PVDF-TrFE as the bottom gate and CYTOP as the top gate, with the same TIPS-pentacene film being the active layer for both dielectrics. The PVDF-TrFE geometry entailed a bottom-contact device. A distinct thermally activated transport is observed with CYTOP, whereas, with the PVDF-TrFE layer, a decrease in mobility is observed beyond 240 K [28]. The PVDF-TrFE layer in this dual-geometry FET is 550 nm, compared to the 430-nm-thick layer in Figs. 3(c) and 3(d). The polarization field from a thicker ferroelectric layer is lower than from a thinner layer (also observed in pentacene/PVDF-TrFE FETs [21]); hence, it is not surprising that the percentage decrease in mobility for the dual-geometry FET is lower than for the device shown in Figs. 3 and 4. The connection between the polarization effect and the change in carrier mobility is elaborated on in Sec. III B. In order to further elucidate whether the negative coefficient of mobility beyond 220 K in TIPS-pentacene is an inherent property of the semiconductor itself, we conduct detailed temperature dependence from TIPS-pentacene diodes and compare them with pentacene diodes.

B. Diode characteristics: TIPS-pentacene versus pentacene

We use the two Au contacts across TIPS-pentacene [as shown in Fig. 1(e)] to measure the bulk current-voltage characteristics (the hole current) as a function of temperature. This structure further ensures that we are using the same TIPS-pentacene film, with an identical trap distribution, as used for the FET measurements. SCLC-based models have been used to study trap states in organic molecules and polymers for more than 50 years. Shallow trapping with a single trap level was initially observed in pure polycrystalline organic molecules such as anthracene and naphthalene [42]. Subsequently, such a discrete set of trap-level SCLC has also been observed in semicrystalline blue-emitting ethyl-hexyl polyfluorene (PF2/6) conjugated polymers [43,44], where regions of structural ordering are believed to be responsible for charge injection and transport.

Figure 5(a) shows the current density (J) versus voltage (V) for hole carriers in a TIPS-pentacene diode. The J-V curve (the log-log plot) shows four distinct regions, characteristic of a one-carrier single set of traps. The first is the Ohmic region, where $J = (qn_0\mu V)/d$, with q being the charge, n_0 the free carrier density, d the thickness of film between the electrodes, and μ the carrier mobility. The second region is SCLC trap limited, with the current density given by

$$J = \frac{9}{8}\epsilon\epsilon_0\mu\theta\frac{V^2}{d^3}. \quad (1)$$

In Eq. (1), θ is the trapping fraction, ϵ the dielectric constant of the polymer, and ϵ_0 the permittivity of free space. For an exponential trap distribution, $J \propto V^m$, with $m > 2$. The third region in Fig. 5, where the current increases vertically, is the trap-filled limit. The onset is the trap-filled voltage, V_{TFL}, which is proportional to the density of traps (N_t):

$$N_t = \frac{3}{2}\frac{\epsilon\epsilon_0 V_{\mathrm{TFL}}}{qd^2}. \quad (2)$$

The final region is the current only limited by the space charge and free from the influence of traps. The trap-free SCLC region is similar to the second region expressed by Eq. (1), with $\theta = 1$. Furthermore, the trap energy (E_t) is related to the trapping parameter by $\theta = (N_v/N_t)\exp[-(E_t/k_BT)]$, where N_v is the density of states within k_BT of the valence band edge.

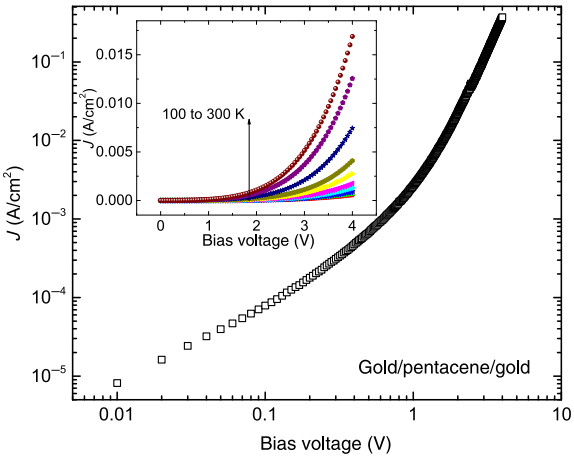

FIG. 6. Current density versus voltage plot for a pentacene diode at room temperature. (Inset) Temperature-dependent J-V curves from 100 to 300 K.

The first run yields all four regions shown in Fig. 5(a); however, subsequent voltage sweeps somewhat decrease the current. This decrease is most likely due to the generation of additional traps while sweeping the voltage beyond V_{TFL}, which is also observed in PF2/6 [43]. To obtain the different parameters in Eqs. (1) and (2), one then has to resort to the very first run. From the trap-free SCLC region shown in Fig. 5(a), we obtain a carrier mobility of approximately $1.4\ \mathrm{cm}^2/\mathrm{V\,s}$ at room temperature. The second run yields more than an order of magnitude lower value of the mobility. The SCLC data are also confirmed from other Au/TIPS-pentacene/Au devices and from different runs of the same device [28]. We use the trap-free SCLC region to obtain μ at all temperatures. An average value of $\mu = 0.08 \pm 0.03\ \mathrm{cm}^2/\mathrm{V\,s}$ at 300 K is found by using the second or third sweep from different batches of TIPS-pentacene diodes. More than the absolute values, we are interested in the trend in carrier mobilities as a function of temperature for obtaining insights into the bulk-transport phenomenon.

Since PVDF-TrFE–based pentacene FETs shows no negative coefficient of carrier mobility with temperature [21], we further compare the nature of the trap states in TIPS-pentacene with pentacene, and thus we perform a temperature-dependent J-V measurement from pentacene diodes as well. These diodes are grown by sandwiching a pentacene film between ITO and Au (in a vertical geometry), ensuring that it is predominantly hole transport. Figure 6 shows the J-V characteristics (the log-log plot) from a pentacene diode at room temperature. Unlike TIPS-pentacene, discrete-trap SCLC is not observed. The SCLC follows a distribution of traps, which is typically seen in most π-conjugated molecules and polymers. With increasing temperature, the slope of the J-V curve continuously increases (as seen in the inset). Although trap-free SCLC is not observed, Eq. (1) fits the voltage range 0.2 to 1 V quite well, from where we can then deduce the product of $\theta\mu$.

The hole mobilities extracted from the J-V measurements by fitting the trap-free SCLC region with $J \propto V^2$ dependence in TIPS-pentacene are plotted in Fig. 7(a). Beyond 180 K, μ is seen to decrease with an increase in temperature. These measurements have been repeated with several devices where the architecture is similar to Fig. 1(e), and the TIPS-pentacene is grown on different dielectrics (CYTOP, SiO_2, PVDF-TrFE). We point out that the dielectric layer plays no role in these measurements and that charge injection and transport is solely through the TIPS-pentacene film. Similar experiments from pentacene highlight that the J-V curve does not show a single-trap SCLC behavior (Fig. 6). The trap-limited region agrees with $J \propto V^2$ dependence, from where we obtain the trends in mobilities with temperature. A cautionary remark here is that since the trapping fraction is unknown, we obtain the product of $\theta\mu$ from temperature-dependent J-V curves [plotted in Fig. 7(b)]. It is evident that μ increases with temperature even from the individual J-V curves of the pentacene diode (see inset in Fig. 6). As an additional check, the product of $\theta\mu$ is also obtained for TIPS-pentacene from the trap-limited SCLC region, shown in Fig. 7(a). This product shows the same trend as μ.

Temperature-dependent J-V measurements from two terminal devices allow an independent measure of transport in organic semiconductors without the influence of the dielectric. In comparing TIPS-pentacene to pentacene, we find that the J-V diode characteristics are quite different:

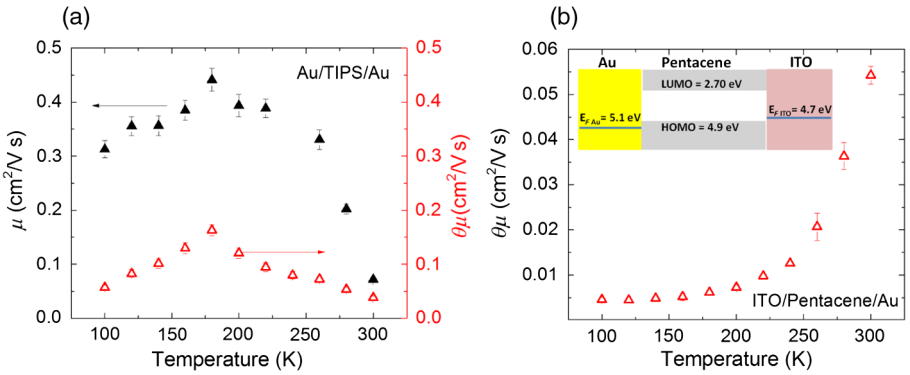

FIG. 7. (a) Hole mobility (the filled triangles) as a function of temperature extracted from the trap-free SCLC region in a TIPS-pentacene diode. The open triangles show the product of the trapping fraction and the carrier mobility in TIPS-pentacene extracted from the trap-limited SCLC region. (b) Product of the trapping fraction and carrier mobility as a function of temperature for a pentacene diode. (Inset) Schematic of the energy levels.

TIPS-pentacene distinctly shows a discrete-trap behavior with all four regions, unlike pentacene. Furthermore, the hole mobilities in pentacene show a hopping transport with $d\mu/dT > 0$ in the temperature range of 100–300 K. High-purity crystals such as anthracene and tetracene with discrete-trap SCLC typically display a diminishing mobility with temperature (for both electrons and holes) [42,45]. In tetracene, however, the decreasing mobility with temperatures beyond 180 K has been attributed to a phase transition [46]. Moreover, temperature dependence of the drift mobilities in crystals belonging to the acene family and other systems is strongly dependent upon the crystallographic directions [47]. The negative coefficient of mobility observed in TIPS-pentacene thus follows other molecular semiconductors that exhibit discrete-trap SCLC behavior.

It is instructive to correlate the bulk mobility of pentacene with FET transport characteristics. Thermally activated transport in pentacene FETs (using nonferroelectric dielectrics) has been observed by many groups [48–50]. Pentacene-based FETs with PVDF-TrFE show two regimes in transport: polarization influenced as long as the dielectric is in the ferroelectric phase and an activated transport when the dielectric is in the paraelectric phase [21]. In the ferroelectric phase, Fröhlich polarons play a role in suppressing the carrier mobility. The nature of transport in pentacene FETs agrees well with bulk transport (as seen from the diode characteristics here). Overall, the distribution of trap states in pentacene favors an activated transport. The weak dependence of the charge-carrier mobility (in pentacene FETs) in the ferroelectric phase of PVDF-TrFE is attributed to a polarization-fluctuation-driven transport.

The bulk-transport properties in TIPS-pentacene is different from pentacene. A distinct discrete shallow-trap SCLC is observed in TIPS-pentacene compared to the distribution of traps in pentacene. Beyond 180 K, a negative coefficient of mobility is observed. This result is completely reversible upon cycling of the temperature. Our results agree with the recent charge-modulation-spectroscopy results of Meneau *et al.* [6], where it is seen that charges become localized onto individual molecules in shallow-trap states at low temperatures. Although the FET mobilities reported in this work are 2 to 3 orders of magnitude smaller than what is required to approach disorder-free limits, the temperature dependence of carrier mobilities from PVDF-TrFE–based FETs clearly shows $d\mu/dT < 0$ beyond 200 K, consistent with bulk-transport measurements. The higher dielectric constant of PVDF-TrFE beyond 200 K (and under substantial electric fields) may partially reduce the trap depth due to screening, resulting in a detrapping mechanism. This process facilitates a transport through discrete traps, as is schematically shown in Fig. 5(b), which is manifested as bandlike transport. Such a behavior is not observed in nonferroelectric dielectric–based FETs due to the lack of any polarization field and lower screening effects.

A high dielectric constant of the gate insulator thus results in a strong dynamic coupling of the charge carriers, mainly due to the Fröhlich polarons, which tends to suppress carrier mobilities, as observed in pentacene FETs [21] and P3HT FETs [22]. The tunability of the dielectric constant of PVDF-TrFE with temperature provides a platform for changing the coupling between the charge carriers and the electronic polarization. Along with this coupling, the nature of the trap states also plays a role in dictating transport properties as seen in TIPS-pentacene FETs. Increasing the dielectric constant may enhance screening, reducing the trap depth and thus facilitating transport through discrete trap states. This consequence is manifested as a negative coefficient of carrier mobility with temperature in TIPS-pentacene FETs.

IV. CONCLUSIONS

Drop-casted TIPS-pentacene films exhibit single-trap-level SCLC, similar to high-purity crystalline organic molecules. The origin of these traps could be structural or other chemical defects, which typically give rise to discrete trap states and may occur at the grain boundaries. A bulk-transport measurement from TIPS-pentacene clearly shows a negative coefficient of mobility beyond 180 K. A similar behavior is seen in FET transport when a ferroelectric dielectric, PVDF-TrFE, is used. As such, the FET mobilities reported here are lower than the minimum condition mobility required for observing disorder-free transport, yet the presence of a polarization field of the ferroelectric dielectric results in a transport mechanism, exemplifying bandlike transport above a certain temperature. We attribute this result to an ease of a detrapping mechanism owing to the nature of discrete traps. Ferroelectric dielectrics with the ability for tuning their polarization strength with temperature provide a mechanism for exploring different transport regimes in organic FETs. This work paves the way for exploring bandlike transport ($d\mu/dT < 0$) in other solution-processable π-conjugated molecules and polymers with discrete trap levels by utilizing ferroelectric dielectrics in FET geometries.

ACKNOWLEDGMENTS

We acknowledge the support of this work through the National Science Foundation under Grant No. ECCS-1305642.

[1] S. Fratini and S. Ciuchi, Bandlike Motion and Mobility Saturation in Organic Molecular Semiconductors, Phys. Rev. Lett. **103**, 266601 (2009).

[2] V. Coropceanu, J. Cornil, D. A. da Silva Filho, Y. Olivier, R. Silbey, and J-L. Bredas, Charge transport in organic semiconductors, Chem. Rev. **107**, 926 (2007).

[3] V. Podzorov, E. Menard, J. A. Rogers, and M. E. Gershenson, Hall Effect in the Accumulation Layers on the Surface of Organic Semiconductors, Phys. Rev. Lett. **95**, 226601 (2005).
[4] J. Takeya, K. Tsukagoshi, Y. Aoyagi, T. Takenobu, and Y. Iwasa, Hall effect of quasi-hole gas in organic single-crystal transistors, Jpn. J. Appl. Phys. **44**, L1393 (2005).
[5] T. Sakanoue and H. Sirringhaus, Band-like temperature dependence of mobility in a solution-processed organic semiconductor, Nat. Mater. **9**, 736 (2010).
[6] A. Y. B. Meneau, Y. Olivier, T. Backlund, M. James, D. W. Breiby, J. W. Andreasen, and H. Sirringhaus, Temperature dependence of charge localization in high-mobility, solution-crystallized small molecule semiconductors studied by charge modulation spectroscopy, Adv. Funct. Mater. **26**, 2326 (2016).
[7] M. Kohei, M. Takaaki, and I. Mitsumasa, Band-like transport observed in TIPS-pentacene thin film by time-resolved microscopic optical second-harmonic generation imaging, Appl. Phys. Express **8**, 041601 (2015).
[8] S. P. Senanayak, A. Z. Ashar, C. Kanimozhi, S. Patil, and K. S. Narayan, Room-temperature bandlike transport and Hall effect in a high-mobility ambipolar polymer, Phys. Rev. B **91**, 115302 (2015).
[9] S. Schott, E. Gann, L. Thomsen, S.-H. Jung, J.-K. Lee, C. R. McNeill, and H. Sirringhaus, Charge-transport anisotropy in a uniaxially aligned diketopyrrolopyrrole-based copolymer, Adv. Mater. **27**, 7356 (2015).
[10] D. Venkateshvaran, M. Nikolka, A. Sadhanala, V. Lemaur, M. Zelazny, M. Kepa, M. Hurhangee, A. J. Kronemeijer, V. Pecunia, I. Nasrallah, I. Romanov, K. Broch, I. McCulloch, D. Emin, Y. Olivier, J. Cornil, D. Beljonne, and H. Sirringhaus, Approaching disorder-free transport in high-mobility conjugated polymers, Nature (London) **515**, 384 (2014).
[11] S. Stafstrom, Electron localization and the transition from adiabatic to nonadiabatic charge transport in organic conductors, Chem. Soc. Rev. **39**, 2484 (2010).
[12] Y. Chen, H. T. Yi, and V. Podzorov, High-Resolution ac Measurements of the Hall Effect in Organic Field-Effect Transistors, Phys. Rev. Applied **5**, 034008 (2016).
[13] H. T. Yi, Y. N. Gartstein, and V. Podzorov, Charge carrier coherence and Hall effect in organic semiconductors, Sci. Rep. **6**, 23650 (2016).
[14] L. B. Schein, C. B. Duke, and A. R. McGhie, Observation of the Band-Hopping Transition for Electrons in Naphthalene, Phys. Rev. Lett. **40**, 197 (1978).
[15] L. J. Wang, Q. Peng, Q. K. Li, and Z. Shuai, Roles of inter- and intramolecular vibrations and band-hopping crossover in the charge transport in naphthalene crystal, J. Chem. Phys. **127**, 044506 (2007).
[16] L. Wang, O. V. Prezhdo, and D. Beljonne, Mixed quantum-classical dynamics for charge transport in organics, Phys. Chem. Chem. Phys. **17**, 12395 (2015).
[17] H. Houili, J. D. Picon, L. Zuppiroli, and M. N. Bussac, Polarization effects in the channel of an organic field-effect transistor, J. Appl. Phys. **100**, 023702 (2006).
[18] S. J. Konezny, M. N. Bussac, and L. Zuppiroli, Hopping and trapping mechanisms in organic field-effect transistors, Phys. Rev. B **81**, 045313 (2010).
[19] I. N. Hulea, S. Fratini, H. Xie, C. L. Mulder, N. N. Iossad, G. Rastelli, S. Ciuchi, and A. F. Morpurgo, Tunable Fröhlich polarons in organic single-crystal transistors, Nat. Mater. **5**, 982 (2006).
[20] P. Yu and M. Cardona, *Fundamentals of Semiconductors: Physics and Materials Properties*, 4th ed., Graduate Texts in Physics (Springer-Verlag, Berlin, 2010).
[21] A. Laudari and S. Guha, Polarization-induced transport in ferroelectric organic field-effect transistors, J. Appl. Phys. **117**, 105501 (2015).
[22] S. P. Senanayak, S. Guha, and K. S. Narayan, Polarization fluctuation dominated electrical transport processes of polymer-based ferroelectric field effect transistors, Phys. Rev. B **85**, 115311 (2012).
[23] G. Knotts, A. Bhaumik, K. Ghosh, and S. Guha, Enhanced performance of ferroelectric-based all organic capacitors and transistors through choice of solvent, Appl. Phys. Lett. **104**, 233301 (2014).
[24] C. A. Nguyen, S. G. Mhaisalkar, J. Ma, and P. S. Lee, Enhanced organic ferroelectric field effect transistor characteristics with strained poly(vinylidene fluoride-trifluoroethylene) dielectric, Org. Electron. **9**, 1087 (2008).
[25] K. Müller, I. Paloumpa, K. Henkel, and D. Schmeisser, A polymer high-*k* dielectric insulator for organic field-effect transistors, J. Appl. Phys. **98**, 056104 (2005).
[26] J-H. Lee, H-J. Yoon, T. Y. Kim, M. K. Gupta, J. H. Lee, W. Seung, H. Ryu, and S-W. Kim, Micropatterned PVDF-TrFE film-based piezoelectric nanogenerators for highly sensitive self-powered pressure sensors, Adv. Funct. Mater. **25**, 3203 (2015).
[27] P-H. Ducrot, I. Dufour, and C. Ayela, Optimization of PVDF-TrFE processing conditions for the fabrication of organic MEMS resonators, Sci. Rep. **6**, 19426 (2016).
[28] See Supplemental Material at http://link.aps.org/supplemental/10.1103/PhysRevApplied.6.044007 for the carrier mobilities as a function of the dielectric constant at 300 K and the mobilities for all FETs as a function of temperature; leakage currents; architecture and characteristics of the dual-geometry TIPS-penatcene FET, utilizing the same active layer for both CYTOP and PVDF-TrFE dielectrics; and SCLC characteristics of other Au/TIPS-pentacene/Au diodes.
[29] J.-H. Bae, J. Park, C.-M. Keum, W.-H Kim, M.-H. Kim, S.-O. Kim, S. K. Kwon, and S.-D. Lee, Thermal annealing effect on the crack development and the stability of 6,13-bis (triisopropylsilylethynyl)-pentacene field-effect transistors with a solution-processed polymer insulator, Org. Electron. **11**, 784 (2010).
[30] J. M. Guimaraes Neto, O. N. Oliveira, and R. M. Faria, Influence of phase transitions on the spontaneous voltage in PVDF/TrFE copolymers, Appl. Phys. A **71**, 267 (2000).
[31] W. L. Kalb and B. Batlogg, Calculating the trap density of states in organic field-effect transistors from experiment: A comparison of different methods, Phys. Rev. B **81**, 035327 (2010).
[32] F. Ante, D. Kälblein, T. Zaki, U. Zschieschang, K. Takimiya, M. Ikeda, T. Sekitani, T. Someya, J. N. Burghartz, K. Kern, and H. Klauk, Contact resistance and megahertz operation of aggressively scaled organic transistors, Small **8**, 73 (2012).

[33] D. J. Gundlach, L. Zhou, J. A. Nichols, T. N. Jackson, P. V. Necliudov, and M. S. Shur, An experimental study of contact effects in organic thin film transistors, J. Appl. Phys. **100**, 024509 (2006).

[34] H. Sun, Y. Yin, Q. Wang, Q. Jun, Y. Wang, K. Tsukagoshi, X. Wang, Z. Hu, L. Pan, Y. Zheng, Y. Shi, and Y. Li, Reducing contact resistance in ferroelectric organic transistors by buffering the semiconductor/dielectric interface, Appl. Phys. Lett. **107**, 053304 (2015).

[35] P. V. Pesavento, R. J. Chesterfield, C. R. Newman, and C. D. Frisbie, Gated four-probe measurements on pentacene thin-film transistors: Contact resistance as a function of gate voltage and temperature, J. Appl. Phys. **96**, 7312 (2004).

[36] E. Orgiu, S. Locci, B. Fraboni, E. Scavetta, P. Lugli, and A. Bonfiglio, Analysis of the hysteresis in organic thin-film transistors with polymeric gate dielectric, Org. Electron. **12**, 477 (2011).

[37] G. Horowitz, Organic field-effect transistors, Adv. Mater. **10**, 365 (1998).

[38] J. A. Letizia, J. Rivnay, A. Facchetti, M. A. Ratner, and T. J. Marks, Variable temperature mobility analysis of *n*-channel, *p*-channel, and ambipolar organic field-effect transistors, Adv. Funct. Mater. **20**, 50 (2010).

[39] J. Veres, S. D. Ogier, S. W. Leeming, D. C. Cupertino, and S. M. Khaffaf, Low-*k* insulators as the choice of dielectrics in organic field-effect transistors, Adv. Funct. Mater. **13**, 199 (2003).

[40] Y. Xu, M. Benwadih, R. Gwoziecki, R. Coppard, T. Minari, C. Liu, K. Tsukagoshi, J. Chroboczek, F. Balestra, and G. Ghibaudo, Carrier mobility in organic field-effect transistors, J. Appl. Phys. **110**, 104513 (2011).

[41] K. Gooden, A. Laudari, G. Knotts, and S. Guha, Printed dielectric-based organic diodes and transistors, Flex. Print. Electron. **1**, 015004 (2016).

[42] M. Pope and C. E. Swenberg, *Electronic Processes in Organic Crystals and Polymers*, 2nd ed. (Oxford University Press, Oxford, 1999).

[43] M. Arif, M. S. Yun, S. Gangopadhyay, K. Ghosh, L. Fadiga, F. Galbrecht, U. Scherf, and S. Guha, Polyfluorene as a model system for space-charge-limited conduction, Phys. Rev. B **75**, 195202 (2007).

[44] S. Guha, M. Arif, S. Gangopadhyay, and U. Scherf, Space-charge-limited conduction in ethyl-hexyl substituted polyfluorene, J. Mater. Sci. Mater. Electron. **20**, 351 (2009).

[45] L. B. Schein, C. B. Duke, and A. R. McGhie, Observation of the Band-Hopping Transition for Electrons in Naphthalene, Phys. Rev. Lett. **40**, 197 (1978).

[46] R. W. I. de Boer, M. Jochemsen, T. M. Klapwijk, A. F. Morpurgo, J. Niemax, A. K. Tripathi, and J. Pflaum, Space charge limited transport and time of flight measurements in tetracene single crystals: A comparative study, J. Appl. Phys. **95**, 1196 (2004).

[47] N. Karl and J. Ziegler, Generation and transport of charge carriers in the charge-transfer complex anthracene-pyromellitic-dianhydride, Chem. Phys. Lett. **32**, 438 (1975).

[48] D. Knipp, R. A. Street, A. Völkel, and J. Ho, Pentacene thin film transistors on inorganic dielectrics: Morphology, structural properties, and electronic transport, J. Appl. Phys. **93**, 347 (2003).

[49] D. Guo, T. Miyadera, S. Ikeda, T. Shimada, and K. Saiki, Analysis of charge transport in a polycrystalline pentacene thin film transistor by temperature and gate bias dependent mobility and conductance, J. Appl. Phys. **102**, 023706 (2007).

[50] L. Dunn and A. Dodabalapur, Temperature dependent transient velocity and mobility studies in an organic field effect transistor, J. Appl. Phys. **107**, 113714 (2010).