Dual-Gate Velocity-Modulated Transistor Based on Black Phosphorus

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The layered semiconductor black phosphorus has attracted attention as a 2D atomic crystal that can be prepared in ultrathin layers for operation as field-effect transistors. Despite the susceptibility of black phosphorus to photo-oxidation, improvements to the electronic quality of black phosphorus devices has culminated in the observation of the quantum Hall effect. In this paper, we demonstrate the room-temperature operation of a dual-gated black phosphorus transistor operating as a velocity-modulated transistor, whereby modification of hole density distribution within a black phosphorus quantum well leads to a twofold modulation of hole mobility. Simultaneous modulation of Schottky-barrier resistance leads to a fourfold modulation of transconductance at a fixed hole density. Our work explicitly demonstrates the critical role of charge-density distribution upon charge carrier transport within 2D atomic crystals.

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I. INTRODUCTION

Black phosphorus (bP) is an elemental allotrope and a direct band-gap semiconductor with a puckered, honeycomb layer structure [1–3] that can be exfoliated down to atomic few-layer thickness [4–9]. Although bP is the most thermodynamically stable allotrope of phosphorus, photo-oxidation in the presence of water, oxygen, and visible light is known to degrade bP with a reaction rate that increases as the bP layer thickness decreases [7]. Several materials have been used to encapsulate bP in order to protect it against photo-oxidation, including hexagonal boron-nitride [10–12], aluminum oxide [13], silicon oxide [14], parylene [7], and poly-methylmethacrylate [15]. Recent works also show that 2D hole transport can be achieved in a single 2D subband within an accumulation layer of many-layer bP [10,12,15], effectively combining 2D transport characteristics with the increased chemical stability of many-layer bP. These advances have culminated in the observation of the quantum Hall effect in bP [16]. In parallel, the optoelectronic properties of bP FETs are also being explored [17,18]. Nonetheless, further understanding and control of transconductance, carrier mobility, and contact resistance in bP field-effect transistors (FETs) is desired.

We report here an experimental investigation of the transport characteristics of bP FETs with an asymmetric dual-gate geometry consisting of top- and bottom-gate electrodes capable of inducing hole accumulation layers at the top and bottom of the bP channel. We find the top-hole accumulation layer to have a mobility of $\mu < 0.1\ \mathrm{cm}^2/\mathrm{Vs}$ while we find the bottom-hole accumulation layer to have a mobility of $\mu \sim 400\ \mathrm{cm}^2/\mathrm{Vs}$, in the absence of gate-voltage optimization. We find the top gate to be effective in modulating the characteristics of the bottom accumulation layer, including both field-effect mobility and Schottky-barrier contact resistance. The mobility modulation effect, in particular, enables the operation of the dual-gate bP FET as a velocity-modulated transistor (VMT), first proposed by Sakaki [19] to overcome the limitation on transistor switching frequency imposed by the channel transit time of charge carriers. Mobility modulation has since been demonstrated in GaAs/(AlGa)As heterojunctions [20], wide GaAs/(AlGa)As quantum wells [21], silicon-on-insulator FETs [22], and the $LaAlO_3/SrTiO_3$ interface [23]. Room-temperature VMT operation in silicon-on-insulator FETs has been demonstrated with up to 1.4-fold mobility modulation [22]. Our asymmetric dual-gate bP FETs exhibit a twofold mobility modulation at room temperature, and the underlying mechanism is modulation of hole density distribution with the naked bP quantum-well channel of the bP FET, with a resultant modulation of scattering by charged impurities, surface roughness, and other spatially dependent scattering mechanisms. Simultaneously, bP FETs exhibit strong Schottky-barrier modulation. First conclusively observed in carbon nanotube FETs [24], Schottky-barrier modulation has recently been shown to dominate off-state conductance of bP FETs [25]. The combination of two-point and four-point resistance measurements in our work enables us to independently measure mobility modulation and Schottky-barrier modulation. The combined effects of mobility modulation and Schottky-barrier modulation of dual-gate bP FETs enables fourfold transconductance modulation at a fixed carrier density of $4 \times 10^{11}\ \mathrm{cm}^{-2}$ induced by the bottom gate.

II. TRANSISTOR FABRICATION

Nanometer-scale bP crystals are exfoliated using a polydimethylsiloxane stamp technique [15]. The bP crystals are 99.998% purity from Smart-elements (Vienna,

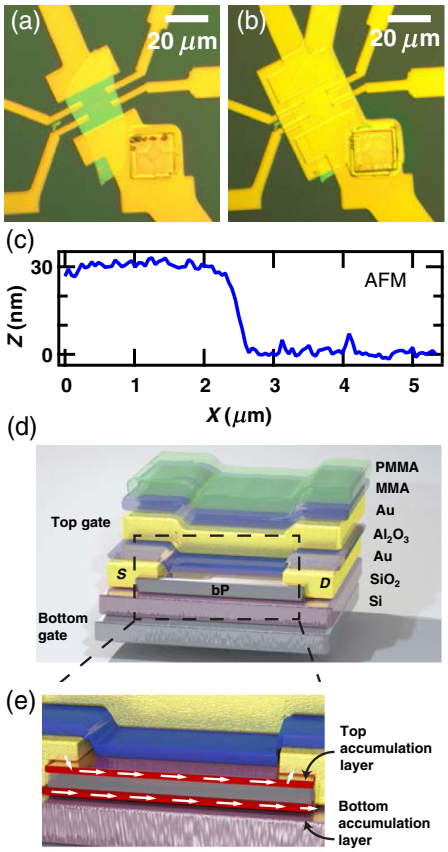

FIG. 1. (a) Optical image of a bP FET in a multiple-terminal geometry prior to top-gate deposition. Scale bar is 20 μm. (b) Optical image of the device shown in (b) including top-gate and methylmethacrylate (MMA) and poly(methylmethacrylate) (PMMA) encapsulation. Scale bar is 20 μm. (c) Atomic-force-microscope (AFM) line scan of a region of bare bP/Al_2O_3 of the device in (b), with the MMA and PMMA layers removed. (d) Schematic view of a dual-gate bP FET with SiO_2 back-gate, Al_2O_3 top-gate dielectric, source (S) and drain (D) contacts, and encapsulating layers of MMA and PMMA. (e) Schematic view of the bP FET channel with top- and bottom-hole accumulation layers (red) providing two parallel conduction paths between source and drain.

Austria). The exfoliation is performed inside a nitrogen glovebox with O_2 and H_2O concentration below 5 ppm. The thin bP crystals are transferred to a degenerately doped Si wafer with a 300-nm-thick SiO_2 layer. The wafer is previously dehydrated at $T = 150\,°C$ under vacuum and functionalized with a hexamethyldisilazane (HMDS) layer. The hydrophobic HMDS layer aids in protecting the freshly cleaved surface of the bP from water adsorbates on the SiO_2 surface and suppresses charge-transfer doping that will otherwise lead to hysteresis and instability in FET characteristics [26]. Further microfabrication is performed to define contact electrodes, a top-gate structure, and final encapsulation. Electrodes contacting the bP are defined using standard electron-beam lithography (EBL) followed by 5-nm Ti and 80-nm Au metal deposition. A top-gate dielectric layer of 25-nm Al_2O_3 is deposited atop the bP by atomic-layer deposition (ALD) at 150 °C through an EBL-defined window. A top-gate metal layer is defined by a further EBL step followed by metal deposition (5 nm Ti and 80 nm Au). The final encapsulation step is to spin coat the samples with 300 nm of copolymer (methyl methacrylate) and 200 nm of polymer (polymethyl methacrylate).

An optical image of a typical bP FET in a multiple-terminal geometry is shown in Fig. 1(a) prior to top-gate fabrication and in Fig. 1(b) after top-gate fabrication. After all electronic characterization described further below, the encapsulating polymer layers are removed with warm acetone and AFM is performed within a glovebox environment. The thickness of the bP layer under the top gate of the bP FET is determined to be 32 nm by atomic force microscopy, as shown in Fig. 1(c). A schematic of the complete bP FET structure is displayed in Fig. 1(d). Encapsulating the bP layer between a HMDS functionalized SiO_2 on Si substrate and an optically opaque gate stack is found to effectively mitigate degradation due to photo-oxidation. The I-V characteristics of our bP FETs are stable over a period of six months. An important aspect of the dual-gate bP FET is the capacity for the top and bottom gates to each induce hole accumulation layers at the top and bottom surfaces of the bP channel, respectively, as shown in Fig. 1(e). The source and drain electrodes electrically contact both accumulation layers, with the top surface metallization expected to lead to lower contact resistance to the top accumulation layer than the bottom. Also important for the operation of the dual-gate bP FET studied here is the asymmetry in conductance between the top- and bottom-hole accumulation layers.

III. CHARGE-TRANSPORT MEASUREMENTS

Charge-transport measurements are performed using quasi-dc excitation with a semiconductor parameter analyzer and vacuum probe station ($P \sim 10^{-4}$ Torr) at room temperature. Figure 2 shows the I-V characteristics of the device shown in Fig. 1. The measured two-terminal source-drain current I versus source-drain bias voltage V_{SD} is plotted in Fig. 2(a) with 0 V applied to the top and bottom gates. The linear I-V_{SD} characteristic indicates Ohmic or quasi-Ohmic behavior of the contact electrodes. The two-terminal conductance G_{2p} as a function of top-gate voltage V_{TG} is plotted in Fig. 2(b) demonstrating strong conductance modulation consistent with electron conduction and a negligible hysteresis. Gate-leakage currents are recorded simultaneously in all of our charge-transport experiments, never exceeding 5% of the source-drain current and generally being much lower than the source-drain current. The two-terminal conductance G_{2p} at a constant bias current of 4 μA as a function of back-gate voltage V_{BG} is plotted in Fig. 2(c) with top-gate voltage held at $V_{TG} = -4$, 0, and +4 V. The room-temperature conductance modulation reaches 2 orders of magnitude, and there is minimal

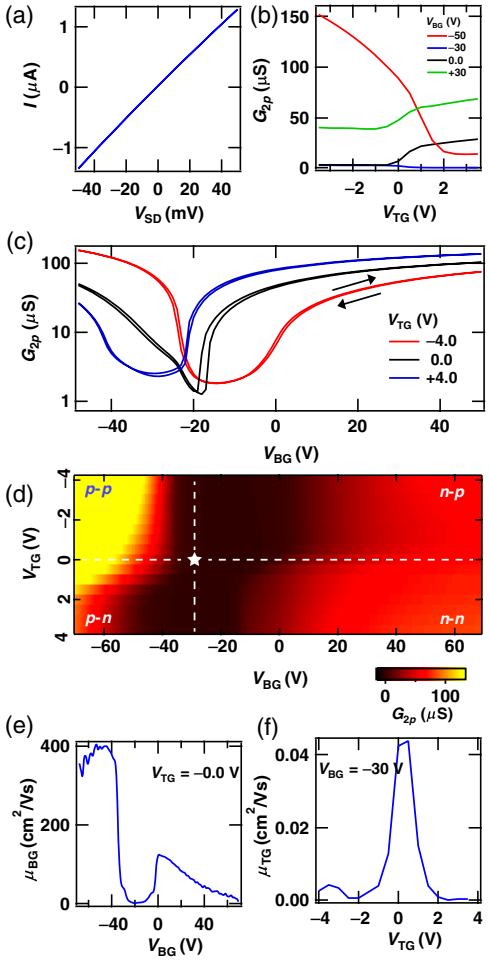

FIG. 2. (a) Source-drain current I as a function of the source-drain voltage V_{SD} with bottom-gate and top-gate biases of $V_{TG} = 0$ V and $V_{TG} = 0$ V indicative of Ohmic contacts. (b) Two-terminal conductance G_{2p} as a function of top-gate voltage V_{TG} at fixed bottom-gate voltages $V_{BG} = -50$, -30, 0, $+30$ V. (c) Two-terminal conductance G_{2p} versus back-gate voltage V_{BG} at three top-gate voltages $V_{TG} = -4$, 0, $+4$ V at room temperature. Minimal hysteresis is observed at the 1 V/s sweep rate used for the back-gate potential. (d) Two-dimensional contour plot of two-terminal conductance G_{2p} versus gate voltages V_{TG} and V_{BG} at $T = 77$ K, for the same device. A bias point corresponding to minimal conduction and complete channel depletion located at $V_{TG} = 0$ V and $V_{BG} = -30$ V is indicated by a star symbol. Cuts of constant top-gate voltage and constant bottom-gate voltage used to determine field-effect mobility are shown. (e) The absolute value of bottom-gate field-effect mobility μ_{BG} versus V_{BG} at $V_{TG} = 0$ V. (f) The absolute value of top-gate field-effect mobility μ_{TG} versus V_{TG} at $V_{TG} = -30$ V.

hysteresis in conductance as back-gate voltage is swept at a rate of ± 1 V/s, which we attribute to the HMDS functionalization of the oxide layer below the bP. The threshold voltages for the onset of electron and hole conduction are modulated by the applied top-gate potential. An increasingly negative top-gate voltage results in increased back-gate threshold voltages for both electron and hole conduction, as expected.

We investigate the dependence of the bP FET conductance as a function of both top- and bottom-gate voltages, with the goal of quantifying the conduction properties of the top- and bottom-hole accumulation layers. A standard ac lock-in measurement technique is used to measure the FET conductance at a bias current $I_{SD} = 1$ μA and a frequency $f = 13.013$ Hz at $T = 77$ K in a liquid nitrogen cryostat. The measured two-point conductance G_{2p} is plotted in Fig. 2(d) as a color contour versus both V_{TG} and V_{BG}. Note that the capacitance ratio $C_{TG} : C_{BG} = 25$, so that $V_{TG} = 2$ V induces the same charge density at the top of the bP well as $V_{BG} = 50$ V induces at the bottom of the bP well. An insulating region (dark) is visible in the contour plot corresponding to minimal mobile carrier density within the bP channel. With $V_{BG} < 0$ V and $V_{TG} < 0$ V, both gate potentials induce holes within the bP to result in strong hole conduction identified as p-p in Fig. 2(d). In contrast, with $V_{BG} > 0$ V and $V_{TG} > 0$ V, both gate potentials induce electrons and electron conduction is unambiguously observed, identified as n-n. The top-gate voltage can also be used to induce an opposite carrier type to that induced by the bottom gate, identified as p-n and n-p in Fig. 2(d).

The top-gate potential influences the back-gate threshold voltage for both hole and electron conduction over a narrow range -2 V $< V_{TG} < 2$ V, beyond which the top-gate voltage has comparatively little influence upon the channel conductance. The inability of the top gate to induce electron or hole conduction over the back-gate voltage range -40 V $< V_{BG} < -10$ V indicates that the charge carriers induced by the top gate are of very low mobility and may, to a large extent, be localized at charge traps. The strongly asymmetric conductance behavior versus top- and bottom-gate potential can be further quantified. We identify in Fig. 2(d) a point of minimal channel conduction at $V_{TG} = 0$ V and $V_{BG} = -30$ V. At this bias point, the bP layer is depleted of charge carriers. The independent action of the bottom gate to induce conduction in the channel from this depleted insulating state (at $V_{TG} = 0$ V and $V_{BG} = -30$ V) is a measure of the conduction in the bottom accumulation layer. Likewise, the independent action of the top gate to induce conduction in the channel from this depleted insulating state (at $V_{TG} = 0$ V and $V_{BG} = -30$ V) is a measure of the conduction in the bottom accumulation layer.

The approximate bottom-gate field-effect mobility $\mu_{BG} = \partial G_{2p}/\partial(C_{BG}V_{BG})$ versus bottom-gate voltage V_{BG} at fixed top-gate voltage $V_{TG} = 0$ V is plotted in Fig. 2(e), where $C_{BG} = 11.5$ nF/cm^2 is the bottom-gate capacitance. A peak mobility of 400 cm^2/Vs is observed. This field-effect mobility is a measure of conduction in the bottom accumulation layer induced by the bottom gate out of a depleted channel. A more accurate determination based on four-point probe measurements is discussed further below.

The approximate top-gate field-effect mobility $\mu_{TG} = \partial G_{2p}/\partial(C_{TG}V_{TG})$ versus top-gate voltage V_{TG} at fixed bottom-gate voltage $V_{BG} = -30$ V is plotted in Fig. 2(f), where $C_{TG} = 280$ nF/cm^2 is the top-gate capacitance. A peak mobility of <0.1 cm^2/Vs is observed. This field-effect mobility is a measure of conduction in the top accumulation layer induced by the top gate out of a depleted channel. Noting the capacitance ratio $C_{TG}:C_{BG} = 25$, the top-gate voltage range probed is adequate to induce accumulation in the bP channel. In summary, the bottom gate is much more effective in inducing conduction within the depleted channel than the top gate.

The origin of the asymmetry between top and bottom surfaces may be caused by the Al_2O_3 atomic-layer deposition process, which takes place under strongly oxidative conditions that may lead to the formation of charge traps and scattering centers at the top bP surface. The asymmetric behavior of the asymmetric dual-gate bP FET is distinct from the symmetric behavior of symmetric dual-gate bP FETs [27]. Under these strongly asymmetric conditions, conduction is dominated by the bottom accumulation layer. The top-gate potential and the charge carriers induced by the top gate are, nonetheless, found to influence the conduction properties of charge carriers induced within the bottom accumulation layer.

IV. SCHRÖDINGER-POISSON ANALYSIS

Self-consistent Schrödinger-Poisson calculations combining an effective mass theory for bP and a mean-field approximation to Coulomb interactions are employed to gain further insight into the behavior of the dual-gated bP FET. Effective masses for bulk bP determined by cyclotron resonance experiments [28] are used in our calculations. The band diagram and volumetric hole density with the bP layer are shown in Fig. 3(a) at $T = 300$ K for a negative back-gate voltage and positive top-gate voltage adjusted to induce a total hole density of $p_{BG} = 10^{12}$ cm^{-2} and a total electron density $n_{TG} = 10^{12}$ cm^{-2}. The rms thickness of the hole accumulation layer is 3.5 nm. Under these bias conditions, a *p-n* junction is formed vertically within the bP layer, with holes (electrons) confined at the bottom (top) of the bP. If conduction is strongly suppressed at the top surface due to ALD processing, hole conduction in the bottom accumulation layer will dominate the contribution to total channel conduction. Moreover, the top-gate potential is screened by the electrons within the inversion layer at the top surface, as observed in our experimental data with $V_{TG} > 2$ V. The band diagram and volumetric hole density are shown in Fig. 3(b) at $T = 300$ K with gate voltages adjusted to induce a total hole density of $p_{BG} = 10^{12}$ cm^{-2} and flat bands at the top surface. The holes are less tightly confined to the bottom of the bP layer under these conditions. The top-gate voltage is no longer screened by induced electrons and will, therefore, modulate the threshold

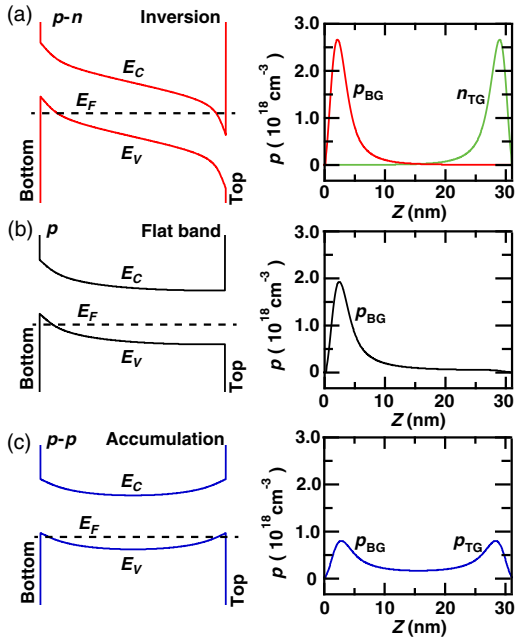

FIG. 3. The band diagrams and volumetric charge-density distribution in a 32-nm-wide bP quantum well determined by Schrödinger-Poisson calculations at $T = 300$ K for different gate-bias potentials. (a) Asymmetric gate bias inducing a *p-n* carrier distribution with $p_{BG} = n_{TG} = 10^{12}$ cm^{-2} and an associated inversion in carrier type. (b) Gate bias inducing $p_{BG} = 10^{12}$ cm^{-2} at one bP surface and flat-band conditions at the other. (c) Symmetric gate bias inducing a *p-p* carrier distribution with a total hole concentration of $p_{BG} + p_{TG} = 10^{12}$ cm^{-2} corresponding to hole accumulation at both bP surfaces.

back-gate voltage for the onset of hole conduction, as observed in our experiments for -2 V $< V_{TG} < 2$ V. The band diagram and volumetric hole density with the bP layer are shown in Fig. 3(c) at $T = 300$ K for negative back-gate and top-gate voltages adjusted to induce a total hole density of $p_{BG} + p_{TG} = 10^{12}$ cm^{-2} distributed symmetrically within the structure. The top-gate potential is screened from influencing the hole density at the bottom of the bP layer, and the volumetric hole density extends within the bulk of the bP layer. At the hole density $p = 10^{12}$ cm^{-2} used for our calculations, the Fermi temperature $T_F = p/(k_B m^*/\pi\hbar^2) = 126$ K for holes accumulating within a single 2D subband. Analysis of the 2D subband population reveals that two 2D subbands are substantially populated for the carrier densities accessed in our calculations, leading to nondegenerate carrier statistics at room temperature.

V. TRANSISTOR PARAMETER ANALYSIS

The transistor parameters of the bP FET are investigated in greater detail at $T = 300$ K. Figure 4 (a) shows the two-terminal back-gate transconductance $g_m = \partial I_{SD}/\partial V_{BG}$ plotted versus the mobile hole density $p_{BG} = C_{BG}(V_{BG} - V_{th})/e$ induced by the back-gate voltage, with a threshold

voltage $V_{\rm th}$ that is dependent upon top-gate voltage. The threshold voltage $V_{\rm th}$ for the hole conduction in the bottom accumulation layer is readily found because the total channel conduction is dominated by the bottom accumulation layer. The top-gate voltage is found to strongly modulate the back-gate transconductance at a fixed hole density. We measure the four-point conductance G_{xx} in our multiterminal bP FET. The field-effect mobility extracted from four-point conductance $\mu_{4p} = \partial G_{xx}/\partial(C_{\rm BG}V_{\rm BG})$ is plotted in Fig. 4(b) versus the induced hole density $p_{\rm BG}$.

At low hole densities $p_{\rm BG} < 4 \times 10^{11}$ cm^{-2}, the mobility increases as expected from the onset of percolation in the vicinity of the conduction threshold. At high hole densities $p_{\rm BG} > 8 \times 10^{11}$ cm^{-2}, the hole mobility falls with increasing carrier density, consistent with surface roughness scattering [29,30]. The hole mobility is also modulated

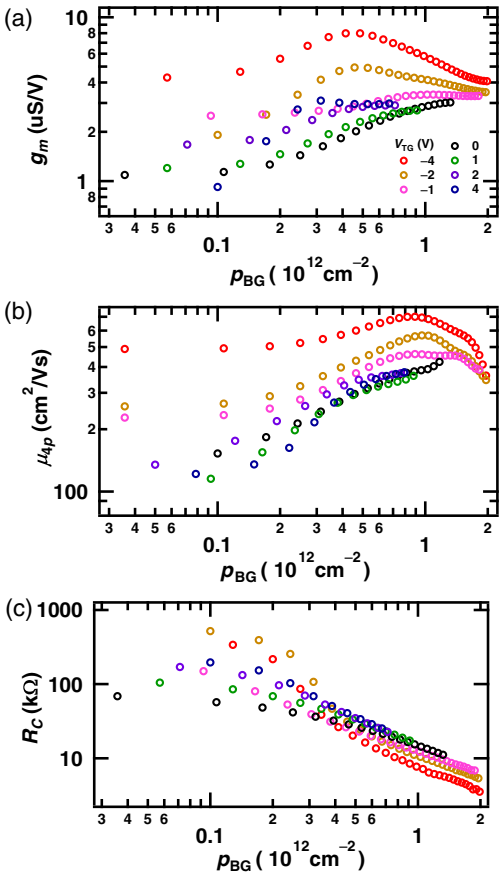

FIG. 4. (a) The measured two-terminal back-gate transconductance g_m of the device shown in Figs. 1 and 2 as a function of hole density $p_{\rm BG}$ induced by the back gate, at fixed top-gate voltages $V_{\rm TG}$ at $T = 300$ K. A fourfold enhancement of two-terminal g_m is observed as $V_{\rm TG}$ is tuned from 0 to −4 V. (b) The field-effect mobility μ_{4p} of the same device on a log-log scale versus $p_{\rm BG}$ at fixed top-gate voltages at $T = 300$ K. A twofold enhancement in mobility is achieved by tuning the top-gate potential. (c) The contact resistance R_C of the same device versus $p_{\rm BG}$ at fixed top-gate voltage. A twofold modulation in contact resistance is observed as the top-gate voltage is tuned.

up to twofold by the top-gate voltage, with maximum mobility of 780 cm^2/Vs reached at $V_{\rm TG} = -4$ V, the most negative top-gate voltage applied in our experiments and $V_{\rm BG} = -25$ V corresponding to a hole density of $p_{\rm BG} = 8 \times 10^{11}$ cm^{-2}. From our Schrödinger-Poisson calculations at comparable hole density, we can infer that a negative top-gate potential induces a hole accumulation layer at the top of the bP layer and that the volumetric hole density is spread throughout the bP layer. The hole accumulation layer induced at the top of the bP layer may contribute to the screening of trapped charge, reducing charged impurity scattering and enhancing mobility for holes within the bulk of the bP. The screening of trapped charge and the concomitant increase of carrier mobility has been previously observed in bP by introduction of a graphene layer in close proximity to the bP layer, by which means that significantly enhanced bP hole mobility has been observed [16].

From the sample geometry and the combined measurement of two-point conductance G_{2p} and four-point conductance G_{xx}, the contact resistance R_C is determined and plotted in Fig. 4(c) versus the mobile hole density $p_{\rm BG}$. As anticipated, the contact resistance to the hole gas within the bP layer decreases monotonically as the hole density within the bP layer increases. In addition to this expected trend, the top-gate potential is found to be effective at modulating the contact resistance at a fixed hole density. The top-gate electrode is an ideal place for efficient electrostatic coupling to the region of carrier injection from the contact electrode to the bP layer, as seen in Fig. 1. Our measurements of the contact resistance are in accordance with the electrostatically gated Schottky-barrier model that has been successfully employed in the study of carbon nanotubes [24], ultrathin body silicon FETs, and bP FETs [25] in two-point geometry. Unlike these previous studies, the effect of charge carrier distribution upon carrier injection into a low-dimensional FET channel is directly observed.

VI. CONCLUSIONS

The observation of mobility modulation effects in dual-gate bP FETs demonstrates the capacity for bP to function as a room-temperature VMT. The velocity-modulation effect thus far remains too weak to act as the primary means of transistor channel conductance modulation for practical applications. However, our observation of a maximum back-gate field-effect mobility under a nonzero top-gate bias clearly shows that externally applied fields can optimize transistor behavior via the velocity-modulation effect. Charge-density distribution, thus, plays an important role in the charge-transport properties of 2D atomic crystals. The exposed surfaces of naked quantum-well structures derived from 2D atomic crystals can lead to a strong spatial dependence of charge carrier scattering rates.

In the specific case of bP, the band-gap range accessible by quantum confinement is ideal for applications in

electronics, thermoelectrics, and optoelectronics [3]. Velocity-modulation effects similar to that reported here are expected to be significant for bP devices that are thicker than the charge accumulation layer thickness, but further experimental work is required to understand the role of applied electric field on charge transport in thinner bP devices that approach the monolayer limit. Band-gap tuning of bP by a giant Stark effect [31] and by hydrostatic pressure [2,32] is also demonstrated, leading to a transition from a direct-gap semiconductor to Dirac semimetal in the extreme limit. The engineering of charge carrier distribution and confinement by externally applied potentials within thin bP layers adds a means by which to tune and design bP quantum-well device properties.

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