Electro-Photo-Sensitive Memristor for Neuromorphic and Arithmetic Computing

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We present optically and electrically tunable conductance modifications of a site-controlled quantum-dot memristor. The conductance of the device is tuned by electron localization on a quantum dot. The control of the conductance with voltage and low-power light pulses enables applications in neuromorphic and arithmetic computing. As in neural networks, applying pre- and postsynaptic voltage pulses to the memristor allows us to increase (potentiation) or decrease (depression) the conductance by tuning the time difference between the electrical pulses. Exploiting state-dependent thresholds for potentiation and depression, we are able to demonstrate a memory-dependent induction of learning. The discharging of the quantum dot can further be induced by low-power light pulses in the nanowatt range. In combination with the state-dependent threshold voltage for discharging, this enables applications as generic building blocks to perform arithmetic operations in bases ranging from binary to decimal with low-power optical excitation. Our findings allow the realization of optoelectronic memristor-based synapses in artificial neural networks with a memory-dependent induction of learning and enhanced functionality by performing arithmetic operations.

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I. INTRODUCTION

In the human brain the interconnection of neurons via synapses results in a massively parallel computational network [1]. Synapses, the connections between neurons, are constantly formed or eliminated [2,3] and learning is associated with the modification of their strength that regulates the transmission of action potentials [4]. This modification is controlled by the superposition of action potentials generated by pre- and postsynaptic neurons. According to the model of spike-timing-dependent plasticity (STDP), the relative timing of pre- and postsynaptic spikes is crucial for dynamic potentiation or depression [5–8]. In neural networks, neuronal activities do not necessarily result only in changes of synaptic strength, but they also result in a varying capability for the induction of potentiation or depression [9,10], which ensures intrinsic convergence of synaptic strength [11]. Recently, STDP was demonstrated with memristors [12–15] and interconnecting memristors with neurons, STDP-based learning rules can be emulated in self-learning visual cortices [16]. The memory resistance (memristance) of memristors [17,18] can originate from different physical mechanisms such as self-heating, chemical reactions, ionic transfer, spin polarization, or phase transitions [19]. In addition, a memristive operation mode was observed for floating-gate transistors wired as diode-connected transistors [20,21]. Floating-gate transistors are nonvolatile memories based on field-effect transistors that store information by means of localized charge on an additional gate located between the channel and the control gate [22,23]. Silicon-based floating-gate transistors are used in commercially available nonvolatile flash memory devices such as USB memory sticks and solid-state hard drives. Current Si-based devices with feature sizes of 20 nm show room-temperature retention times of more than ten years, and write and access times of about 1 μs and 10 ns, respectively [24]. Novel approaches in the design of these memory devices, e.g., a three-dimensional layout similar to the tri-gate transistor, further tend to push their feature size limits and thus aims to keep track with Moore's law [25]. However, silicon is an indirect band-gap semiconductor, which makes it impracticable for optical applications. Thus device concepts based on low dimensional direct band-gap semiconductors are especially appealing for an optical and electrical control of charge or spin states. Here, quantum-dot structures based on III-V-semiconductor materials with their atomlike energetic structure in combination with a direct band gap enable optoelectronic applications such as lasers [26], single photon sources [27], entangled-light-emitting diodes [28], spin memories [29,30], and floating-gate transistors [31]. Realizing STDP on a state-of-the-art optoelectronic semiconductor platform would thus allow the realization of electro-photo-sensitive artificial synapses and brain-inspired computing with optical interconnects.

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Here we present an electro-photo-sensitive memristor suitable for neuromorphic and arithmetic computing. The conductance of the device emerges from different amounts of quantum-dot (QD-)localized charges which can be controlled and altered by electrical and low-power optical pulses. Applying nature-inspired voltage pulses to emulate the action potentials of pre- and postsynaptic neurons, the conductance of the device is raised (potentiation) or lowered (depression) by changing the time difference between the onsets of the pulses. We further observe a dependence of the conductance change on the initial state, which was set by the past biasing procedure. Thus, previous input pulses are memorized and the capability for the induction of learning changes accordingly. Finally, we demonstrate an optical control of the memristance. Combining the optical tunability with the state-dependent threshold for potentiation, the device is a basic component for the realization of arithmetic operations with low-power optical pulses.

II. DEVICE LAYOUT

Figure 1(a) shows a scheme of the device, which is based on a GaAs/AlGaAs heterostructure with precisely positioned InAs QDs (highlighted in green). The fabrication process is described in detail in Ref. [32]. The memristive operation is realized by short circuiting the source with the gate contacts [see Fig. 1(b)] [20,21]. This wiring scheme is known as the diode-connected transistor and can, for example, be used as temperature sensor [33]. In our case, the transistor is a quantum-dot floating-gate transistor. In analogy to synapses in neural networks, where the plasticity is controlled by the action potentials of pre- and postsynaptic neurons, we apply two independent voltage pulses labeled as pre- and postsynaptic pulses to the two terminals of the device. The voltages V_{pr} and V_{po} are applied to the drain and source contacts, respectively [see Fig. 1(b)]. The current I is measured as voltage drop across a resistor with $R = 1\ \mathrm{M}\Omega$ in series to the channel. All measurements are conducted at 4.2 K.

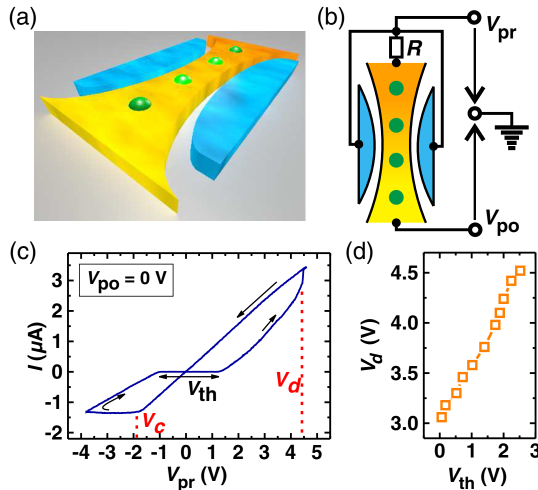

FIG. 1. (a) Scheme of the memristor. The positions of the QDs are highlighted in green. (b) Circuit diagram of the memristor. V_{pr} is applied to the top contact of the wire and the lateral gates. V_{po} is applied to the bottom contact of the wire. (c) Current-voltage characteristic of the device. V_c and V_d are the threshold voltages for charging and discharging, respectively. (d) Linear dependency between the discharging voltage and V_{th}.

III. MEMRISTOR CHARACTERISTICS

Figure 1(c) depicts the current-voltage characteristic of the device. A closed voltage sweep of the voltage applied to the drain and gate contacts between −3.8 and 4.6 V shows a pinched hysteresis loop, the fingerprint of memristors [34]. The low and high conductance values between −1 and 1 V are explained by different amounts of QD-localized electrons n with more charges corresponding to the smaller conductance. V_{th} is the width of the plateau with almost zero conductance and is linear dependent on the amount of localized electrons [21]. The QD becomes charged for voltages below $V_c \approx -1.9$ V ($\Delta n > 0$) and discharged above $V_d \approx 4.4$ V ($\Delta n < 0$). In Fig. 1(c), V_c and V_d are highlighted with the red vertical lines. Hence, the conductance of the device is altered by changing the amount of QD-localized charges which depends sensitively on the time and the voltage value spent above the discharging or below the charging voltage.

The pinched hysteresis loop can be analyzed by the width V_{th} of the plateau with almost zero conductance [21]. Figure 1(d) displays the discharging voltage in dependence on V_{th}. V_{th} is increased by reducing the minimum bias voltage during the voltage sweep cycle in Fig. 1(c). Lower minimum voltages lead to more localized electrons and enhanced V_{th} [21]. A linear increase of V_d is observed for raising V_{th}. Strukov *et al.* explained the dependency of the threshold voltage on the state of the memristor with nonlinearities in ion movements [35]. Here, we describe the shift of the discharging voltage by means of a charge-dependent gate efficiency. Charging the QD with electrons lowers the gate-channel capacitance. The quantum-dot charge-dependent gate-channel capacitance emerges from the depletion of the channel via localized electrons on the quantum dot which effectively leads to a variable effective gate-channel distance with different charge accumulation interfaces. Thus, discharging the QD leads to larger capacitances. Controlling the amount of localized charge with the lateral gates, a hysteresis in the capacitance-voltage curve is evident, which is the fingerprint of memcapacitors [19,36]. For reduced capacitances, larger absolute gate voltages are required to shift the potentials of the QD and the two-dimensional electron gas by the same energy. Thus, the charging and discharging voltages are reduced and increased, respectively.

For excitation with constant parameters (voltage range, sweep time), the pinched hysteresis loop as well as the

threshold voltages V_d and V_c are highly reliable even after many voltage and temperature cycles with small deviations in the threshold voltages for charging and discharging in the order of 50 mV. The energy-barrier height surrounding the floating gate, around 0.4 eV for the presented device, is significantly lower compared to silicon-based floating-gate transistors (3.2 eV) which leads to small retention times of several days at 4.2 K and stable pinched hysteresis loops up to temperatures of about 165 K [21]. Room temperature operation may be possible by tuning the material composition of the III-V compound semiconductors representing the QD and the surrounding matrix [31]. On the other hand, the reduced barrier height enables faster write and erase times and smaller operation voltages. A particular advantage of III-V-semiconductor-based compared to Si-based floating-gate devices is the tunability of the energy barrier by changing the material composition. This may enable the realization of fast write times and room-temperature retention times comparable to Si-based devices [31].

IV. SPIKE-TIMING-DEPENDENT PLASTICITY

Two function generators are used to emulate the voltage pulses in Fig. 2(a), that are applied to the two terminals of the device [see Fig. 1(b)]. The general shape of the pulses is chosen to mimic an action potential measured in the axon of a squid [37]. Simple rectangular pulses are not used, because they only enable us to either emulate potentiation or depression with a single set of pulses [21]. However, the transition from potentiation to depression solely triggered by the timing of the pulses is essential to mimic STDP and requires pulse shapes with positive and negative amplitudes. These pulse shapes allow us to change the voltage difference across the memristor from negative to positive by inverting the temporal order of the two pulses. Thus, charging or discharging of the QD can be induced depending on the order of the pulses. Because of the asymmetric charging and discharging voltages of the device, at least one pulse needs to be asymmetric. Thus, we used amplitudes of (+4.2, −3.1) and (+2.0, −2.0) V for V_{pr} and V_{po}, respectively. The pulse widths are 10 ms. The time difference Δt between the pulses is the crucial parameter of STDP. Here, the postsynaptic pulse is applied after the presynaptic pulse for positive time differences and vice versa.

For the present device, the performance is mainly governed by the voltage difference $V_{\mathrm{pr}} - V_{\mathrm{po}}$ between the two terminals. Depending on Δt, the temporal voltage difference can exceed the threshold voltages for charging and discharging [see red highlighted areas in Fig. 2(b)] for their respective times T_c and T_d. These time intervals depend on Δt, i.e., $T_c(\Delta t)$ and $T_d(\Delta t)$, as sketched in Fig. 2(c). For simple rectangular pulses, either T_c or T_d would be zero and independent on Δt. Thus, tuning the time difference does not allow the observation of a transition from depression to potentiation. For the pulses in Fig. 2(a), the dominant processes are charging (highlighted in yellow) for negative and discharging (highlighted in green) for positive time differences. The time-dependent tunneling from the two-dimensional electron gas to the QD (charging) and from the QD to the two-dimensional electron gas (discharging) can be described by a capacitor model [38]. The dependency of n on T_c and T_d is given by

$$n(\Delta t) = n_0 + n_+\left\{1 - \exp\left[\frac{-T_c(\Delta t)}{\tau_c}\right]\right\} - n_-\left\{1 - \exp\left[\frac{-T_d(\Delta t)}{\tau_d}\right]\right\}. \quad (1)$$

n_0 is the initial amount of QD-localized charges. The second and third term of Eq. (1) represent charging and discharging characteristics with time constants τ_c and τ_d, respectively. n_+ and n_- are constants that represent the total amount of transferred charges.

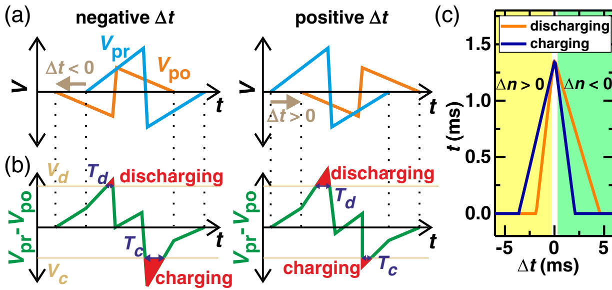

FIG. 2. (a) Scheme of pulse trains for negative (left) and positive (right) time differences Δt. The different voltages are applied to the two terminals of the memristor. Depending on Δt, $V_{\mathrm{pr}} - V_{\mathrm{po}}$ can exceed V_c and V_d [highlighted in red in (b)]. The time intervals in the charging and discharging regions versus Δt are shown schematically in (c). For positive and negative time differences, the QD is discharged (green area) and charged (yellow area), respectively.

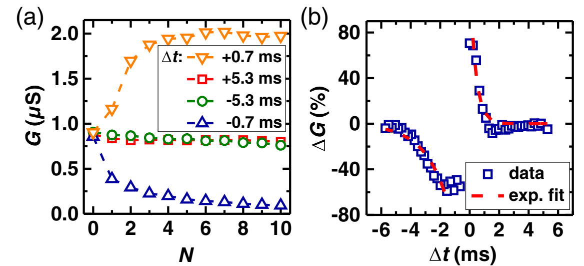

FIG. 3. (a) Conductance versus number of applied pulses for different Δt. G remains almost unaltered for large time differences ($\Delta t = \pm 5.3$ ms), but decreases and increases for $\Delta t = -0.7$ and $+0.7$ ms, respectively. (b) Relative conductance change versus Δt. In the interval of $\Delta t = \pm 4$ ms, ΔG can be tuned efficiently and either depressed or potentiated depending on the sign of Δt.

Figure 3(a) shows the conductance of the memristor versus the number of applied pulses N for different Δt. Here, one pulse is defined as the pair of the pulses depicted in Fig. 2(a). Ten consecutive pulses are applied for constant time differences. Each pulse is followed by a readout pulse with amplitude 2.8 V and width 5 ms to determine the conductance G. For large time differences (± 5.3 ms), the conductance remains almost unaltered up to ten pulses. Smaller time differences lead to an increase and decrease of the conductance with N for $+0.7$ and -0.7 ms, respectively. These observations are due to changes in the voltage difference across the memristor as a function of Δt. Varying time differences lead to different time intervals $T_c(\Delta t)$ and $T_d(\Delta t)$. For $\Delta t = \pm 5.3$ ms, they are almost zero and thus $T_d/\tau_d \approx 0$ and $T_c/\tau_c \approx 0$. Consequently, the amount of QD-localized charges in Eq. (1) remains unaltered with $n(\Delta t) \approx n_0$ and $\Delta n \approx 0$. For $\Delta t = \pm 0.7$ ms, the temporal signal exceeds the threshold voltages for times T_c and T_d greater than zero [see Fig. 2(c)]. For negative Δt, the charging dominates over the discharging process with $T_c/\tau_c > T_d/\tau_d$, and the QD becomes charged with additional electrons [see Eq. (1)]. Discharging the QD dominates for positive time differences.

To explain the influence of the amount of QD-localized charges on the conductance, we use the current-voltage characteristic of a floating-gate transistor

$$I = \beta(V_g - V_{tu})V_b - \beta\frac{V_b^2}{2}, \tag{2}$$

with V_g and V_b being the gate and bias voltages, respectively, V_{tu} the threshold voltage, and β the transconductance [20]. Charging the floating gate (here: QD) with electrons shifts V_{tu} of the nearby transistor with $V_{tu} = ne/C$ (e represents elementary charge, C represents QD-gate capacitance) towards larger values [39]. Additionally the carrier density and the conductance of the transistor are reduced for larger n [40]. In the memristive operation mode we have $V_g = V_{\mathrm{pr}}$ and $V_b \leq V_{\mathrm{pr}}$. Hence, the second term in Eq. (2) can be neglected. With $V_{tu} = ne/C$ it follows that the conductance $G = I/V_b \propto ne/C$ is linearly dependent on the amount of QD-localized charges which in turn can be altered by the times spent in the charging and discharging regions [see Eq. (1)]. Applying N consecutive pulses, the conductance change is

$$G_N(\Delta t) - G_0 \propto -n_+\left\{1 - \exp\left[\frac{-NT_c(\Delta t)}{\tau_c}\right]\right\} + n_-\left\{1 - \exp\left[\frac{-NT_d(\Delta t)}{\tau_d}\right]\right\}. \tag{3}$$

G_0 is the initial conductance and G_N is the conductance after applying N pulses. For negative and positive time differences we have $T_c(\Delta t)/\tau_c > T_d(\Delta t)/\tau_d$ and $T_c(\Delta t)/\tau_c < T_d(\Delta t)/\tau_d$, respectively. Thus, for a given time difference, one term is negligible leading to the exponential decline of $G_N - G_0$ for $\Delta t = -0.7$ ms and the exponential increase for $\Delta t = +0.7$ ms [see Fig. 3(a)].

Figure 3(b) shows the relative conductance change after a single pulse $\Delta G = (G_1 - G_0)/G_0$ versus Δt. For each measurement, G_0 is set to 0.8 μS prior to the first pulse [see Fig. 3(a)]. The relative conductance change depends exponentially on the time difference and can be tuned efficiently within a time interval of about 4 ms. Thus, the relative conductance change is zero for large magnitudes of the time difference. The experimental data for positive and negative time differences can be fitted with single exponential fit functions $A\exp(\Delta t/\tau)$ [see Eq. (3)]. The parameters are $A = 130\%$ and $\tau = -0.4$ ms for positive and $A = 175\%$ and $\tau = 1.6$ ms for negative time differences. The different time constants for charging and discharging (see Ref. [38]) result in a broader time window for depression than for potentiation.

V. STATE-DEPENDENT PLASTICITY

The conductance change of the memristor depends not only on the timing of the voltage pulses, but also on the initial conductance value G_0 as shown in Fig. 4. Figures 4(a) and 4(b) illustrate the conductance versus N for various G_0 and time differences of $+0.9$ and -1.1 ms, respectively. The amplitudes of the voltage pulses are $(+4.2, -2.8)$ V for V_{pr} and $(+2.0, -2.0)$ V for V_{po}. Again, the conductance increases and decreases for positive and negative time differences, respectively. Consequently, the conductance change after one pulse $G_1 - G_0$ versus G_0

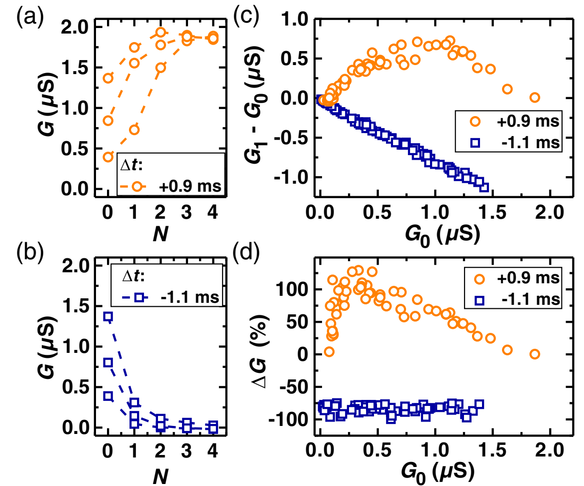

FIG. 4. (a) G versus N for different initial conductance values G_0 and time difference of $+0.9$ ms. (b) Conductance versus pulse number for different G_0 and $\Delta t = -1.1$ ms. (c) $G_1 - G_0$ for potentiation ($\Delta t = +0.9$ ms) and depression ($\Delta t = -1.1$ ms). $G_1 - G_0$ decreases linearly for depression and shows a maximum for potentiation. (d) Relative conductance change versus G_0. ΔG is independent on G_0 for depression but can be modified over a large range for potentiation.

is positive (potentiation) for $\Delta t = +0.9$ ms and negative (depression) for $\Delta t = -1.1$ ms [see Fig. 4(c)]. While $G_1 - G_0$ decreases linearly for depression, it shows a nonlinear response with a maximum at 1 μS for potentiation. The initial conductance corresponds to an initial amount of QD-localized charges n_0 and thus controls the threshold voltages for charging and discharging [as shown in Fig. 1(d) for V_d]. For decreasing n_0 (corresponds to increasing G_0), the discharging voltage is lowered and the charging voltage is raised linearly because both are proportional to $n_0 e/C$. Thus, larger initial conductance values enhance the times T_d and T_c for constant bias voltages which in turn lead to larger absolute values of $G_1 - G_0$ [see Eq. (3)]. The proportionality between V_c and n_0 is directly reflected in the linear $G_1 - G_0$ (G_0) curve for a time difference of -1.1 ms. For potentiation, the linear increase is superimposed by a decline, which originates from the saturation of the conductance at the maximum value (discharged QD). In Eq. (3), n_- correspond to the number of electrons that tunnel out of the QD. This number is limited by n, i.e., $n_- \leq n$. For $G_0 > 1$ μS, the number of tunneling electrons equals n. Consequently, this number is reduced for increasing G_0 which according to Eq. (3) lowers the absolute conductance change.

Figure 4(d) presents the relative conductance change after a single pulse versus the initial conductance. ΔG is almost constant and independent on the initial conductance value for depression, but ranges from 0% to 120% for potentiation. Similar findings in hippocampal neurons showed relative changes of synaptic strength (absolute change divided by initial value) that depend on the initial strength for potentiation but are constant for depression, which is an important stability feature of STDP models [8,11]. The reason, therefore, is that the synaptic strength triggers postsynaptic activity, and thus a constant relative change for potentiation would cause infinite synaptic strengths. A dependency of the relative change on the initial strength prevents this positive feedback and ensures converging synaptic strengths [11]. With the relative conductance change dependent on the initial conductance value, memristor-based synapses thus allow prevention of the positive feedback in artificial neural networks, where the pulses are generated intrinsically by postsynaptic activities, and ensure converging conductances.

Conductance traces versus N for 200 consecutive pulse pairs are displayed in Fig. 5(a). In the following, pulse pairs of pre- and postsynaptic pulses with negative and positive time differences are labeled as depression and potentiation pulses, respectively. The data in Fig. 5(a) is measured by applying N_d depression pulses with time difference of -1 ms, followed by N_p potentiation pulses with time difference of $+1$ ms. The amplitude of V_{pr} is raised from 4.2 to 4.5 V to realize large positive-conductance changes. The curves represent $N_d = N_p = 5$, 10, and 20 from top to bottom. Since the conductance can be decreased

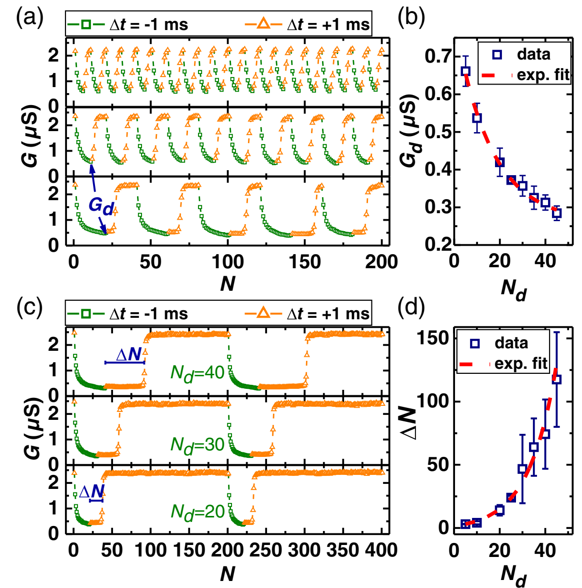

FIG. 5. (a) Conductance traces for 200 consecutive pulse pairs with alternating time difference. G is depressed and potentiated depending on the sign of Δt. The curves represent $N_d = N_p = 5$, 10, and 20 from top to bottom. (b) Conductance G_d after N_d depression pulses versus N_d. G_d decreases exponentially with increasing number of depression pulses. (c) Conductance traces for 400 consecutive pulse pairs with $N_p = 200 - N_d$. Applying N_d depression pulses requires ΔN pulses to raise G up to 50% of the maximum value. ΔN versus N_d shows an exponential dependency, as displayed in (d).

for negative and increased for positive time differences, it alternates periodically by inverting the temporal order of the pulses. The conductance value G_d after N_d depression pulses (before potentiation) shows an exponential decay versus N_d, as shown in Fig. 5(b). The dashed line represents the exponential fit function according to Eq. (3). The conductance reduction per pulse is lowered for larger N_d and thus many pulses are necessary to reduce G_d to zero. Information learned by previous potentiation is stored for a long time because of the intrinsic nonvolatile memory functionality of memristors. The storage capability enables long-term storage (several days at 4.2 K for the present device) of conductance values even for zero bias, which is advantageous compared to simple RC circuits that also show exponential conductance reductions.

Conductance traces for different numbers of depression and potentiation pulses $N_p = 200 - N_d$ are presented in Fig. 5(c) for 400 consecutive pulse pairs. The number of potentiation pulses ΔN to raise the conductance up to 50% of the maximum value increases for larger N_d (lower G_d). The exponential increase of ΔN versus N_d in Fig. 5(d) can be explained bearing in mind that the application of more depression pulses leads to an enhanced amount of QD-localized charges. Thus, the threshold voltage for discharging shifts towards larger values [see Fig. 1(d)]

and the time interval T_d for the consecutive potentiation is lowered. According to Eq. (3), more pulses are needed to compensate the reduction of T_d. This explains the exponential $\Delta N - N_d$ dependence as shown in Fig. 5(d). A correlation between the thresholds for potentiation and depression on the initial synaptic strength (here G_0) is also observed in the goldfish Mauthner cell [41]. Our findings of the $\Delta N - N_d$ dependence enables the implementation of a memory-dependent induction of learning. Here, the number of depression pulses controls the strength before potentiation is induced by learning. The increase of ΔN for large N_d (small initial strengths) implies that potentiation and thus learning is more effective for larger initial strengths, which corresponds to the memory of previous learning processes.

VI. OPTICAL CONDUCTANCE CONTROL

So far, the presented results may be reproducible with Si-based floating-gate transistors with advantages of reduced dimensionality, room-temperature operation, and CMOS compatibility [24]. The presented device is based on a GaAs/AlGaAs heterostructure and it is thus fully compatible with other III-V-based and state-of-the-art optoelectronic semiconductor devices. Because of its direct band gap, the material offers better absorption coefficients compared to similar silicon-based device realizations and hence allows to control the memristance by electrical and low-power optical pulses as shown in Figs. 6 and 7. For the optical excitation, a red light-emitting diode (LED) with wavelength $\lambda = 632$ nm is placed beside the device. The LED illuminates the whole device as illustrated in Fig. 6(a). No (shadow) masks with tunable transmission or microscope objectives are used to focus the light, which would be essential to control single devices in a network. The reported light powers correspond to the full LED emission power and are hence an upper limit of the light power that influences the device operation. Figure 6(b) depicts current-voltage characteristics under cw illumination. The LED is operated below the threshold voltage with output powers below 1 nW (the detection limit of our photosensor). For a

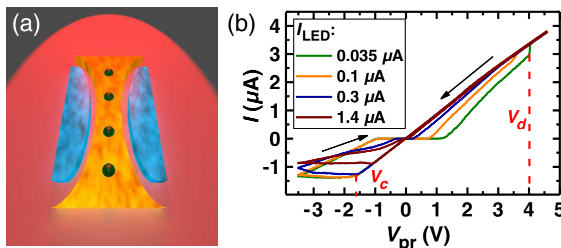

FIG. 6. (a) For optical excitation, the red LED is placed beside the device and illuminates the whole sample. (b) Current-voltage characteristics under cw illumination with light powers below 1 nW. The vertical red lines indicate the charging and discharging voltages for a LED current of 0.035 μA.

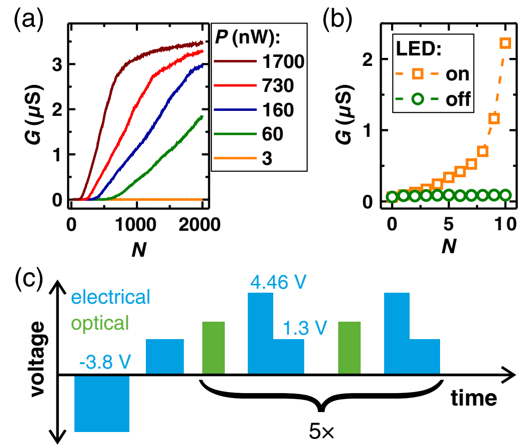

FIG. 7. (a) Conductance versus number of optical pulses with different light powers. (b) Conductance traces for 10 consecutive electrical pulses (LED, off) and pulse pairs of electrical and optical pulses (LED, on). (c) Schematic time trace of the applied electrical (blue) and optical (green) pulses.

current of 10 μA, the excitation power equals 1 nW. For increasing LED currents and hence light powers, the width of the plateau with almost zero conductance around zero bias and therefore the amount of localized charges decreases. Thus, the QD can be discharged optically. We explain the optically activated discharging by intraband absorption, which depopulates the quantum dot when an electric field is present [42].

Figure 7(a) shows the conductance of the memristor versus number of excited light pulses. Instead of cw illumination as in Fig. 6(b), the memristor is excited with pulses with widths of 10 μs and different light powers. Before the measurement ($N = 0$), the QD is charged and thus the conductance is low. For a light power of 1700 nW, the conductance starts to increase after 140 pulses and saturates at 3.5 μS after 2000 pulses. For decreasing light power, more pulses are required to raise the conductance above zero. The conductance remains unaltered for 2000 pulses with a power of 3 nW and below. Because the amount of transferred electrons is controlled by the width and the power of the light pulses, i.e., the number of incoming photons, larger excitation powers enables discharging with shorter light pulses. In Ref. [43], photoinduced charging of the QD in a similar structure is demonstrated with light in the telecommunication range. Thus, we believe that the presented device allows bidirectional, light-induced conductance changes.

VII. ARITHMETIC COMPUTING

The device with its optical control of the QD-localized charge and state-dependent threshold voltage for discharging is a basic component to perform arithmetic operations with optical pulses. Figure 7(b) displays the conductance

versus pulse number for optical and electrical excitation. We excite the memristor with 10 consecutive light pulses with a light power of 1 nW and a width of 10 ms [see Fig. 7(c) for the time trace of the applied pulses]. Each optical pulse (green) is followed by an electrical pulse (blue) with an amplitude of 4.46 V and a width of 10 ms. After each pulse pair, we determine the conductance of the memristor by applying a readout pulse with amplitude 1.3 V. Before the measurement [$N = 0$ in Fig. 7(b)], the QD is charged by an initializing pulse with an amplitude of −3.8 V and thus the conductance is small. Applying only electrical pulses (switched off LED), the conductance remains almost unaltered up to ten pulses. Because the discharging voltage is larger than the amplitude of 4.46 V, the QD is not completely discharged and the conductance is not affected. For electrical and optical excitation, the conductance is raised successively. Each light pulse partially discharges the QD and thus enhances the conductance and reduces the discharging voltage [see Fig. 1(d)]. After the 9th pulse, the discharging voltage is smaller than the electrical pulse amplitude of 4.46 V and the QD becomes fully discharged. A steep increase of the conductance occurs, as shown in Fig. 7(b). With the well-pronounced conductance enhancement after the 9th pulse, the memristor is suitable for basic arithmetic operations as counting or adding in base 10. From 1 to 9 pulses, the conductance increases from 0.09 to 1.16 μS and for the tenth pulse a sudden raise of the conductance to 2.2 μS is observed. An addition can be performed by applying specific numbers of optical pulses that represent the addends. Multidigit operations are required if the sum of the addition exceeds the base and can be realized by combining several memristors and reset circuits to a network [44]. The reset circuits set the state variable to the initial value (reset to zero) and additionally provide the carry signal for the next significant bit. After the operation, the conductance corresponds to a certain pulse number, which is the result of the addition. In analogy to the implementations in Ref. [45], subtraction, multiplication, and division can be performed. The large conductance enhancement after the tenth pulse is possible only because of the state-dependent threshold voltage for discharging and allows triggering the reset with high accuracy and low impact of undesirable readout noise. For practical applications, this well-defined conductance state for a discharged QD triggers the release of an initialization pulse, which can be employed by additional circuitry (on-chip fabrication of comparator). In analogy to synapses in neural networks, the memristor combines processing of information and memory. The result of the arithmetic operation is stored as conductance of the memristor. Similar results have been reported for phase-change materials with much larger excitation powers [45]. Here, the direct band gap leads to high absorption coefficients and the device structure with a single QD controlling the memristance allows tuning of the conductance state

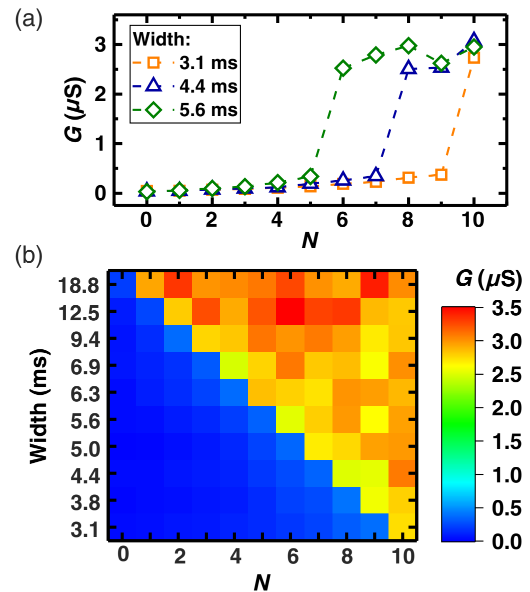

FIG. 8. (a) Conductance versus pulse number for widths of 3.1, 4.4, and 5.6 ms. (b) Color plot of the conductance versus number of electrical and optical pulse pairs. The conductance is shown for different widths of the optical pulses.

by absorbing only a low number of photons. The optical control of the QD charge thus employs an efficient and low-power possibility for arithmetic operations of light pulses.

Figure 8(a) depicts the conductance versus number of applied light pulses with power of 1 nW and different widths of 3.1, 4.4, and 5.6 ms. The initializing pulse is lowered to −4.0 V and the electrical pulses raised to 1.5 (readout) and 5.0 V. For a width of 3.1 ms, the conductance increases above 2.5 μS for the tenth pulse. Raising the width to 4.4 and 5.6 ms, only 8 and 6 pulses are required to discharge the QD, respectively. The color plot in Fig. 8(b) shows that the number of pulses required to discharge the QD can be tuned from one to ten and thus arithmetic operations from binary to decimal bases are possible. The large width of the light pulses (in the order of ms) is chosen to be comparable to the width of the electrical pulses. Arithmetic operations are also demonstrated in Ref. [46] with an optoelectronic resistive switching memory. However, light pulses with widths of seconds are used and a linear dependency between the current of the device and the pulse number is shown. Here, the nonlinear increase of the conductance allows us to clearly distinguish the states after the 9th and 10th pulse for base-10 operations. In addition, the base can be controlled by the width of the light pulses. This is especially beneficial to perform divisions in analogy to Ref. [45], where the number of pulses until a given threshold is exceeded has to be equal to the divisor. Thus, the device is advantageous, because it allows us to tune the number of pulses that are required to exceed the threshold solely by the width of the optical pulses.

VIII. CONCLUSION

In summary, we present an electro-photo-sensitive memristor suitable for neuromorphic and arithmetic computing. Similar to synaptic strength in neural networks, the conductance is controlled by the time difference of incoming voltage pulses. In addition, the threshold voltages to switch the conductance of the device are shown to be state dependent, which emerges from the interplay of a memristance with a memcapacitance. In contrast to other realizations of memristors [47–49], memristance and memcapacitance switching of the presented device are observed between different terminals. The memristance is measured in the two-terminal geometry and the memcapacitance between the lateral gates and the wire. Thus, the state of the device controls the charging and discharging voltages via the gate-channel capacitance (intrinsic feedback). This may enable the implementation of memory-dependent induction of learning or the realization of counters and integrate-and-fire neurons. Here, we exploit the feedback to show the capability of performing arithmetic operations in different bases with clearly distinguishable reset states.

The large pulse widths of several ms and low operation temperature prevent immediate application of the presented device in artificial neural networks. The maximum operation temperature of the device may be enhanced to room temperature by tuning the material composition of the quantum dots and the surrounding matrix [31,50]. The widths of the pulses can be reduced by increasing the amplitude and power of the electrical and optical pulses, respectively. Write times of 6 ns have been already reported for InAs quantum dots in a GaAs matrix [51]. The presented results demonstrate the capability of emulating synaptic functionalities in combination with performing basic arithmetic operations in different bases and may trigger future research regarding the material composition to enhance the maximum operation temperature. With operation at room temperature, the device may be employed in memristor-based non–von Neumann architectures to implement brain-inspired computing with a memory-dependent induction of learning.

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