Design and Cryogenic Operation of a Hybrid Quantum-CMOS Circuit

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Silicon-on-insulator nanowire transistors of very small dimensions exhibit electrostatic or quantum effects like Coulomb blockade or single-dopant transport at low temperature. The same process also yields excellent field-effect transistors (FETs) for larger dimensions, allowing us to design integrated circuits. Using the same process, we cointegrate a FET-based ring oscillator circuit operating at cryogenic temperature which generates a radio-frequency (rf) signal on the gate of a nanoscale device showing Coulomb oscillations. We observe rectification of the rf signal, in good agreement with modeling.

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I. INTRODUCTION

While silicon-based complementary metal-oxide-semiconductor (CMOS) technology constitutes the mainstream of electronics, research for the beyond-CMOS era focuses mostly on devices relying on new materials and/or quantum features [1–3]. Although circuits can be made with these advanced devices, like graphene-based oscillators [4] or single-electron transistors (SETs) [5–7], a first step is to interface these quantum nanoelectronic devices with conventional CMOS circuits. The integration with mainstream technology is greatly simplified when the novel device is silicon based. Hybrid circuits using a small number of field-effect transistors (FETs) and SETs have been demonstrated [8–13]. Recently, Ward *et al.* [14] cointegrated large field-effect transistors used as switches for multiplexing the test of a large number of quantum dots at low temperature. Using only GaAs technology, Hornibrook *et al.* [15] operated a switch matrix at cryogenic temperature for driving quantum bits. Closer to mainstream silicon technology, Suzuki *et al.* [16] integrated a SET device with a one-bit CMOS selector. Here we demonstrate the cointegration of SETs with a more complex logic circuit, on an industrial-scale CMOS facility, on 300-mm wafers. We design, fabricate, and operate at cryogenic temperature a SET relying on well-controlled dimensions [17] and a ring oscillator (RO) CMOS circuit designed for low-temperature operation, made with more than 600 FETs. The different FET or SET behavior is obtained by varying the width of transistors all fabricated with the fully depleted silicon-on-insulator (FD SOI) nanowire technology [18]. The RO output feeds a non-overlapping clock generator which delivers two phase-shifted square wave signals at radio frequency onto the gates of the SET device. When the rf is turned on, we observe a dc current in the SET at zero source-drain bias due to the rectification effect. This effect naturally arises when sufficiently large RF signals are applied to a nonlinear device [19,20].

II. DEVICES AND CIRCUIT FABRICATION

A schematic diagram of the whole circuit patterned on a 300-mm SOI wafer with the trigate SOI technology [18] is shown in Fig. 1.

The wafer has a 145-nm-thick buried oxide and 16-nm-thick Si film on top. This silicon layer is thinned down to 12 nm and patterned to create nanowires by a mesa-isolation technique. Nanowires are defined by optical (deep UV) lithography followed by resist trimming to obtain wire structures as small as 25 nm in width. They are oriented along the ⟨110⟩ direction, with ⟨110⟩ sidewalls surfaces and ⟨100⟩ top surface. The nanowires are capped by approximately 0.8 nm of SiO_2 and 1.9 nm of HfSiON, a 5-nm TiN metal gate (and 50 nm of poly-Si) in order to

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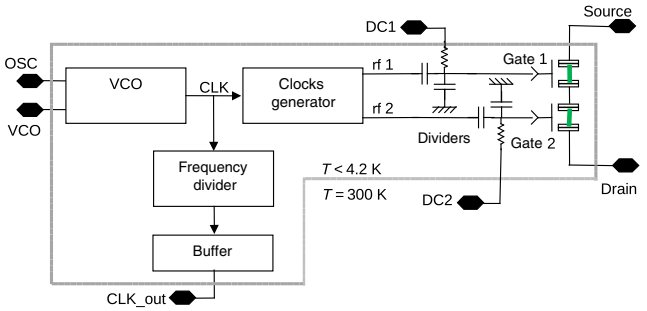

FIG. 1. Schematics of the whole circuit designed and fabricated on 300-mm SOI wafers. The nanowire showing Coulomb blockade below 10 K is on the right. The CMOS circuit driving the gates is made of several subcircuits. A voltage-controlled oscillator (VCO) monitored through a frequency divider feeds a clock generator also based on ring oscillators. This generator delivers two delayed and phase-shifted rf signals, rf 1 and rf 2, which are further attenuated by capacitive dividers and added to external dc biases. The voltage supply V_{DD} referenced to ground GND is not shown.

reduce the gate leakage current and the equivalent oxide thickness, which corresponds to approximately 1.3 nm of SiO_2. After gate etching, a SiN layer of thickness 10 nm is deposited and etched to form a first offset spacer on the sidewalls of the gate. Then, 18-nm-thick Si raised source and drain are selectively grown by epitaxy at 750 C, 20 Torr for the Si transistors prior to a first doping by implantation and activation annealing. A second offset spacer consisting of a tetraethyl orthosilicate liner and a nitride layer is fabricated prior to source and drain implantations, activation spike anneal, and silicidation (NiPtSi silicide), in order to obtain low contact resistances. Finally, tungsten contact and standard Cu back-end-of-the-line processes are used.

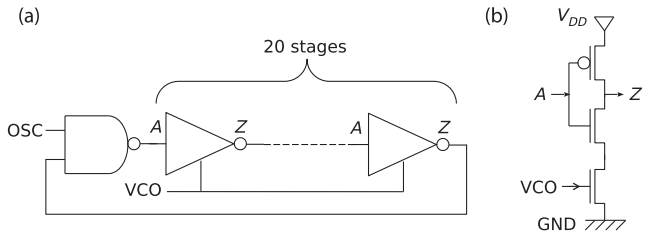

FIG. 2. (a) Schematics of the VCO using a NAND gate at the input as a switch and 20 stages of inverters. (b) Detail of a single inverter stage made of a conventional inverter cell on top (associating *N*- and *P*-type transistors) and a NMOS transistor at the bottom.

All the transistors are supplied with a voltage V_{DD} referenced to ground (GND). The circuit for generating rf signals is made with (2×1)-μm-wide channels and 60-nm-long gates. These dimensions are important to obtain a FET behavior down to low temperature. Cooling should result in the improvement of one of the main figure-of-merit of transistors, namely, an increase of the steepness of the thermally activated subthreshold slope. One should also observe only a moderate increase or decrease of the *on* current. The spacers should be short enough and the nanowire cross section large enough to prevent unwanted effects such as Coulomb blockade [17] or resonant tunneling [21]. There is, therefore, a trade-off between parasitic effects if devices are too small and too much leakage and consumption if devices are too big.

The first block is a VCO, which is detailed in Fig. 2. It can be switched *on* or *off* with the oscillator (OSC) input, and its frequency is tuned by an external control voltage VCO. It is a ring composed of 20 stages of current-starved inverters and a NAND gate to enable the oscillations. The

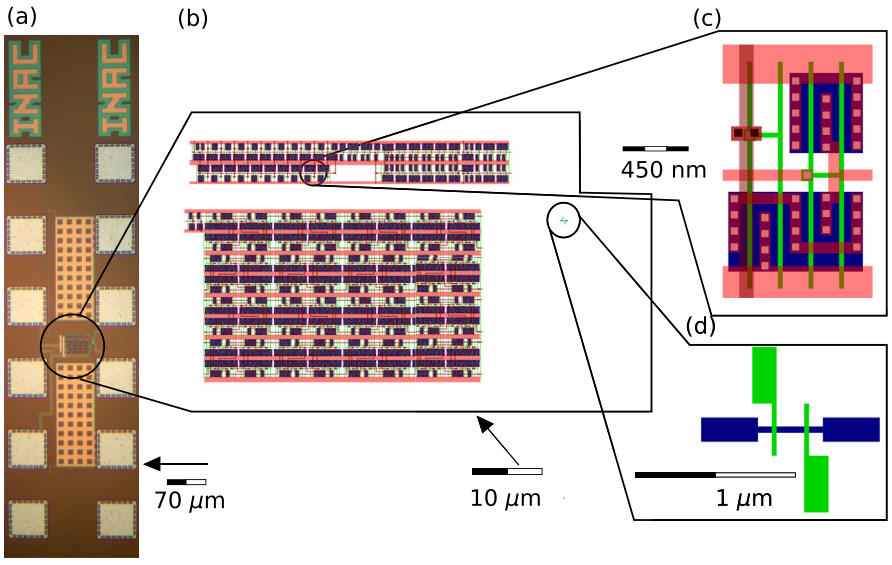

FIG. 3. (a) View of the silicon chip with 12 aluminum contact pads for the whole circuit. The bias resistors implemented at the active area level are not visible in this picture of a finished device after encapsulation. The capacitors are the square arrays made between copper layers of the back-end process. (b) Detailed view of the CMOS transistors and the nanowire with the gate level in green, active area in blue, and metallic vias and lines in red. The top part is the VCO (approximately 130 transistors) and nonoverlapping clock generator (approximately 100 transistors), while the bottom part is the frequency divider (approximately 400 transistors). Both are made with the same wide transistors ($W = 1$ μm) featuring 60-nm-long gates, as depicted in (c). The connections between the group of circuits are not shown for clarity. (d) Detailed view of the single-electron device having a 25-nm-wide channel and a 40-nm-long gate.

current-starved inverter is a simple inverting standard cell complemented by a footer NMOS transistor, as shown in Fig. 2(b). This transistor is used for controlling the amount of current going through the NMOS tree of the inverter. In this way, one gets an oscillator whose voltage-dependent oscillation frequency follows the transfer characteristics $I_{DS}(V_g)$ of the footer transistor, where V_g is its gate voltage and I_{DS} its drain-source current. In agreement with simulations, the VCO output frequency ranges from 300 kHz (VCO = 0.2 V) to 1.8 GHz (VCO = 1 V) at 300 K.

It feeds a second nonoverlapping clock generator with two outputs. This block is made of five buffers allowing us to shift by 108 ps the two signals, ensuring that only one of the two outputs is in the high (V_{DD}) state at any time. In addition, the frequency of the VCO is monitored by a frequency divider. The two outputs rf 1 and rf 2 are attenuated by capacitive dividers in order to lower their amplitudes down to 0.5 mV, and they are added to two dc voltages dc 1 and dc 2 thanks to bias tees realized with 1-MΩ resistors. The design of the passive components is chosen to obtain small temperature coefficients in order to avoid, for instance, freezing of resistors. For that reason, we design the capacitors between the two metallic layers of the back-end process, and the resistors are made with a silicided (NiPtSi) active layer. In the end, dc 1 and rf 1 and dc 2 and rf 2 are, respectively, applied to gates 1 and 2 of the SET. In contrast with the circuit's FETs, this SET is made with a much narrower (25-nm) channel covered by two gates of length 40 nm.

The circuit implementation is shown in Fig. 3, with detailed views of the RO and SET. It uses 12 aluminum pads for external control [see Fig. 3(a)]. The passive components of the circuits are the resistors (not visible) and the 2-pF and 1-fF capacitors [square arrays in Fig. 3(a)] made between the two copper layers of the back-end process.

III. RESULTS AND ANALYSIS

The frequency response of the VCO is shown in Fig. 4 for various temperatures. With the RO being fed by the output current of the N-type field-effect transistors (N-FETs) controlled by the VCO, we obtain a curve similar to the drain-source versus gate-voltage characteristics of a N-FET, with a subthreshold regime getting steeper as the temperature decreases and a saturation at 1.36 GHz at 300 K and 1.06 GHz at 4.2 K. Operation down to 1.1 K is achieved, with a frequency response very similar to the curve at 4.2 K. This very good cryogenic behavior of a CMOS circuit containing approximately 600 transistors shows that conventional silicon electronics is perfectly suitable for use at low temperature, provided that FET behavior is maintained thanks to large-enough dimensions and passive components such as capacitors and mostly resistors are carefully designed. The present design stops suddenly to give any response at approximately 1 K, possibly due to the occurrence of oscillations in some of the transistors because of their relatively short (60-nm) gate length [21]. An advantage of SOI technology is the possibility to use the back gate to tune the device's performance. Here the back-gate voltage is applied over the whole substrate through the buried oxide, in contrast with industrial technology where shallow trench isolation allows the implementation of local back gates. Therefore, in our case, the same potential is applied on *N*- and *P*-type devices; hence, it is not possible to optimize both devices separately. The experimental results obtained when changing the back gate at 1.1 K are shown in Fig. 5. There is an optimum working point for negative back-gate voltage, as

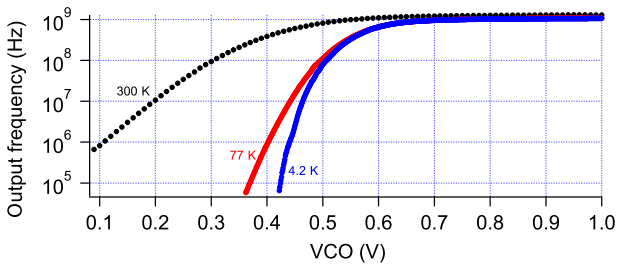

FIG. 4. Output frequency of the voltage-controlled oscillator measured at 300, 77, and 4.2 K after correction by the frequency divider (division by a factor of 65 536). The maximum output frequencies are 1.36 GHz at 300 K, 1.08 GHz at 77 K, and 1.06 GHz at 4.2 K.

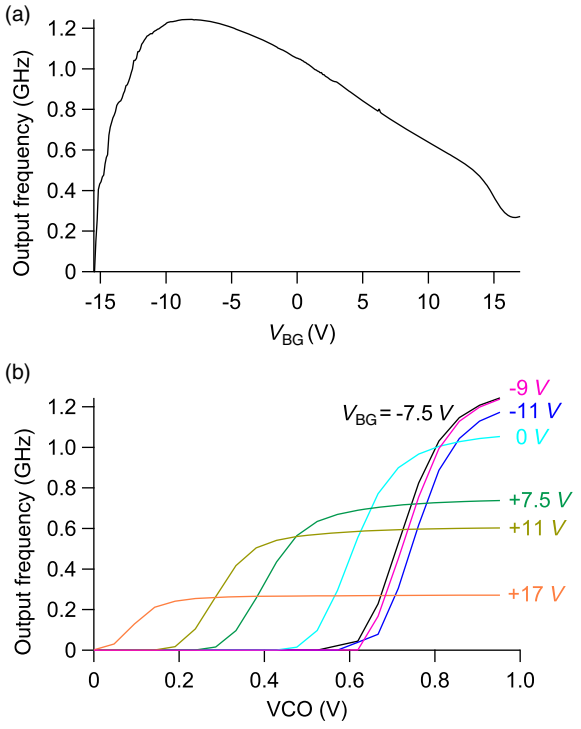

FIG. 5. (a) Frequency response of the VCO at 1.1 K versus back-gate voltage V_{BG}. An optimal working point is found around −8 V. (b) Frequency response versus VCO at different V_{BG}.

shown in Fig. 5(a). We attribute this to *P*-type devices which are known to exhibit a more pronounced shift of their threshold voltage compared to *N* type for the same batch and dimension. There is, therefore, a compromise reached when balancing the thresholds of *P*- and *N*-type devices with a negative back gate. In Fig. 5(b), the effect of the back gate is shown versus VCO. Away from the best working range, we also observe a complete saturation of the frequency which is the result of this disbalance of the thresholds.

Because of its small cross section, the device driven by the CMOS circuit can exhibit Coulomb blockade oscillations below approximately 10 K [17,22]. In the present case, the double-gate SET device shows oscillations only below one gate at low temperature; hence, the other gate is kept at a large dc value (+0.7 V) above threshold, and the device can be considered as a single-gate SET with a voltage V_g applied onto its gate. Its low-frequency transconductance G_{diff} versus V_g is shown in Fig. 6(a). Four quasiperiodic peaks are observed, corresponding to the addition of four electrons in the channel below the gate. The period of 18 mV in V_g corresponds to an effective gate capacitance of 9 aF. These results are obtained without dc drain-source bias and no rf applied; hence, there is no dc current flowing through the device in that case.

When the CMOS circuit is turned on, but still no dc bias applied, we measure a dc current shown in Fig. 6(b).

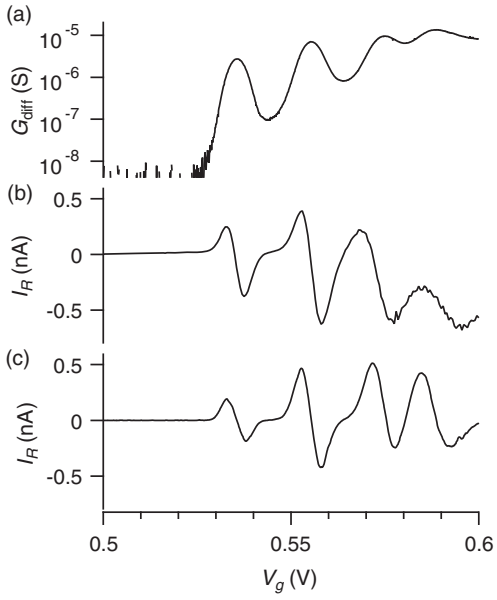

FIG. 6. (a) Coulomb blockade oscillations measured at 1.1 K with a lock-in amplifier with an ac signal of 100 μV at 77 Hz. (b) dc current measured at 1.1 K when $V_{\mathrm{DS}}^{\mathrm{dc}} = 0$ but CMOS circuit switched on, with amplitude 500 μV at 412 MHz. (c) dc current calculated with the rectification model. We find good agreement with the measured current shown in (b). The current follows the derivative of the transconductance, i.e., the second derivative of the conductance.

The presence of current in absence of bias and its characteristic dependence with V_g is well explained by a rectification effect. In nanoscale devices, which are by principle difficult to contact perfectly, ac signals driven onto gates can induce a parasitic oscillatory source-drain bias [19]. For electron pumping experiments, it is important to discriminate between this spurious current and the true pumped current [19,20]. Following these previous studies, we consider a rf-driven gate voltage $V_g(t) = V_g^{\mathrm{dc}} + A\sin(2\pi f t)$, which couples capacitively to the source and drain, hence, creating an additional ac bias component at the same frequency f in addition to the dc bias $V_{\mathrm{DS}}^{\mathrm{dc}}$:

$$V_{\mathrm{DS}}(t) = V_{\mathrm{DS}}^{\mathrm{dc}} + kV_{\mathrm{DS}}^{\mathrm{ac}}\sin(2\pi f t + \phi), \tag{1}$$

where k and ϕ characterize the coupling. The rectified current is the average over one period $1/f$ of the resulting current $I(t) = V_{\mathrm{DS}}(t)G(t)$:

$$I_R = f\int_0^{1/f} V_{\mathrm{DS}}(t)G(t)dt. \tag{2}$$

As already pointed out in Refs. [19,20], the general expression obtained by combining Eqs. (1) and (2) is greatly simplified in the limit of small driving amplitude A. This situation is the same standard case for ac lock-in measurements where one can use a linear approximation: $I(t) \propto (\partial G/\partial V_g)|_{V_g = V_g^{\mathrm{dc}}}$. Here we are interested in the integral over one period [Eq. (2)] to get the dc component; hence, the same approximation is used again and

$$I_R \propto \left.\frac{\partial^2 G}{\partial V_g^2}\right|_{V_g = V_g^{\mathrm{dc}}}. \tag{3}$$

This model is used to calculate the rectified current I_R in the general case and taking into account our nonsinusoidal rf excitation by using the Fourier series describing a square wave instead of a single sine wave. The results are shown in Fig. 6(c). We find excellent agreement with the measurements [Fig. 6(b)] and recover the result that I_R is proportional to the second derivative of the conductance [Eq. (3)]. This is expected since we operate the circuit with rf output amplitude 500 μV, which is small compared to the Coulomb oscillations period in the transconductance. Indeed, this amplitude is of the order of the linewidth of the graph in Fig. 6(a).

IV. CONCLUSION

We design, fabricate, and operate at cryogenic temperatures a circuit allowing us to generate on-chip rf signals on the gates of a nanoscale SET device. The clock generators based on a ring oscillator as well as the capacitance divider and bias resistors are fully operational down to 1.1 K. We observe a finite dc current through the SET device in the

absence of dc bias when the rf drive is turned on. This current, which scales with the derivative of the differential conductance, is well understood within the framework of rectification due to capacitive coupling of the gate signal to the source and drain of the nanodevice. These results pave the way for the integration of conventional CMOS circuits operating at low temperatures together with quantum devices.

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