Mechanism of Fast Current Interruption in *p*-*π*-*n* Diodes for Nanosecond Opening Switches in High-Voltage-Pulse Applications

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Step-recovery diodes operating in the snappy recovery regime are used as opening switches for generating narrow pulses with high-voltage amplitude. Physical modeling of the switching process is complex due to the large number of parameters involved, including diode structure, the extreme physical conditions, and the effect of external driving conditions. In this work, we address the problem by using a physical device simulator for solving the coupled device and electrical driving circuit equations. This method allows deciphering of the physical processes to take place in the diode during the fast current interruption phase. Herein we analyze the complete hard (snappy) reverse recovery process in short-base devices and determine the fast-transition-phase mechanism. It was found that the fast current interruption phase is constructed of two processes; the main parameters governing the switching time duration and the prepulse magnitude are the diode's reverse current density and its base-doping concentration. We describe the dependence of the switching performance in these parameters.

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I. INTRODUCTION

High-voltage pulses with fast transition times are required in various pulsed-power applications. Examples can be found in the fields of plasma research [1], high-power laser driving, particle accelerator beam deflection [2], and ultrawideband radars [3], as well as medical and biological applications such as tumor regression [4]. Generally speaking, such pulses can be generated with various switching devices. Tube-based switches, either vacuum or gas filled, perform well under a wide range of voltage and current operating conditions. These switches usually act as closing switches and are limited to lower pulse-repetition rates compared to solid-state devices. Fast solid-state switches may be either closing switches, based on the avalanche phenomenon (avalanche diode or transistor [5]), or opening switches, as will be shortly discussed. The use of solid-state switches for pulse generation has the merits of producing pulses with high repetition rates and good performance in terms of reliability, service life, stability, repeatability, jitter, and compactness [6–8]. Therefore, an all-solid-state pulse generator is a very appealing building block for applications where high repetition rates, with voltage amplitude reaching tens of kilovolts and rise times in the nanosecond to subnanosecond range, are required.

The ability to exploit step-reverse recovery to produce a fast opening switch for pulse generation was empirically discovered in 1960 by Boff, Moll, and Shen [9]. Pulses, approximately 10 ns wide and 5 V in amplitude, were generated, exceeding any of the existing theories at that time. In the next decade, devices which were named step-recovery diodes (SRDs) or charge-storage diodes evolved, with *p*-*i*-*n* structure and a base width of 0.5–4 μm. For these structures, it is indicated that abrupt junctions are preferable for achieving step recovery [10]. SRDs are widely used in a range of applications with transition times ranging from ten to several hundred picoseconds, with an amplitude of up to several tens of volts.

In the early 1980s, an effort to develop SRD-based opening switches for higher operating voltage was initiated at the Ioffe Physical Technical Institute, St. Petersburg, Russia. Diodes for high operating voltage were manufactured with a *p*-*π*-*ν*-*n* (*p*, *n* and *π*, *ν* stand for heavily and lightly doped layers, respectively.) structure [11]. These diodes (using a specific and unique driving scheme) are named drift step-recovery diodes (DSRDs) [12]. In the following years, similar and improved diodes such as the inverse recovery diode, silicon opening switch, reversely switched dynistor, and others were introduced. DSRD-based generators were improved, producing pulses with voltage amplitude reaching tens of kilovolts and rise times ranging from a few nanoseconds to subnanoseconds [2,13–18]. These improvements are enabled thanks to the modular nature of this technology, in which higher pulse amplitudes can be achieved by facile connection of a number of devices in series.

The production of DSRD diodes is conducted by deep Al diffusion into an *n*-type substrate. Shinohara *et al.* [19] studied the step recovery in a 1000-V, *p*-*π*-*n* device also made by deep diffusion and showed that *p*-type base doping is superior to *n*-type for step recovery. Kozlov *et al.*

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presented scaled-down DSRD structures using epitaxial growth technology together with multiple diffusion steps for the p-type layers [20]. The junction doping profile in all these devices is limited to that of diffusion, preventing the possibility of abrupt junctions.

The reverse recovery process in power rectifiers was first analyzed in a work by Benda and Spenke [21]. Unlike prior studies, this work takes into consideration a high injection level. This is a simplified model assuming constant mobility, neglecting diffusion current (long base compared to Debye length), and negligible recombination. Regarding the external circuitry, the reverse bias is assumed to be driven by a voltage source and series resistor. The effect of base-doping type on the potential distribution and voltage temporal evolution was also investigated [22].

The analysis of the reverse recovery phenomenon in power diodes is usually conducted with the aim of avoiding snappy behavior [23–27]. Different diode structures are being developed in order to enable a wider range of operation while having fast and yet soft recovery [28,29]. Kyuregyan suggested a behavioral model for drift step recovery in p-π-n structures [30]. The model consists of an equivalent circuit of a switched resistor and capacitor. Based on some simplifying assumptions, the equivalent resistance and capacitance nonlinear charge dependences are formulated, and a set of optimized parameters for the device structure and driving parameters is suggested. Yang *et al.* numerically solved the same parameter set for various diode base lengths [31]. They have used a fluid dynamics model for solving the circuit and diode equations.

Although the phenomenon of fast current interruption during snappy reverse recovery in diodes was used for high-voltage opening switches for nearly 50 years, there is no description of the physical mechanism governing this central process [30,31]. The theory of reverse recovery stated by Benda *et al.* is still used today as the basis for explaining the physical basis of DSRD operation [13]. However, this theory does not cover the phase of the fast current interruption which is used for the realization of the opening switch. It also does not include inductance in the current loop. For these reasons, together with the complexity originating from the large number of parameters involved, the design of pulse generators was thus far conducted in a laborious semiempirical process of driving parameters and diode selection [30].

The objective of this research is to determine the physical mechanism governing the fast current interruption occurring during reverse recovery and leading to the snappy recovery phenomenon. This analysis is performed by using a physical technology computer-aided design (TCAD) device simulator, which enables performing the analysis without having to make fundamental simplifying assumptions [32,33].

In diffusion technology, the doping concentration, its profile, and the layer thickness depend on each other. On the other hand, epitaxial technology enables better control over these parameters independently in a wide range of doping concentrations (10^{14} to 10^{19} cm^{-3}) and width up to approximately 100 μm. In recent years, such layers, grown by chemical vapor deposition (CVD), have become widely available commercially. Thick epitaxial silicon layer technology is used in various applications. Examples can be found from the unique tracking detectors used for particle physics experiments [34] to commercial superjunction power transistors [35]. These devices are based on high-quality silicon epitaxial layers, several tens of micrometers thick.

In addition to the analysis of the physical mechanism, the relations between the parameters of the diode's structure and driving conditions to the obtained switching performance are studied in this paper, allowing the design of improved structures. Based on our conclusions, CVD technology may be utilized for manufacturing faster single devices allowing deep subnanosecond switching times, operating at a few hundred volts each.

II. DEVICE STRUCTURE AND MODEL DESCRIPTION

The study of reverse recovery behavior in different silicon p-π-n structures under various driving constrains is performed by using a physical device simulator: Sentaurus-TCAD by Synopsys. The simulator solves the coupled Poisson equation, the current continuity equations, and the electrical-circuit equations. First, the breakdown voltage is extracted from the I-V curves calculated for each structure in steady state using the quasistationary mode. In this case, no electrical circuit is defined, the cathode contact is set as zero potential, and negative voltage is applied to the anode contact. The diode current is calculated while advancing the voltage bias. Near breakdown voltage, the I-V curve becomes parallel to the current axis, and the calculation fails to converge. At this point, the electrode is set to the current mode; i.e., the current through it is enforced and its potential calculated. Next, the device's behavior under various driving current constraints is simulated in mixed mode. For that purpose, the simulator solves the equations of the device, coupled to those of the driving circuit. The simulation uses implicit discretization of the transient equations, for which the backward Euler method is used. The structure mesh grid is set to have tighter spacing at the junction areas in which the doping gradient is high. Doing so has improved the simulation stability and allowed performing more accurate analysis of the space-charge evolution in these areas.

The device model is a one-dimensional, three-layered structure as shown in Fig. 1. As the figure shows, the p and n layers are 10 μm thick and heavily doped with concentrations of 2×10^{19} cm^{-3}, assuring high injection efficiencies. Ohmic contact, with a distributed resistance of 10^{-5} Ω/cm^2, is defined for both diodes' electrodes.

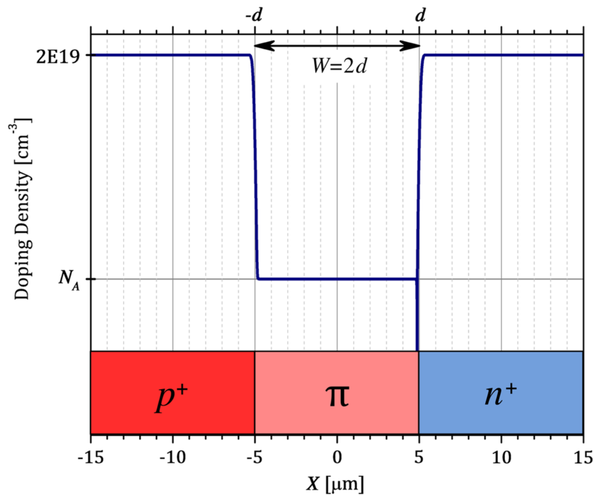

FIG. 1. The simulated diode's doping profile. The p^+ and π layers are B doped, and the n^+ substrate layer is doped with As. The p^+ and n^+ doping is 2×10^{19} cm^{-3}, and the π (N_A) is a DOE parameter, ranging from 10^{14} to 10^{15} cm^{-3}.

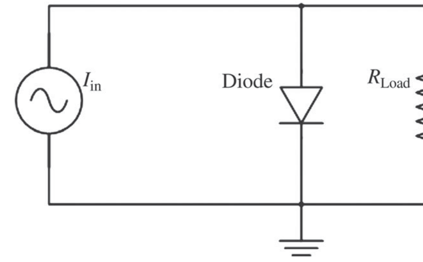

FIG. 2. The simplified driving circuit used for the simulation. The current source is realized by using four parallel ideal sine current sources, yielding the current waveform shown in the inset in Fig. 3 by the black curve.

The design of experiment (DOE) parameters are the base (π) layer doping concentration N_A, its width W, and the reverse current density amplitude J_{rev}. In this work, Fermi-Dirac statistics is taken into account in order to improve the calculation accuracy in the higher carrier densities. Several mechanisms of mobility degradation are taken into account. Those include impurity scattering according to the Masetti model, carrier-carrier scattering by the Conwell-Weisskopf model, and carrier velocity saturation in a high field by the Canali model. Shockley-Read-Hall recombination, including its doping dependence and Auger recombination, are included as well. The Van Overstraeten–de Man model is used for avalanche generation and the model of Slotboom for band-gap narrowing. All models are used with their default values [36].

In practical driving circuits, the energy, initially stored in a capacitor, is transferred during the reverse pulse to an inductor (resonance LC loops). When the diode interrupts the current, the inductor connected in series acts as a current source. The driving circuit used in this work is thus constructed from a current source, the diode under investigation, and a 50-Ω load resistance connected in parallel; see Fig. 2. Replacing the inductor with an ideal current source does not interfere with the analysis of the diode's behavior during its reverse recovery, while it simplifies the simulated circuit and the control over driving parameters. Since resonance LC loops are usually used for driving both the forward and the reverse current pulses, half sine pulses are used in the simulation. The forward pulse width and amplitude are kept constant. Its width and magnitude are chosen such that the injected charge suffices to allow a wide enough reverse pulse width even for the highest J_{rev} value. The reverse pulse width is adjusted such that the diode current amplitude is reduced to half by the reverse recovery process when the input current is maximal. The maximal reverse current level is limited to 4 A, yielding maximal voltage of 200 V over the load resistance. This keeps the maximal voltage over the diode below its breakdown. In order to control J_{rev} as one of the DOE parameters, the device area is changed accordingly.

The diode's ability to block the reverse current recovers in two main phases. Initially, the diode current decreases in a relatively slow rate, and at a certain point in time the rate becomes much faster; see the example in Fig. 3. The generated pulse voltage behaves accordingly; see Fig. 4. The first phase is referred to as the prepulse and the second as the fast transition. These two phases are separated by a knee point, marked by subscript pp. The current interruption waveforms and voltage pulses over the load are processed by using MATLAB software, according to their

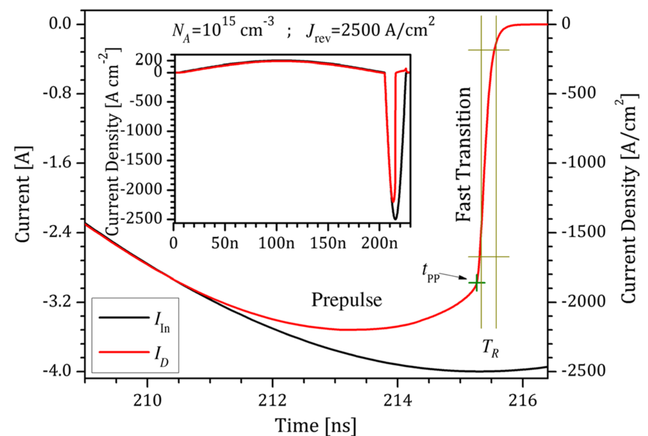

FIG. 3. An example of input (black line) and diode (red line) current waveforms. The diode base doping in this example is 10^{15} cm^{-3}, and its area is 1.6×10^{-3} cm^2. The input reverse current amplitude is 4 A, and hence the maximal reverse current density is 2500 A/cm^2. The figure shows the prepulse phase at $t < 215.24$ ns and the fast-transition phase at 215.24 ns $< t < 215.8$ ns. The green marker at $t = t_{pp}$ shows the knee point separating between the two phases. The rise time T_R duration, defined between 10% to 90% of the fast-transition phase, is marked accordingly. The inset shows the entire driving current waveform including both the forward and reverse pulses.

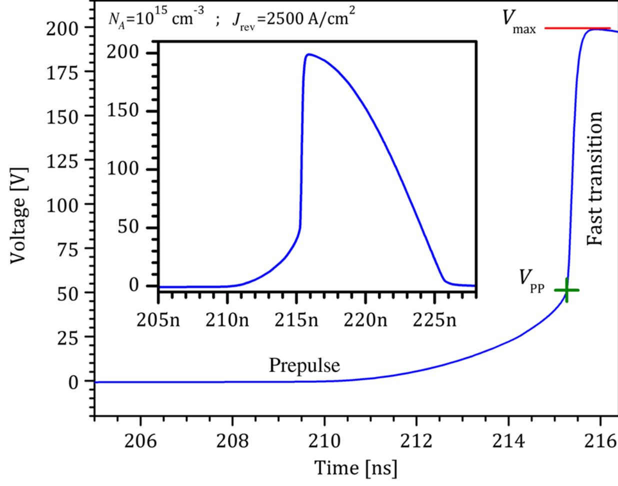

FIG. 4. The output (load) voltage waveform corresponds to the current waveforms shown in Fig. 3. At the prepulse, the load voltage increases slowly, in agreement with the difference between the input and diode currents during that time. The green + marker at $t = 215.24$ ns shows the knee point defining the prepulse voltage V_{pp}. After that time, the fast, snappy, current interruption occurs.

distinct features. The knee point voltage (V_{pp}) is automatically traced by using the L-method algorithm [37]. The fast-transition rise time (T_R) is defined as the time between V_{pp} and the peak voltage ($V_{\max}$), from 10% to 90% of that voltage difference. The generated pulse can thus be characterized by two parameters: (i) the normalized prepulse η_{pp}, defined as $\eta_{pp} = V_{pp}/V_{\max}$, and (ii) the rise time T_R of the fast transition.

III. RESULTS AND DISCUSSION

In order to determine the physical mechanism governing the reverse recovery process, p-π-n diode structures are chosen for analysis, as in the works of Kyuregyan [30] and Yang [31]. Compared to the four-layer DSRD structures, this choice helps reduce the number of structural parameters without affecting the studied phenomena. First, we present preliminary simulations performed for the purpose of setting the parameters for this study. These parameters are then used for the analysis in two hierarchical levels. (i) A DOE including various driving conditions is executed. This way, the dependencies between the different structural and driving parameters to the diode's switching performance are identified. (ii) A deeper insight into the physical mechanisms governing these phenomena is gained by using the simulation's ability to visualize physical processes in space and time domains, without having to include simplifying assumptions. The simulation yields waveforms, in the time domain, from which snapshots at chosen time points are taken. Using snapshots, we can examine the distributions of physical quantities such as carriers, space-charge, and electric field distribution, and the time evolution of these quantities can be analyzed.

A. Diode structural and driving parameters

Prior to analyzing the reverse recovery process in p-π-n diodes, the diode region of operation in terms of the breakdown voltage ($V_{\rm bd}$) is mapped by using the device simulator. The dependence of $V_{\rm bd}$ on the base- (π layer) doping concentration N_A, with W (base width) as a parameter, is shown in Fig. 5. As in the case of p-ν-n [38], in the lower doping concentrations, the graphs are parallel to the horizontal axis, in accordance to the punch-through (PT) mode of operation, and W determines the breakdown voltage. When increasing the doping concentration for a given base width, eventually the device breakdown occurs in a non-punch-through (NPT) mode, and the breakdown voltage is governed by the doping concentration. Based on that figure, one can determine the suitable range of design parameters for a given breakdown voltage. In this work, we focus on devices with a base width of 10 μm operating at PT mode. This choice allows flexibility in testing the influence of the base-doping density without having to adjust other parameters. In order to avoid lowering of the breakdown voltage, the base-doping concentration for such devices must be lower than approximately 1.2×10^{15} cm^{-3}. The DOE includes devices with base doping $N_A = 10^{14}$, 5×10^{14}, and 10^{15} cm^{-3}, which are marked in the figure with red diamonds.

The injected carrier distribution at the end of the forward pulse sets the initial conditions for their extraction by the reverse pulse. A measure of the carrier's distribution is

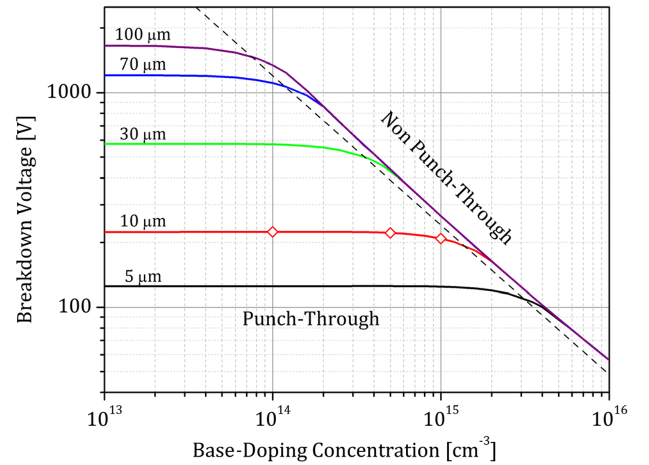

FIG. 5. Simulation results showing the breakdown voltage of p-π-n structure versus its base-doping concentration. The base width, ranging from 5 to 100 μm, is marked near each curve. The red diamonds show the devices that are simulated in mixed mode for dynamic analysis. The black dashed line roughly marks the transition from punch-through (PT) breakdown, on its left, and non-punch-through (NPT) breakdown, on its right.

the concentration ratio K between the injected carrier's concentrations at the base edges [28]:

$$K = \frac{n_e(p^+\pi)}{n_e(\pi n^+)}. \tag{1}$$

Preliminary simulation runs were executed in order to study the effect of the forward pulse width and amplitude on the injected carrier distribution at the end of the forward pulse. Half sine current pulses 50–400 ns long with a current density amplitude ranging from 50 to 200 $\mathrm{A/cm^2}$ were simulated. It was found that for $W = 10\ \mu\mathrm{m}$ the distribution is quite uniform over both pulse width and current density amplitude with $K \approx 1$. For that reason, the forward pulse width and current density amplitude were kept constant throughout the DOE. The forward pulse amplitude was set to 200 $\mathrm{A/cm^2}$ and its width to 200 ns, as can be seen in the inset in Fig. 3.

Our DOE included structures with three different base-doping concentrations as mentioned above. These structures were simulated in the mixed mode under different J_{rev} values, between 100 and 3500 $\mathrm{A/cm^2}$. For each value, a simulation run was conducted, yielding the pulse waveforms. η_{pp} and T_R values were extracted from that data as defined in the model description section.

B. The prepulse phase

As mentioned above, the theory of Benda *et al.* [21,22] is still the fundamental theory used today to analyze the reverse recovery phenomena in DSRD [13,30,31]. Prior to the diode simulation using a modern numerical device simulator, this theory is used here to analyze the structures and driving parameters defined in our DOE. In this theory, simplifying assumptions are used in order to arrive at an analytical solution. This theory describes the reverse recovery process only up to the knee point defined here as $t = t_{pp}$.

In Benda's theory, initially, the carrier distribution in forward bias is solved for the steady-state case. Next, the current is abruptly reversed, and the time of each extraction boundary formation is calculated. After the boundary is formed, this calculation yields negative carrier concentrations. Therefore, from this point on, the analysis is carried out for a simplified case of abrupt boundaries (advancing front of carrier extraction) and constant carrier concentration. As these boundaries advance inward, the space-charge regions on both base rims grow wider. At time $t = t_{pp}$, the inner edges of both rims meet, i.e., $d_l + d_r = W$ (d_l and d_r are the left and right rim width, respectively). The diode voltage at this stage is evaluated by Eq. (2) and is equal to the potential over these rims. In the following equations, V_{SC_l} and V_{SC_r} are the potentials over the left and right space-charge regions, respectively. J_{DR} is the diode reverse current density, q the electron charge, N_A the base doping, μ_p and μ_n the hole and electron mobilities, respectively, and ϵ the dielectric constant. The different exponent values m and n are set by the condition over the normalized length, Eq. (3):

$$V = V_{\mathrm{SC}_l} + V_{\mathrm{SC}_r} = \frac{J_{\mathrm{DR}}}{qN_A}\left(\frac{d_l^n}{\mu_p} + \frac{d_r^m}{\mu_n}\right), \tag{2}$$

$$C_l = \frac{\mu_p q^2 N_A^2}{\epsilon\epsilon_0 J_{\mathrm{rev}}} d_l \quad \text{and} \quad C_r = \frac{\mu_n q^2 N_A^2}{\epsilon\epsilon_0 J_{\mathrm{rev}}} d_r, \tag{3a}$$

$$n = \begin{cases} 1.5 & C_l \ll 1, \\ 1 & C_l \gg 1, \end{cases} \tag{3b}$$

$$m = \begin{cases} 1.5 & C_r \ll 1, \\ 2 & C_r \gg 1. \end{cases} \tag{3c}$$

For each structure and driving condition in our DOE, the potential (V_{pp}) is calculated according to the theory herein described. The results are presented in Fig. 6 by the dashed lines for each of the three base-doping concentrations. As reflected from Eq. (2), the voltage dependence on J_{rev} according to this model is linear.

The dependence of η_{pp} on J_{rev} is next calculated by using the device simulator and is shown in Fig. 6 by the markers and solid lines. In the higher values of J_{rev}, a large portion of the voltage amplitude, up to approximately 35%, is built during the prepulse. An important effect on the prepulse is also observed for changing the base doping. Increasing the base doping leads to a decrease in η_{pp}. However, the maximal base doping is restricted by the diode's breakdown voltage, as reflected in Fig. 5.

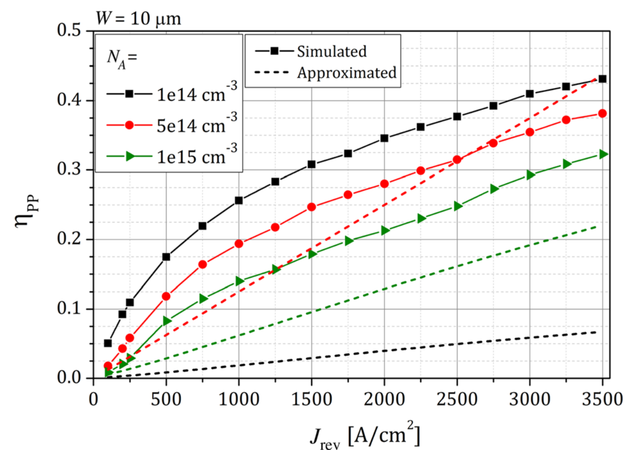

FIG. 6. The normalized prepulse: η_{pp} versus J_{rev}. The simulated η_{pp} results for structures with different base doping (N_A) are shown by the markers and solid lines. An evaluation of η_{pp} according to the Benda and Spenke model is shown for these cases by the dashed lines.

Comparison of the simulation results to Benda and Spenke's approximation shows a large discrepancy, usually underestimating the prepulse voltage. Although this theory is commonly used to describe the operation of step-recovery diodes as opening switches, assumptions made in the model do not necessarily hold for these devices. In our case of a short base length and high reverse current density, the diffusion current is no longer negligible. The high reverse current densities yield high electric fields, which in turn cause carrier mobility degradation while the mobilities are assumed constant in the approximation. In addition, the diode in our case is driven by a current source, representing the loop inductance, while the approximation assumes a high-reverse-voltage source with a large series resistance.

In order to understand the underlying physical process taking place in the diode during the reverse recovery, a detailed study of the carrier transport and their distribution evolution in time was conducted by using the physical device simulator. Because of the large amount of data, two representing cases are presented hereafter, demonstrating the results. The reverse recovery at low (200 $\mathrm{A/cm^2}$) and at high (2500 $\mathrm{A/cm^2}$) J_{rev} values is shown in the following figures. The diode's base doping in the presented figures is set to 10^{15} $\mathrm{cm^{-3}}$.

First, the prepulse is analyzed by taking snapshots of the carrier density distribution in several time points as shown in Figs. 7(c) and 7(f) (at low and high J_{rev}, respectively). [These time points are also marked on the corresponding current and voltage waveforms, Figs. 7(a), 7(b), 7(d), and 7(e) and detailed in Table I.] The first and last snapshots show the carrier distribution at the end of the forward current pulse and at the knee point, respectively.

In the low current density case, as shown in Figs. 7(a) and 7(b), almost no prepulse voltage exists. At approximately $t = t_{p3}$, the boundary of electron extraction is formed and begins advancing to the right [Fig. 7(c)]. Since J_{rev} is low in this case, that boundary is formed nearly 100 ns after the reverse current pulse has begun. Because of the difference between the two carrier mobilities, the boundary of hole extraction is formed later on $t = t_{p8}$ at the π-n junction and starts moving leftwards. Consequently, the boundaries meet less than 1 μm from the π-n junction, on $t = t_{p9}$. After that moment, the fast transition occurs.

As mentioned above, in the case studied here the diffusion current is not negligible. By the time the first boundary forms, the carrier concentration in the still-swamped area has decreased from 10^{17} to 2×10^{16} $\mathrm{cm^{-3}}$. When the hole and electron extraction boundaries meet on $t = t_{p9}$, the carrier concentration at the still-swamped area has dropped to nearly the doping level.

Throughout the process, the hole concentration behind the (left-) moving boundary falls to the value of the doping concentration, according to

TABLE I. Time table of the forward pulse and prepulse snapshots used for displaying the carrier and space-charge evolution.

J_{rev} ($\mathrm{A/cm^2}$)		200		2500	
Time (ns)		t	Δt	t	Δt
Forward pulse	Start	5	200	5	200
	End	205		205	
Reverse pulse	t_{p1}	205		205	
			70		3.265
	t_{p2}	275		208.265	
			25		2.0
	t_{p3}	300		210.265	
			2.9		2.0
	t_{p4}	302.9		212.265	
			3.0		1.0
	t_{p5}	305.9		213.265	
			3.0		1.0
	t_{p6}	308.9		214.265	
			2.0		0.75
	t_{p7}	310.9		215.015	
			0.5		0.25
	t_{p8}	311.4		215.265	
			0.5		...
	t_{p9}	311.9		...	

$$J_{\mathrm{rev}} = qp\mu_p E = qpv, \tag{4}$$

where q is the electron (hole) charge, v the hole velocity, μ_p the hole mobility, and p the hole density. The current density behind the advancing boundary, at the base left rim, is carried by holes solely. Consequently, in the low current density case, no space charge accumulates in that expending region, and there is no potential buildup across the base region [Fig. 7(b)]. Such a situation exists as long as the carrier concentration at the base can support the reverse current density without exceeding the doping concentration. Increasing J_{rev} leads to an increase in the hole velocity according to Eq. (4). When the hole velocity approaches its maximal value v_{sat}, the hole concentration must increase in order to support the forced current density.

Starting from the same initial state at $t = t_{p1}$, but forcing $J_{\mathrm{rev}} = 2500$ $\mathrm{A/cm^2}$ [Figs. 7(d)–7(f)] naturally leads to a faster carrier extraction. The (left) electron extraction boundary is formed only about 4 ns after the forward pulse has ended. Since the entire process is much faster in this case, the diffusion current effect is almost entirely suppressed. The carrier density at the still-swamped area is thus 2×10^{16} $\mathrm{cm^{-3}}$ on $t = t_{p7}$, just 0.25 ns before the boundaries meet. Under these conditions, the base doping cannot support the hole current behind the boundary with accordance to the condition in Eq. (4). The diode's maximal current density in this example is nearly 2200 $\mathrm{A/cm^2}$ around $t = t_{p5}$ [see Fig. 7(d)]. Since

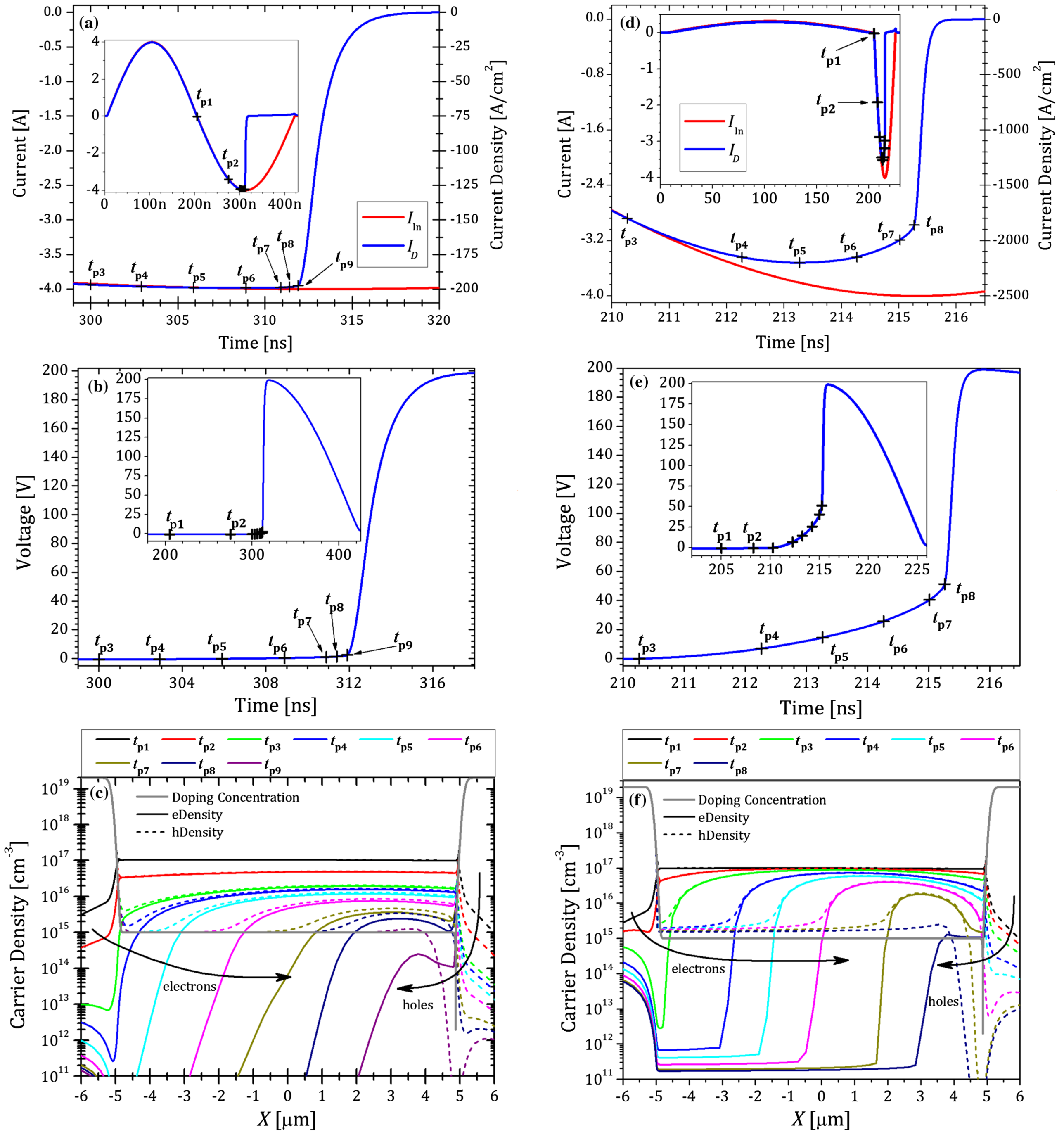

FIG. 7. Demonstrating two cases of reverse current density drive. In (a)–(c) the case of $J_{\text{rev}} = 200\ \text{A/cm}^2$ and in (d)–(f) the case of $J_{\text{rev}} = 2500\ \text{A/cm}^2$ are shown. The input and diode currents waveforms are correspondingly presented in (a) and (d). The figures show the prepulse and fast current interruptions. The right vertical axis indicates the diode current density, while the left and inset vertical axes show the absolute current of both input and diode currents. The insets show the current waveforms including the forward pulse. The corresponding diode and load voltage waveforms are shown in (b) and (e). The carrier distribution evolution for both cases is shown (c), (f) by snapshots of the electron (solid lines) and hole (dashed lines) distributions taken at the time points indicated by markers in the corresponding current-voltage waveforms. The advancement of the boundaries is marked by the black arrows, and the electrons are extracted to the right and the holes to the left.

$v_{h,\text{sat}} = 8.37 \times 10^6$ cm/s, and for $N_A = 10^{15}\ \text{cm}^{-3}$ the maximal current density that can be supported is approximately $1340\ \text{A/cm}^2$, the hole concentration behind the boundary falls to a level higher than that of the base doping, to about $1.6 \times 10^{15}\ \text{cm}^{-3}$. As a result, space charge does accumulate behind the advancing boundary, leading to a potential drop over that region. Accordingly, the space-charge concentration directly depends on the diode current

density and on the base doping. For this reason, increasing the base doping lowers the prepulse voltage. This relationship between the diode's prepulse voltage, the reverse current density, and the base doping is reflected in the results shown in Fig. 6. By using CVD technology, the base-doping profile can be controlled. This may allow lowering the prepulse voltage while allowing high reverse current density.

C. The fast-transition phase

As stated in the introduction, most analyses of reverse recovery aim at achieving soft recovery. When dealing with the snappy recovery, the fast transition is referred to as an abrupt process occurring as a side effect when the diode stored charge has been exhausted. Therefore, the analysis of the prepulse is equivalent to the treatment of the entire reverse recovery in the case where it is soft.

Thus far, we analyzed that stage, i.e., the prepulse. We now arrive at the analysis of the fast current interruption phase. The DOE results are used for the analysis of the general trends and the relations between different parameters and performance. The same two representative cases as before ($N_A = 10^{15}$ cm^{-3}, $J_{\text{rev}} = 200$, and 2500 A/cm^2) are used for demonstrating the physical processes in the diode during that phase. Table II specifies the points in time where snapshots are taken in each case for the analysis. These points are displayed in the following figures. The dependence of the rise time duration T_R on J_{rev} (Fig. 8) is evaluated from the simulated diode current waveforms. At lower J_{rev} values, T_R rapidly decreases with J_{rev}, and at higher current densities, that decrease is saturated. In the case of $J_{\text{rev}} = 3500$ A/cm^2, a T_R value as low as 190 ps is obtained. Considering $N_A = 10^{15}$ cm^{-3}, where $\eta_{pp} = 0.35$, this T_R value translates to a rise rate of 0.72 V/ps. This result, of a basic p-π-n model structure, is comparable to experimental results obtained in four-layered diffusion-based DSRDs, where rise rates of 0.65 V/ps [20] and 0.8 V/ps [13] were demonstrated. As can be seen from Fig. 8, the base-doping level has no effect on T_R itself. Yet, the rise rate is affected from the doping level, through its effect on η_{pp}. Since, for a given J_{rev}, higher N_A leads to lowering of η_{pp}, a higher doping level will lead to higher rise rates.

TABLE II. Time points in which snapshots are displayed for visualizing the processes leading to the fast-transition phenomenon, as displayed in the following figures.

J_{rev} (A/cm^2)		200		2500	
Time (ns)		t	Δt	t	Δt
Reverse fast transition	t_{f1}	311.9		215.265	
			0.2		0.025
	t_{f2}	312.1		215.29	
			0.3		0.05
	t_{f3}	312.4		215.34	
			0.25		0.05
	t_{f4}	312.65		215.39	
			0.25		0.05
	t_{f5}	312.9		215.44	
			0.25		0.05
	t_{f6}	313.15		215.49	
			1.0		0.05
	t_{f7}	314.15		215.54	
			3.25		0.075
	t_{f8}	317.4		215.615	

The input and diode current waveforms versus time for the two cases are shown in Figs. 9(a) and 9(c). As can be observed in the figures, it is found that the fast-transition phase is actually divided into two stages. This behavior is observed in all cases simulated and is demonstrated here in both low and high J_{rev}. The first stage, occurring between time points t_{f2} and t_{f4} in both cases, is characterized by a sharp linear decrease in the diode's current. The second stage, starting at t_{f4}, is characterized by slower exponential decay of the current towards zero.

By studying the carrier density evolution [Figs. 10(a) and 10(c)] during the fast-transition phase and comparing it to the current waveforms [Figs. 9(a) and 9(c)], it is clearly seen that the first stage corresponds to the depletion of holes from the base layer. Similar to the carrier extraction mechanism during the prepulse phase, the hole (and electron) depletion is performed by a moving boundary. Owing to the difference between electron and hole mobilities, the prepulse extraction boundaries meet near the π-n junction. This point is the starting point for the hole depleting boundary, moving leftward. The electron depletion is much faster, and the base is depleted from electrons by $t = t_{f3}$. The fast transition is therefore governed by the hole extraction. The current linear time dependence during the first stage indicates a constant

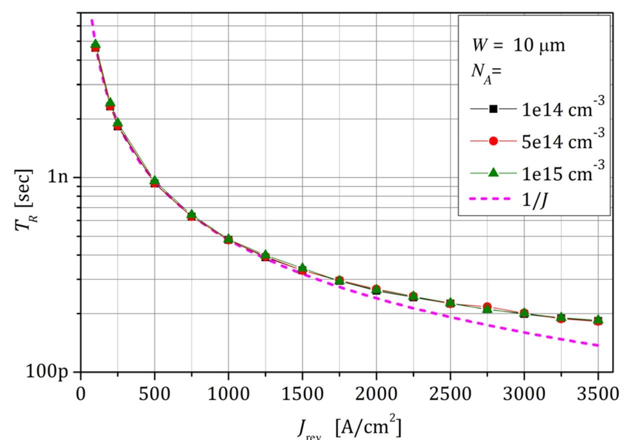

FIG. 8. The duration of the fast-transition phase of current interruption, T_R, and its dependence on the reverse current density amplitude.

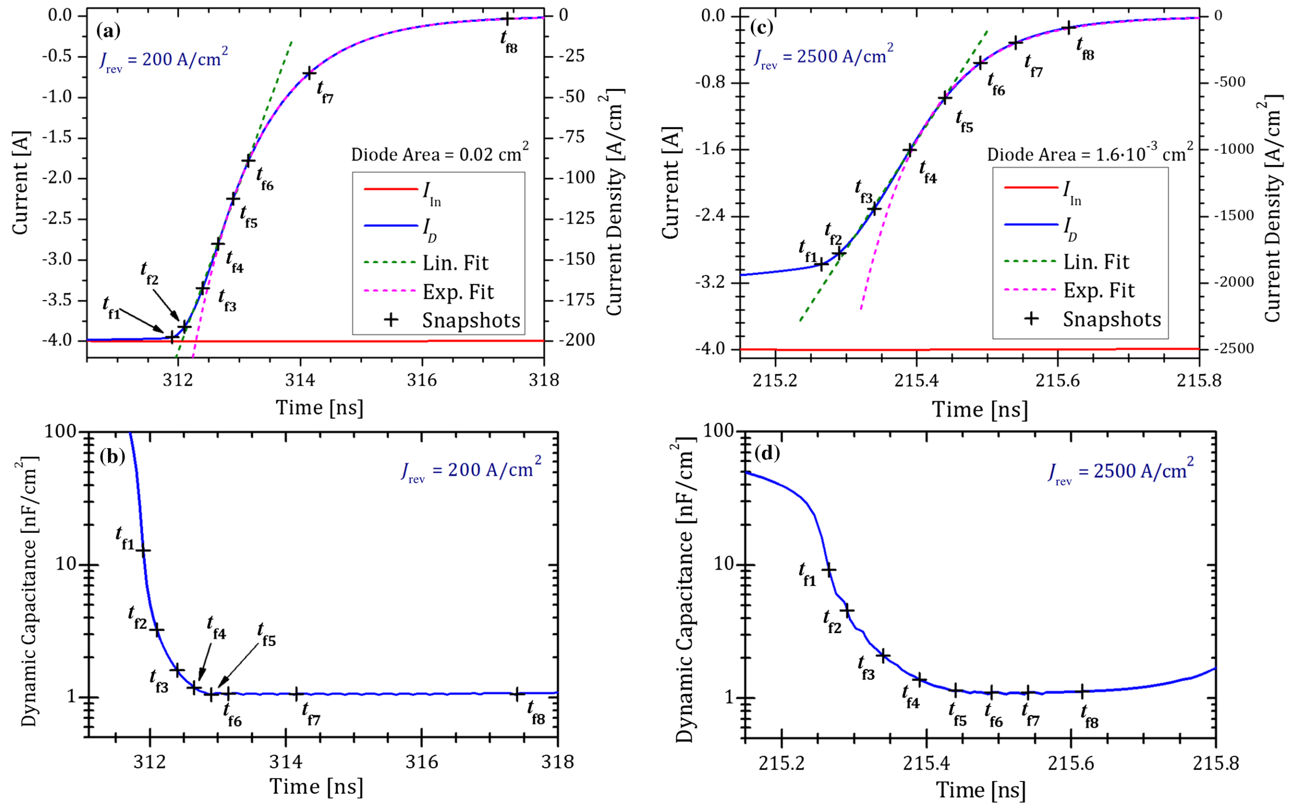

FIG. 9. Current versus time waveforms for low- and high-current density amplitudes, $J_{\mathrm{rev}} = 200\ \mathrm{A/cm^2}$ in (a) and $J_{\mathrm{rev}} = 2500\ \mathrm{A/cm^2}$ in (c). In both graphs, the input current (red curve) and diode current (blue curve) are shown. The diode current density is displayed on the right vertical axis. The first stage of the fast current interruption phase is linearly fitted (dashed green curve), and the second stage is fitted to the expected function of the equivalent RC circuit (dashed magenta curve). The lower graphs, (b) and (d), show the corresponding diode's differential capacitance time dependence. The black markers in all graphs correspond to the snapshots shown in Figs. 10 and 11.

extraction rate and accordingly a constant boundary velocity. Therefore, the duration of this stage depends directly on the base-layer width and the boundary velocity.

In order to estimate T_R dependence in the reverse current density during the first stage, we can observe the current density as the rate of charge (Q) extraction from the base. Assuming the boundary shape is constant in time, we obtain

$$J = \frac{dQ}{dt}\frac{1}{A} = \frac{qp}{A}\frac{dx}{dt}, \tag{5}$$

where A is the diode area, q the electron (hole) charge, and p the hole density. Therefore, $T_R(\propto dt)$ has a $1/J$ dependence. Such dependency is presented in Fig. 8 by the dashed line. In the lower current densities, up to about $1500\ \mathrm{A\,cm^{-2}}$, this relation describes the diode's behavior accurately. At higher current densities, this simple relation predicts faster current interruption by the diode, comparing to the simulation. This discrepancy is attributed to the mobility degradation at high current densities, due to the carrier's velocity saturation in high electric fields.

In the previous section, describing the prepulse phase, it is shown that the remaining carrier concentration at the end of the prepulse phase is set by the diode current density. While the space charge at that stage depends on the sum of the free carriers and the doping concentration, and thus the base doping affects η_{pp}, in the fast-transition phase these free carriers are extracted, and therefore this process does not depend on the base-doping concentration, as reflected from Fig. 8.

The current interruption rates during the first stage of the fast transition are evaluated by linearly fitting the current waveforms (Fig. 9). In the low J_{rev} case, the diode current density is reduced from 200 to about $140\ \mathrm{A/cm^2}$ with an interruption rate of $dJ/dt = 2.1\times10^9\ \mathrm{A/cm^2\,s}$. Similarly, in high J_{rev}, it decreases from about 1860 to $1000\ \mathrm{A/cm^{-2}}$ with a rate of $dJ/dt = 1.3\times10^{10}\ \mathrm{A/cm^{-2}\,s}$; see Figs. 9(a) and 9(c). In this phase, comparing to the prepulse phase, the initial (hole) concentration is considerably lower, and thus the boundaries' velocities are much faster.

The advancing boundaries, depleting the base region during the first stage, differ in their appearance in the low and high J_{rev}. In the low J_{rev} case, once the hole-depleting

boundary starts advancing, its width converges to a constant value [Fig. 10(a)]. In the high J_{rev} case, on the other hand, the boundary width keeps growing until (at $t = t_{f4}$) the base left edge is depleted [Fig. 10(c)]. This difference originates from the different initial conditions for the base depletion in both cases. In the low current case, the base charge is initially neutral. With the boundary movement, the electric field at the depleted area trailing the boundary increases. The electric field's distribution throughout the process is monotonically increasing with position and similar to its final (steady-state) distribution [Fig. 10(b)]. In the high current density case, the base is initially charged with a positive charge across the base yielding an electric field with an opposite (decreasing) gradient; see Fig. 10(d), the black line at $t = t_{f1}$. During the hole depletion, those on the left side experience a stronger field and thus drift faster. The boundary is consequently widened leftward. The electric field behind the boundary, at the depleted area, naturally grows higher, and its final distribution converges to its steady-state profile. During that process, the dominating current component at the depleted areas is the displacement current. Although there is a difference between the processes depleting the base during the first stage, manifested by the difference in the boundaries' shapes, the current interruption time dependence is consistently linear.

During the reverse recovery process, the diode's capacitance decreases from its high (steady-state forward) value to its minimal (steady-state reverse) value. The diode's behavior may be examined through its dynamic capacitance, defined as

$$C = \frac{dQ_D}{dV} = J_D \frac{dt}{dV}, \tag{6}$$

where Q_D is the diode's charge density and J_D the current density through it, and $dQ_D = J_D dt$. The dynamic capacitance is calculated from the diode's current and voltage waveforms for each case and is shown in Figs. 9(b) and 9(d). Comparing to the diode's steady-state C-V dependence, its dynamic capacitance, analyzed here, sustains higher capacitance values than would be expected. Therefore, the steady-state C-V curve cannot be used for estimating the diode's capacitance versus its voltage during that process. Actually, this curve is the lower boundary for the diode's dynamic capacitance. The diode's capacitance

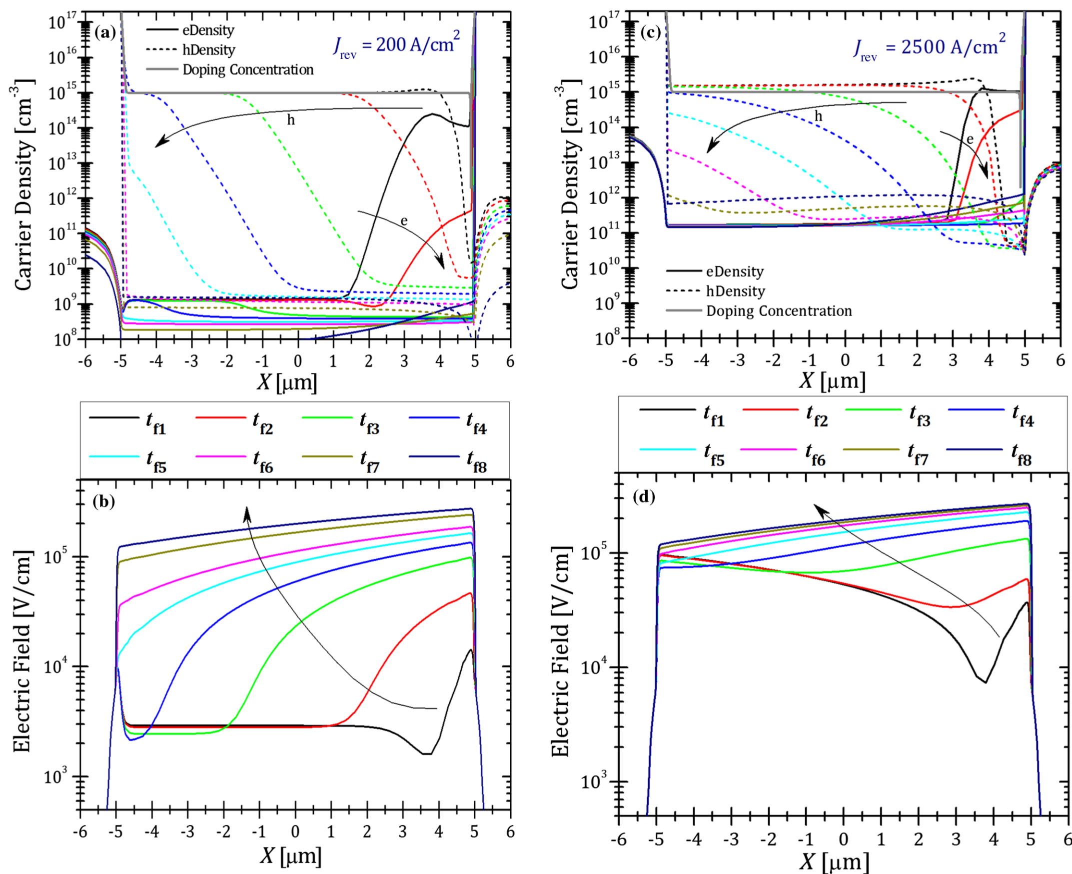

FIG. 10. (a) and (c) show snapshots of the carrier density distribution and its time evolution. In (b) and (d), snapshots of the electric field (displayed in absolute value) evolution are shown. The graphs on the left show the case of $J_{\mathrm{rev}} = 200\ \mathrm{A/cm^2}$ and on the right the case of $J_{\mathrm{rev}} = 2500\ \mathrm{A/cm^2}$. The arrows in the figures show the direction of time advancing. The snapshot time points correspond to Table II.

in a certain voltage is set by the dynamic process parameters. It is found that only when the diode voltage arrives at V_{pp}, does its capacitance rapidly decrease. As was shown, V_{pp} depends on $J_{\rm rev}$; therefore, the rapid decrease in the diode's capacitance occurs at higher voltage as $J_{\rm rev}$ is increased.

After the entire base region has been depleted, the second stage begins. Around time mark t_{f4}, the diode's capacitance reaches its minimal value and maintains that value until its current has been exhausted. The minimal capacitance value for p-i-n diodes can be modeled as a parallel plate capacitor with the width of the diode base. For the studied structures, $W = 10$ μm, and using a silicon dielectric constant and normalized to an area of 1 cm^2:

$$C_{\rm min} = \frac{\epsilon_0 \epsilon_r A}{W} = 1.05 \text{ nF}. \tag{7}$$

The calculated $C_{\rm min}$ is consistent with the simulated data shown in Figs. 9(b) and 9(d) after $t = t_{f4}$. Therefore, in this stage, the current waveform is approximated according to the expected behavior of the RC circuit shown in Fig. 2 by replacing the diode with a constant capacitor with $C = C_{\rm min}$. The expected diode current step response $u(t)$ is thus of the form

$$i_D(t) = u(t) \exp\left(-\frac{t - t_0}{\tau}\right), \tag{8a}$$

$$u(t) = \begin{cases} -4 & \text{if } t > t_0, \\ 0 & \text{otherwise,} \end{cases} \tag{8b}$$

where $\tau = RC$ is the time constant. The step amplitude is set to 4 A with accordance to the simulation conditions. Fitting the simulation results (starting t_{f4}) to this expression yields the time constants $\tau = 1.1$ ns and $\tau = 91.7$ ps, for the low and high current densities, respectively. As seen in Figs. 9(a) and 9(c) (exponential fit), the fitted data match the simulated results with $R^2 = 0.999$. The time constant calculated directly from the diode's structural parameters is $\tau = 1.1$ ns and $\tau = 88$ ps for these two cases, respectively. (This calculation took into account the diode area used for controlling $J_{\rm rev}$ while keeping a constant current and load resistance of 4 A and 50 Ω, respectively). Thus, we can conclude that the governing mechanism in the second stage of the fast transition is that of capacitor charging by displacement current.

The space-charge density time evolution at the base region and at its edges is presented in Figs. 11 and 12, respectively. In the case of low $J_{\rm rev}$, at $t = t_{f1}$ space charge exists only at the base edges [Fig. 11(a), black line]. Thus, at this time point the diode behaves like two capacitors connected in series. Because of the short distance between their opposing charges, the capacitance is high in both junctions. At the first stage (between t_{f1} to t_{f4}), the depletion region expands to the left by the hole extraction boundary, moving leftwards. This process is equivalent to separating the right capacitor plates by moving its left plate leftwards. The right edge (the π-n) capacitance is lowered, and consequently it dictates the total diode capacitance. For that reason, the diode capacitance during the first stage is rapidly decreasing; see Figs. 9(b) and 11(a). At the same time, negative charge accumulates at the base, and in accordance the opposing positive charge at the edge of the n layer (at $x \approx 5$ μm) is increasing; see Fig. 12(b). Eventually, between time points t_{f4} and t_{f5}, the entire base is depleted, and the positive charge (peak) of the left capacitor is removed. This results in merging the two base edge capacitances into one. At this point in time, the second stage begins.

In the case of high current density, the base is initially (at t_{f1}) charged positively, and that charge balances the negative charge at the p layer edge (around $x = -5$ μm); see Fig. 11(b). Therefore, the positive charge peak that

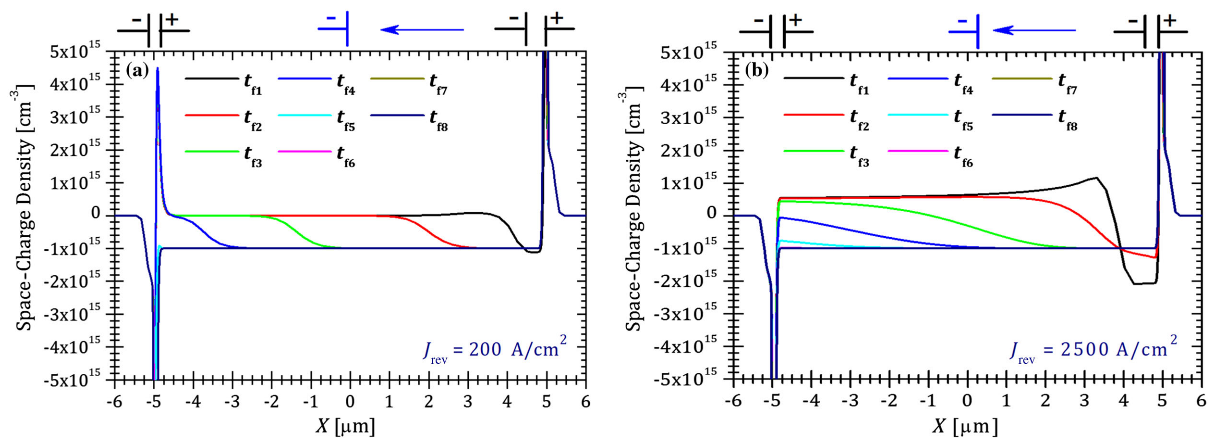

FIG. 11. Space-charge density evolution in the diode base for the two cases (a) $J_{\rm rev} = 200$ A/cm^2 and (b) $J_{\rm rev} = 2500$ A/cm^2. The snapshots correspond to the time points shown in the previous graphs. The initial junction capacitance is schematically illustrated above the graph in black, and the right capacitor "moving plate" in analogy to the moving hole extraction boundary in blue.

existed on the right side of that junction in the low current density case does not exist in this case. The depletion of excess holes from the base changes the space-charge polarity from positive to negative. This is balanced by accordingly changing the charge density in both base edge peaks [Figs. 12(c) and 12(d)]. At the right edge the positive charge is increasing, and on the left edge the negative charge is decreasing. After $t = t_{f5}$, the entire base is depleted, and the diode capacitance is the normal parallel plate capacitance as described earlier.

D. Outlook

For the structures analyzed in this work, we show that the base width and carrier's saturation velocity determine the minimal theoretical rise time for the fast-transition phase; i.e., the advancing boundary transit time through the base dictates the duration of the fast transition's first stage, and, thus, decreasing the base width will reduce its duration. Future design may enable moving the prepulse extraction boundary meeting point to the left (inward). This will enable the fast-transition boundaries to be depleted outwards simultaneously. In this way, the duration of the base depleting (i.e., the fast-transition first stage) will be shorter. This may be done, for example, by engineering the injected carrier's distribution at the forward pulse through the control of the hole and electron injection efficiencies.

The second stage of the fast transition further increases the rise time due to the diode's capacitance charging. Although technically challenging, systems have been reported where many diodes are connected in series to obtain a switching device. This helps reduce the capacitive time constant. For the case of connecting a series of n diodes, the device operating voltage is n times that of a single diode and its capacitance is divided by n. In addition, the load resistance seen by a single diode is the load resistance divided by n. Unlike the case of four-layered DSRD (p-π-ν-n), for the p-π-n case, we show in this work that it is beneficial to drive the diode in high reverse current density. This creates a strong electric field leading

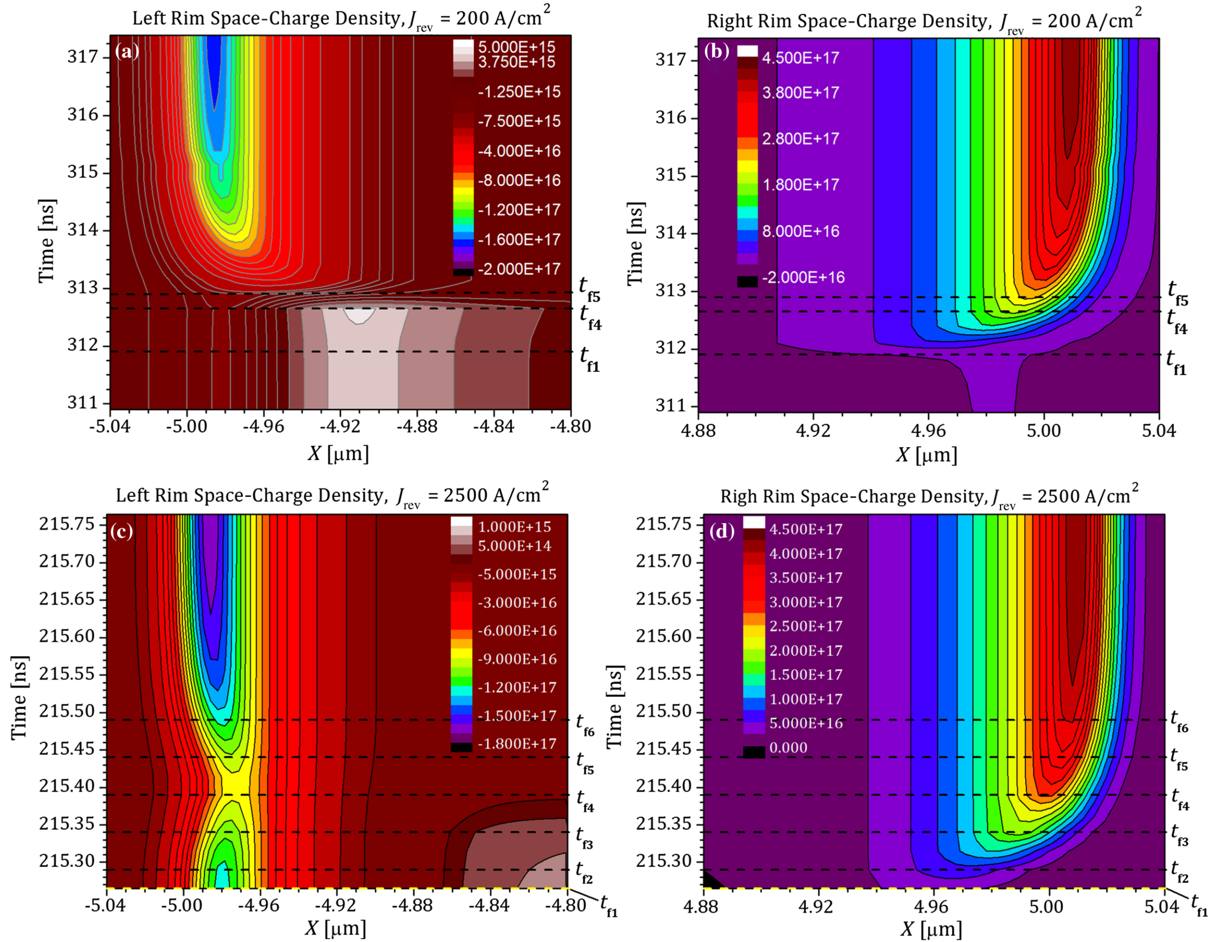

FIG. 12. Space-charge density time evolution at the junction areas. (a) and (b) show the left and right junction, respectively, for $J_{\rm rev} = 200\ {\rm A/cm^2}$, (c) and (d) for $J_{\rm rev} = 2500\ {\rm A/cm^2}$. In all graphs, the horizontal axis is the position x, the vertical axis is time (in nanoseconds), and the color map (z axis) shows the space-charge density. Dashed lines mark time points corresponding to the same current density cases in Figs. 9–11.

to higher carrier velocities, approaching saturation velocity. In addition, this allows decreasing the device area for a given current and thus further reducing its capacitance.

Fabrication of DSRD devices using Al diffusion technology has limiting factors. Manufacturing future diodes using thick layer epitaxy may improve their performance by expanding these limits. Such a device may be fabricated by growing a lightly doped p-type (π) layer over a highly doped substrate [39]. The layer thickness can be ten to about 100 μm thick. The upper, contact, layer can be realized by growing a second, highly doped, epitaxial layer with the doping type opposite to that of the substrate. Additional ion implantation may be used in order to improve the contact resistance. Finally, contact metals are deposited. In contrast to the laborious semiempirical methodology, the combination of TCAD simulation with CVD technology will enable a systematic design methodology of device structure and its driving parameters with improved flexibly in device realization.

IV. CONCLUSIONS

In this work, the physical mechanism of fast current interruption in p-π-n high-voltage step-recovery diodes is established and presented. By using a device simulator, the prepulse and snappy or fast-transition phases are analyzed. It is shown that the existing model inadequately describes the prepulse phase in the discussed case of a short device. The discrepancy is attributed to the neglecting of various physical effects, namely, the diffusion current and the mobility degradation in high electrical fields.

The fast-transition phase (the fast-switching phase) is analyzed here. The rise time is found to be inversely proportional to the reverse current density at its low values. At higher current densities, further decrease of the rise time is limited by carrier mobility degradation. A significant observation is that the fast transition is divided into two stages. In the first stage, the base is depleted from the remaining carriers. In the second stage, the inner edges of the p and n layers are charged by displacement current, as in the case of a parallel plate capacitor. The latter process is shown to be slower, depending on the RC time constant.

The methodology demonstrated here allows the design of improved switching devices, exploiting the advantages of contemporary CVD technology.

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