Mo-Si superconducting nanowire single-photon detectors on GaAs

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We report on Mo-Si-based superconducting nanowire single-photon detectors on a gallium arsenide substrate. Mo-Si deposited on a passivated GaAs surface has the same critical temperature as Mo-Si deposited on silicon. The critical temperature decreases slightly on depositing Mo-Si directly on the native oxide of GaAs. Hence, Mo-Si works well as a thin-film superconductor on GaAs. We propose that the amorphous structure of Mo-Si ensures compatibility with the GaAs matrix. Superconducting nanowire single-photon detectors (SNSPDs) are fabricated with Mo-Si on GaAs using a meander-wire design. The SNSPD metrics are very similar to those of devices fabricated with the same procedure on a silicon substrate. We observe a plateau in the response-versus-bias curve, signaling a saturated internal quantum efficiency. The plateau remains even at an elevated temperature, 2.2 K, at a wavelength of 980 nm. We achieve a timing jitter of 50 ps and a recovery time of 29 ns. These results point to the promise of integrating Mo-Si SNSPDs with GaAs photonic circuits.

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I. INTRODUCTION

Quantum photonics, the manipulation and detection of photonic qubits, is increasingly pursued on chip. Typically, the waveguides consist of silicon or silicon nitride. GaAs is also a possibility [1]. Individual InAs quantum dots create single photons in the GaAs waveguides with near-unity efficiency [2,3], and the photons can be highly indistinguishable [4]. Furthermore, GaAs is electro-optically active, allowing for the creation of voltage-tunable switches and phase shifters [5]. Quantum photonic integrated circuits on this platform can be fabricated in a single lithographic step without the need for a hard etching mask [6].

Quantum photonics requires not only single-photon sources and a waveguide circuit but also single-photon detectors with high efficiency, a low dark count-rate, a high repetition rate, and low timing jitter. Such metrics can be achieved presently only with superconducting nanowire single-photon detectors (SNSPDs) [7]. These detectors are based on a superconductor switching from the superconducting to the resistive state by absorption of a photon [8–10].

It is advantageous to integrate the detectors with the on-chip waveguides. On the one hand, evanescent coupling of an in-waveguide photon to an on-waveguide detector can be highly efficient [11]. On the other hand, by removing the need for out-coupling to an external detector, photon loss can be much reduced. The challenge lies in the heterogeneous nature of the materials used for the waveguides and for the SNSPDs.

The most commonly used superconductors for SNSPDs are niobium nitride (NbN) and niobium titanium nitride (Nb-Ti-N) [9,10,12]. This material provides outstanding metrics, such as system detection efficiencies above 90% [13], timing jitters below 5 ps [14], repetition rates of 25 MHz, [15] and dark count-rates below 10 Hz [13,16]. Furthermore, the critical temperature is about 10 K even in thin-film form, such that NbN-based SNSPDs operate with low noise in ^{4}He cryostats at about 2 K. The integration of NbN SNSPDs with an optical waveguide results in a coupling efficiency close to unity [11]. In the past, waveguide-integrated NbN SNSPDs have been realized for several photonic platforms [16], including GaAs [17,18]. However, NbN is deposited as a polycrystalline film. Experience shows that it is challenging to deposit the polycrystalline material Nb-Ti-N directly on crystalline substrates such as GaAs. This is a consequence of a lattice mismatch [16,19,20]. For most single-crystal substrates, technologically challenging high-temperature deposition is necessary to reduce structural defects [20,21]. High-yield integration of NbN SNSPDs with GaAs is therefore not straightforward and has not yet been achieved.

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Amorphous superconductors such as tungsten silicide (WSi) or molybdenum silicide (Mo-Si) represent an alternative material system for SNSPDs [22,23]. These materials provide a yield close to unity on silicon substrates, even for deposition at room temperature [10,16]. The detector efficiency can be very high, above 90%. The critical temperature is about 5 K in thin-film form and because of this, operation at a temperature of 1 K or less typically provides better performance [23]. The amorphous nature of the materials renders them much less substrate specific than the crystalline NbN. Recently, Mo-Si SNSPDs have been integrated with nanophotonic silicon nitride (Si_3N_4) waveguides on a silicon chip and an on-chip efficiency of 73% has been achieved [24].

An open question is the extent to which Mo-Si is compatible with a GaAs substrate. We answer this question here by establishing a fabrication process of Mo-Si-based SNSPDs on GaAs. We present a detailed analysis of the properties of the material itself and an optimization of its deposition conditions. Mo-Si films on a GaAs substrate superconduct with a critical temperature only slightly lower than those of equivalent films on a Si substrate. We successfully operate Mo-Si meander lines on GaAs as single-photon detectors. The efficiency, timing jitter and recovery time of these Mo-Si SNSPDs on GaAs are very similar to commercial Mo-Si SNSPDs fabricated on silicon substrates.

II. OPTIMIZATION OF SUPERCONDUCTING Mo-Si THIN FILMS

One of the critical steps in SNSPD fabrication is the thin-film deposition of the superconducting material. Mo-Si is deposited via cosputtering using a dc and rf bias for the molybdenum and silicon targets, respectively, under ultrahigh-vacuum conditions (pressure below 10^{-9} mbar). The target is at room temperature. Before opening the sample shutter, presputtering for 60 s cleans the targets and stabilizes the sputtering conditions. Once the thickness of the Mo-Si film reaches the desired thickness, we close the Mo shutter separately and continue the deposition of silicon to create a Si capping layer. Controlling the sputtering rates of Mo and Si separately allows thin films with different compositions to be deposited deterministically.

To assess the properties of the thin films, the superconducting material is cooled down to cryogenic temperatures and its resistivity is measured. A variable-temperature insert (VTI) allows control of the temperature down to 1.4 K. To measure the sheet resistance of the thin layers, we use a four-point method that is independent of the contact resistance [25].

Given a specific substrate material and sputtering process, the superconducting properties of the thin films depend on thickness and composition. The impact of the former on the superconducting transition is illustrated in Fig. 1 for two different substrate materials, commercial intrinsic (001) silicon with a 285-nm-thick oxide layer and GaAs, specifically a 50-nm-thick GaAs epilayer grown by molecular-beam epitaxy on top of an AlAs/GaAs superlattice, itself on a commercial (001) GaAs substrate. In Fig. 1(a) we depict sheet-resistance versus temperature curves for film thicknesses of 4.0 nm (red), 5.0 nm (blue), and 6.0 nm (green), deposited on Si (solid) and GaAs substrates (dashed). For Si, we obtain critical temperatures of 4.4, 4.9, and 5.1 K; and for GaAs, 3.6, 4.2, and 4.7 K, respectively. The critical temperatures on GaAs are slightly lower compared to those on Si. This is a consequence of the complex native oxide that forms almost immediately in ambient conditions on the GaAs surface: it consists of a mixture of Ga- and As-related oxide compounds [28]. It is challenging to remove this oxide in the sputtering chamber without damaging the surface. Instead, we demonstrate the importance of the oxide by passivating the GaAs substrate: after removal of the natural oxide, a 10-nm-thick alumina (Al_2O_3) layer is deposited by atomic layer deposition [29]. We find that Mo-Si deposited on a passivated GaAs substrate exhibits an identical critical temperature to that of Mo-Si on a Si substrate.

Based on Ginzburg-Landau theory, Simonin has developed a model describing the correlation between the critical temperature T_c and the film thickness d of a superconducting material [26]:

$$T_c = T_{\mathrm{co}}(1 - d_c/d), \tag{1}$$

where T_{co} is the critical temperature of the bulk material and d_c is the critical thickness below which the superconducting properties of the material disappear. The critical temperatures for different thicknesses can be extracted from Fig. 1(a) and are shown in Fig. 1(b), a plot of T_c versus $1/d$. Fitting the Simonin model to the data results in $T_{\mathrm{co}} = 6.71 \pm 0.07$ K and $d_c = 1.38 \pm 0.03$ nm for deposition on the Si substrate; with $T_{\mathrm{co}} = 6.79 \pm 0.23$ K and $d_c = 1.87 \pm 0.10$ nm for the GaAs substrate. The intercept with the y axis represents the critical temperature of the bulk material and is identical (within the uncertainties in the fit parameters) for Si and GaAs. This can be explained by the fact that the influence of the substrate decreases with increasing thickness. Starting from bulk material, the critical temperature decreases for decreasing thickness, more rapidly for GaAs than for Si.

Finkel'stein has proposed a law connecting the critical temperature T_c with the sheet resistance R_s in the resistive phase [27]:

$$\frac{T_c}{T_{\mathrm{co}}} = \exp(\gamma)\left(\frac{1-\chi}{1+\chi}\right)^{1/\sqrt{2r}}, \tag{2}$$

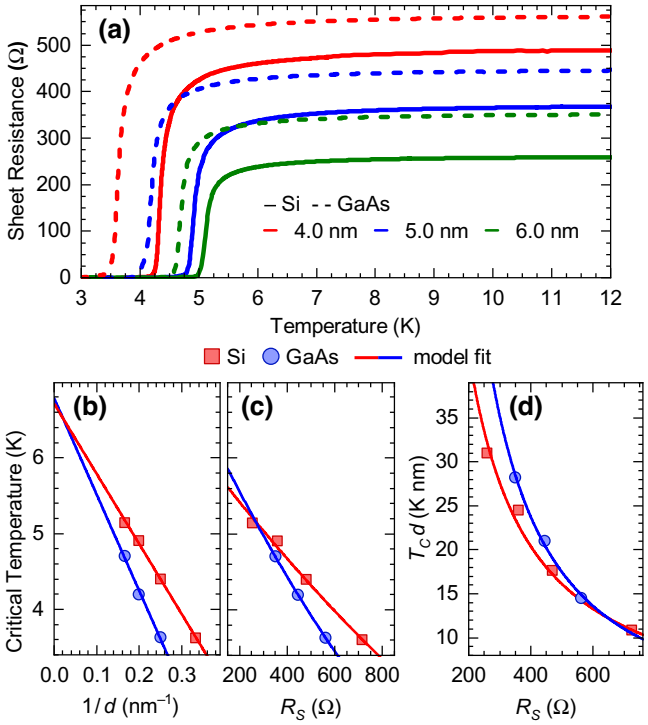

FIG. 1. The superconducting transition temperature and sheet resistance in the resistive phase versus the film thickness for films on Si and GaAs substrates. (a) The sheet resistance versus the temperature for $Mo_{0.69}Si_{0.31}$ layers of three different thicknesses deposited on a silicon surface (solid) and a natural GaAs surface (dashed). (b) The critical temperature T_C versus the reciprocal of the Mo-Si-layer thickness d for deposition on Si (squares, red) and GaAs substrates (circles, blue). The data points are extracted from (a) and fitted using a function of the form $T_c = T_{co}(1 - d_c/d)$ according to the Simonin model [26], [Eq. (1)]. On Si, $T_{co} = 6.71 \pm 0.07$ K and $d_c = 1.38 \pm 0.03$ nm; on GaAs, $T_{co} = 6.79 \pm 0.23$ K and $d_c = 1.87 \pm 0.10$ nm. (c) The critical temperature T_C versus the sheet resistance R_S extracted from (a) and fitted according to the Finkel'stein model [27] [Eq. (2)]. On Si, $T_{co} = 6.22 \pm 0.07$ K and $\gamma = 7.40 \pm 0.06$; on GaAs, $T_{co} = 6.82 \pm 0.03$ K and $\gamma = 8.35 \pm 0.02$. (d) $T_C \times d$ versus R_S for different thicknesses of Mo-Si deposited on Si (red, square) and on GaAs (blue, circle), extracted from (a). The data are fitted to Ivry's universal scaling law [Eq. (4)].

where

$$\chi = \left(\frac{\sqrt{r/2}}{r/4 + 1/\gamma}\right) \quad \text{and} \quad r = \frac{e^2}{2\pi^2\hbar}R_s, \tag{3}$$

$\hbar$ is the reduced Planck's constant, e is the elementary charge, and γ is a fit parameter. This model was originally developed for quasi-two-dimensional films. However, it has been shown that the model gives realistic values for the mean scattering time, the diffusion constant, and the electron density even for films with a thickness larger than the mean free path [30]. In Fig. 1(c), we show fits of the data to Finkel'stein's law. We obtain values of $T_{co} = 6.22 \pm 0.07$ K, $\gamma = 7.40 \pm 0.06$ for Mo-Si on a Si substrate; and $T_{co} = 6.82 \pm 0.03$ K and $\gamma = 8.35 \pm 0.02$ on a GaAs substrate. These high values of γ indicate an amorphous structure of the superconducting layer [27]. Banerjee *et al.* have extracted values of $T_{co} = 7.8$ K and $\gamma = 7.66 \pm 0.1$ for $Mo_{0.83}Si_{0.17}$ [30]. The higher value of T_c with respect to our results is a consequence of the higher concentration of Mo in the material.

From Finkel'stein's law, we estimate an electron scattering time in the resistive state at room temperature of 7.5×10^{-16} s for the Mo-Si film of 6-nm thickness. From the Drude law, this gives an estimation of the electron density, $n \simeq 3.2 \times 10^{-28}$ m^{-3}. [We have not attempted to determine n directly from a measurement of the (very small) Hall resistance.] In turn, this gives a value of the Ioffe-Regel parameter $k_F L$ (where k_F is the Fermi wave vector and L the mean free path) of $k_F L \simeq 8.3$. This value, well above 1, indicates moderate disorder as far as the electron motion is concerned [31].

For thin films near the superconducting-to-resistive transition, the connection between the critical temperature T_c, the film thickness d, and the sheet resistance R_s can be described by a universal scaling law [32]:

$$T_c d = A R_s^{-B}, \tag{4}$$

where A and B are fit parameters. In Fig. 1(d), we show how the data fit to the universal scaling law. We obtain $A = 11\,000 \pm 7000$ and $B = 1.06 \pm 0.11$ for Mo-Si deposition on a Si substrate; and $A = 90\,000 \pm 50\,000$ and $B = 1.37 \pm 0.10$ on a GaAs substrate. (A and B are given in SI units.) The values of $B > 1$ indicate an amorphous structure [32]. Small uncertainties in the thicknesses of the Mo-Si films have a huge influence on $T_c d$ such that A cannot be determined more precisely.

The second parameter that affects the superconducting transition is the composition of the thin films. The composition can be controlled by setting the sputtering parameters via

$$\frac{n_{Mo}}{n_{Si}} = \frac{\dot{d}_{Mo}}{\dot{d}_{Si}} \underbrace{\frac{\rho_{Mo}}{\rho_{Si}} \times \frac{M_{Si}}{M_{Mo}}}_{=1.286}, \tag{5}$$

where $\dot{d}_{Mo\,(Si)}$ are the deposition rates, $\rho_{Mo\,(Si)}$ the densities, and $M_{Mo\,(Si)}$ the molar masses of Mo (Si). In Fig. 2, we depict sheet-resistance versus temperature curves for five different compositions ranging from $Mo_{0.69}Si_{0.31}$ to $Mo_{0.80}Si_{0.20}$. Smaller Mo concentrations have not been explored here. The films have thickness 6.0 nm and have been deposited on Si substrates. The curve representing the composition $Mo_{0.69}Si_{0.31}$ is identical to the one shown in Fig. 1(a) (green curve). The critical temperature increases with the Mo concentration from 5.1 to 6.9 K, whereas

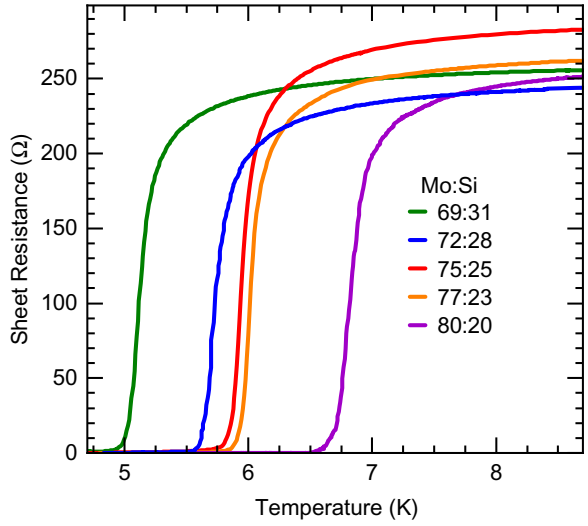

FIG. 2. The sheet resistance versus the temperature of Mo-Si films with five different compositions. The films have thickness 6.0 nm and have been deposited on Si substrates.

the sheet resistance in the resistive state remains approximately constant. Interestingly, there is a range around $Mo_{0.75}Si_{0.25}$ where the critical temperature is hardly dependent on the composition. This means that the superconducting properties are weakly dependent on fluctuations in the sputtering process, which is advantageous for repeatability and also production yield. However, we have decided to use a lower fraction of Mo (69%) for the detectors to decrease the superconducting energy gap, resulting in a high internal quantum efficiency, in particular at elevated operation temperature [24]. An even lower critical temperature can probably be achieved at lower Mo concentration but this results in an even lower operating temperature of the resultant detector and the lower critical temperature results in a lower critical current, impacting negatively the timing jitter. The choice of $Mo_{0.69}Si_{0.21}$ represents a good compromise. For an Mo concentration exceeding 80%, a regime is approached in which spontaneous crystallization can take place above a certain layer thickness, causing a sharp drop of the critical temperature [33,34].

Similar studies can be found in the literature [30,34–36]. However, our results are not directly comparable with the observations in these publications, since the exact details of the superconducting films differ in thickness and/or composition.

All these results demonstrate that thin films of Mo-Si on a GaAs substrate become superconducting at low temperature, with a critical temperature only slightly impaired with respect to equivalent films on a Si substrate.

III. FABRICATION OF MEANDER-TYPE SNSPDs ON GALLIUM ARSENIDE SUBSTRATES

We fabricate SNSPDs on GaAs. The nanowire has a meander design and photons are coupled from the top via a single-mode optical fiber. In Fig. 3(a), we sketch the main steps in the SNSPD fabrication. The starting point for the fabrication process is a GaAs wafer (green).

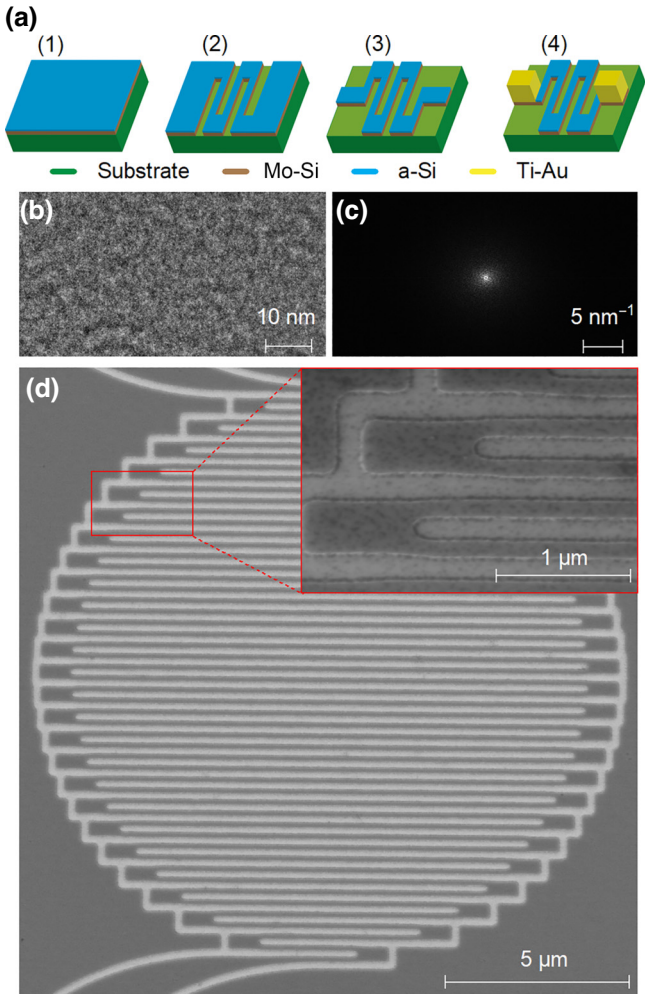

FIG. 3. (a) The process flow for SNSPD fabrication: (1) deposition of the superconductor; (2) nanowire patterning; (3) device isolation; (4) partial removal of protective Si layer and deposition of contact pads. (b) A TEM image of a 6-nm-thick layer of Mo-Si capped by a 3-nm-thick layer of amorphous silicon. (c) The Fourier transform of (b). (d) A SEM image of a nanowire featuring a width of 130 nm: dark gray, superconductor; light gray, substrate.

The first step (1) is the deposition of a 6-nm-thick $Mo_{0.69}Si_{0.31}$ film (brown) followed by a 3-nm-thick amorphous-silicon capping layer (blue) that prevents the superconductor from oxidizing. To prove the amorphous character of the film, we investigate the Mo-Si layer in a transmission-electron microscope (TEM). For this purpose, we deposit the Mo-Si film on pioloform-coated 400-mesh copper grids that are transparent for electron beams. In Fig. 3(b), we show a TEM image recorded with an acceleration voltage of 200 kV and a magnification of 500 k. The corresponding Fourier transformation is depicted in

Fig. 3(c) and shows clearly the amorphous character of the superconducting film. To verify the composition, we have performed an X-ray photoelectron spectroscopy measurement.

The second step (2) is to pattern the Mo-Si layer into meander nanowires covering an area of 8 μm radius. This is carried out via electron-beam lithography and inductively coupled plasma (ICP) etching. The nanowires are etched using an SF_6-Ar plasma. The addition of Ar ions leads to physical etching, and also sputtering, which reduces the edge roughness of the etched structures [6]. Each chip contains nanowires featuring different widths (100–150 nm) and fill factors. In Fig. 3(d), we show a scanning-electron microscope (SEM) image of a nanowire featuring a width of 130 nm and a gap of 120 nm. At this point, the superconducting material covers also the space in between the individual nanowires such that all the detectors are short circuited. To overcome this issue, the superconducting material is removed between the contact pads of the different SNSPDs using UV lithography. We call this step device isolation, step (3). The final step (4) is the fabrication of the electrode pads consisting of titanium and gold (orange) with thicknesses of 10 nm and 90 nm, respectively. To provide an electrical contact with low resistance, the amorphous-silicon protection layer is locally removed beforehand via Ar milling.

IV. TESTING OF DETECTOR EFFICIENCY, TIMING JITTER, AND RECOVERY TIME

We have fabricated SNSPDs on two different types of substrates, a GaAs substrate with a native oxide at the surface and a passivated GaAs substrate. The superconducting material is a 6-nm-thick layer of Mo-Si (composition 69:31), protected by a 3-nm-thick amorphous-silicon layer. The SNSPDs are characterized with a flood-illuminated setup (see Fig. 4). The SNSPD is placed in a three-stage cryostat and is cooled down to 0.9 K. The electrical readout circuit contains a bias tee, allowing us to apply the direct current of a constant current source while measuring the rf output signal of the detector. The voltage signal from the ac port is amplified twice, at cryogenic temperature and subsequently at room temperature, and is fed to a time-tagging machine.

The device functions as a single-photon detector—a series of voltage pulses is created at the output in the presence of the weak optical excitation. Without the optical excitation, the count rate, i.e., the dark count-rate, is very small. To measure the detection rate, we have employed a continuous-wave (cw) laser, which is attenuated by three variable optical attenuators (A, B, and C) so that the detector is illuminated by single photons. The signal-versus-current curve is shown in Fig. 5(a). It exhibits a plateau at large currents (red curve, wavelength $\lambda = 980$ nm, temperature $T = 0.9$ K, and passivated GaAs). The plateau is

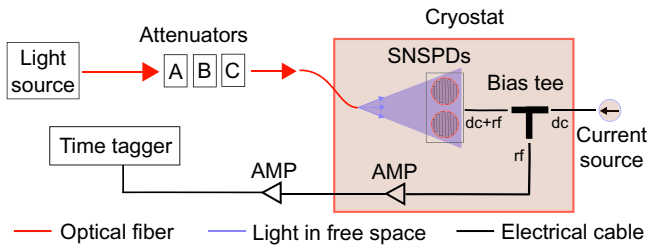

FIG. 4. An overview of the flood-illumination setup used to test the single-photon detectors. The output signal of a cw laser is attenuated to the single-photon level by three variable attenuators, A, B, and C. The detectors are placed in a three-stage cryostat at temperatures between 0.9 and 2.2 K. The electrical output signal of the detection circuit is fed to a time-tagging machine. AMP, amplifier.

important—it demonstrates that the internal quantum efficiency is only limited by properties of the material and not by the temperature or fabrication errors [13]. The plateau can therefore be used as a proxy to determine the quantum efficiency of the Mo-Si-on-GaAs detector.

It is known that nanowires of this Mo-Si material on silicon give high detection efficiencies: the absorption of a photon results in a resistive region and hence a voltage pulse at the output with almost total certainty, provided that the material is biased in the plateau region [37]. We argue therefore that on GaAs, it is possible to achieve efficiencies as good as the ones on silicon, above 80%, if the typical SNSPD structure is made, including a mirror and a cavity [22,37]. We note that the use of epitaxially grown GaAs as a substrate, as is the case here, offers an excellent way of equipping an SNSPD with a bottom mirror. An almost lossless Bragg mirror can be incorporated in the substrate by epitaxial growth of a GaAs/AlAs Bragg mirror. It can be designed such that there is a field maximum at the surface.

The dark count-rate increases drastically for currents above 16 μA. The origin of this behavior is the sections along the nanowire with a reduced cross section, named constrictions [9,38]. The blue circles in Fig. 5(a) indicate the dark count-rate plotted on a logarithmic scale. The critical current in this case is 18 μA.

We access the timing uncertainty, the timing jitter, of our fiber-coupled detectors. For this, we plug a pulsed picosecond-laser (wavelength 1064 nm) and record the count rate in histogram mode as shown in Fig. 5(b). The jitter is defined as the full width at half maximum (FWHM) and is determined to be 50 ps for a detector on the passivated GaAs substrate. The measurement shows a non-Gaussian tail, which becomes more pronounced at higher detection wavelengths. This behavior has been reported in previous experiments [37,39], and is described theoretically by a combined effect of Fano fluctuations and a spatial nonuniformity of the nanowire [40,41].

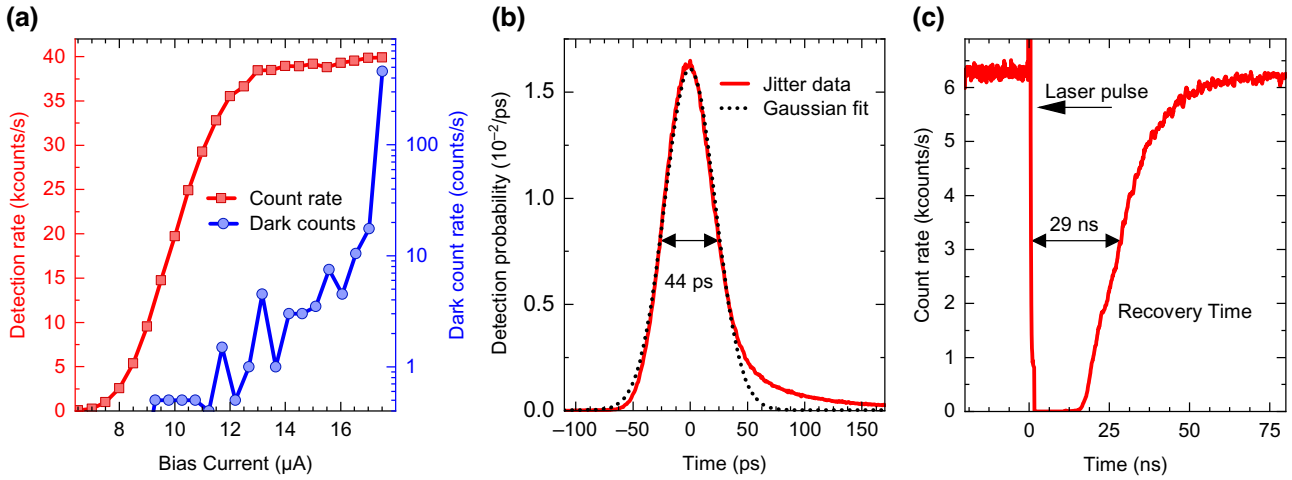

FIG. 5. A single-photon detector test on passivated GaAs at a wavelength of 980 nm. (a) The detection rate (red, squares) and dark count-rate (blue, circles) as a function of the bias current. (b) Jitter and (c) recovery-time measurements.

The recovery time is defined as the time required following a detection event for the detector to recover half of its efficiency [42]. It can be determined using a hybrid-autocorrelation method [43]. This requires both a pulsed laser and a cw laser. The pulses contain a few tens of photons per pulse, such that each pulse results in a detector click with a high probability. First, the pulsed laser triggers an initial detection event, after which the cw laser makes the detector click at a random time. We have recorded the count rate in dependence on the time relative to the initial detection event at time $t = 0$. The result of this measurement (passivated GaAs substrate, wavelength 980 nm) is shown in Fig. 5(c). The recovery time is determined to be 29 ns.

Table I (upper half) shows an overview of the results of the detector tests differing in laser wavelength and substrate material. All the tested detectors feature an identical nanowire design. Corresponding plateau curves, which we use as a measure for efficiency, are shown in Fig. 6(a). The red curve (passivated substrate, 980-nm wavelength) is identical to that in Fig. 5(a). On passivated GaAs, the plateau extends from 13 to 18 μA (wavelength 980 nm). At a detection wavelength of 1550 nm (green curve), the count rate starts to rise at higher bias currents compared to the response measured at 980 nm (red curve). Even at 1550-nm wavelength, the onset of the plateau is visible. Detection using Mo-Si on native oxide GaAs (980 nm, blue curve) works similarly well but the relative length of the plateau is shorter (19% with respect to the bias current I_C, where I_C is defined as the current at which the dark count-rate reaches 1 kcount/s) compared to the detector on the passivated substrate (relative plateau length 26%). As a consequence, a plateau is not observed at 1550-nm wavelength using native GaAs (orange curve). For the detection at wavelength 980 nm, we obtain a timing jitter of 64 ps on native GaAs and 50 ps on passivated GaAs. The corresponding recovery times are 56 and 29 ns, respectively. This significant difference is due to the shape of the detection rate curve with respect to the bias current: this shows a longer plateau in the case of the passivated sample. Hence the bias current can reflow more quickly after a detection event to a value where the efficiency is maximal [43]. The test at wavelength 1550 nm results in timing jitters of 65 and 55 ps and recovery times of 73 and 65 ns on native GaAs and passivated GaAs, respectively.

TABLE I. A summary of the various detector tests.

Wavelength (nm)	GaAs substrate	Temperature (K)	Bias current (μA)	Efficiency	Jitter (ps)	Recovery time (ns)
980	Native	0.9	14.0	Saturated	60	56
980	Passivated	0.9	16.5	Saturated	50	29
1550	Native	0.9	14.0	Not saturated	64	73
1550	Passivated	0.9	16.5	Almost saturated	55	65
980	Passivated	0.9	16.5	Saturated	50	28
980	Passivated	1.5	15	Saturated	56	34
980	Passivated	2.2	11.5	Saturated	...	49

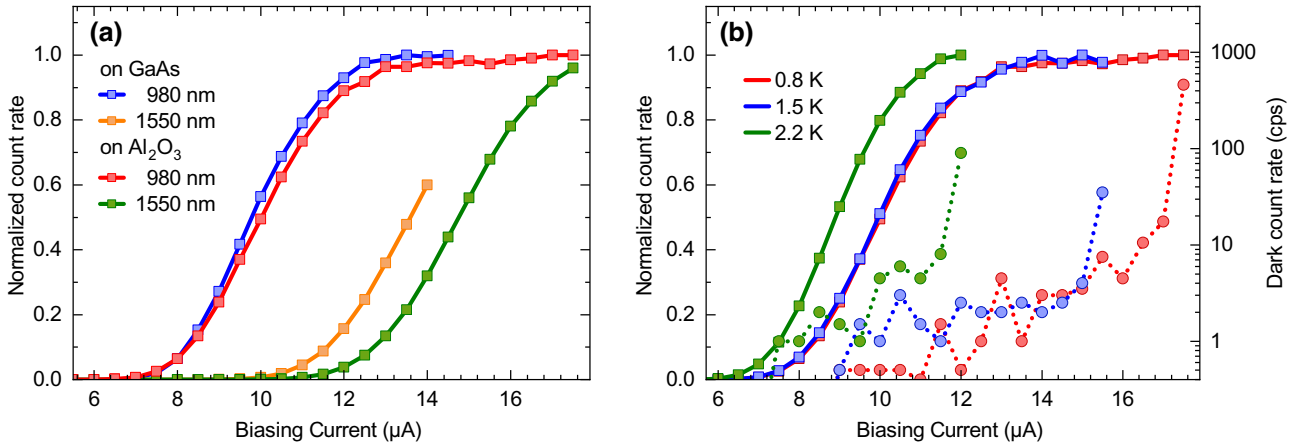

FIG. 6. (a) A single-photon detector test on both passivated GaAs and unpassivated GaAs at wavelengths of 980 nm and 1550 nm and at a temperature of 0.9 K. The normalized detection rate is plotted against bias current in each case. (b) Temperature dependence of the normalized detection rate and dark count-rate versus bias current for the detector in (a) on passivated GaAs at a wavelength of 980 nm.

These results show that passivating the GaAs surface with aluminum oxide (Al_2O_3) improves the detector performance. However, the detectors on native GaAs also have excellent properties, especially for wavelength 980 nm and below. These wavelengths are important for the on-chip detection of single photons emitted by InAs quantum dots.

InAs quantum dots in GaAs can operate at elevated temperatures of 4.2 K. Therefore, it is also interesting to see how the detectors behave at higher temperature. Table I (lower half) shows a detector test at temperatures of 0.9, 1.5, and 2.2 K, performed on an SNSPD on passivated GaAs. The incident photons have a wavelength of 980 nm for the measurements of the efficiency and the recovery time and 1064 nm for the jitter measurement. The plateau curves are shown in Fig. 6(b), as well as the corresponding dark count-rates. The data for detection at 0.9 K (red) are identical to those in Fig. 5(a) and show a saturated internal quantum efficiency for currents between 14 and 17 μA. Detection at a higher temperature of 1.5 K (blue) results in a shorter plateau, extending from 14 to 15.5 μA. At the even higher temperature of 2.2 K (green), only the onset of the plateau is visible. Additionally, the counts-versus-current curve is shifted toward lower bias currents. The reason for this is that the phase transition depends on both temperature and electrical current: the critical current decreases with increasing temperature. For the timing jitter, we have determined a value of 50 ps at a temperature of 0.9 K and 56 ps at 1.5 K. The recovery time is 28 ns at a temperature of 0.9 K, with 34 and 49 ns at 1.5 and 2.2 K, respectively. Overall, we note that the SNSPD performance does not decrease significantly from 0.9 to 1.5 K and we achieve saturated internal quantum efficiency even at 2.2 K. This obviates the necessity of a subkelvin system, at least at the near-infrared wavelengths relevant for quantum dot photons.

V. CONCLUSIONS AND OUTLOOK

We have carried out ultrahigh-vacuum sputtering of thin-film Mo-Si on both silicon and GaAs substrates. We have found that:

(i) Thin Mo-Si films deposited on the native GaAs oxide superconduct but with a slightly lower critical temperature than Mo-Si on silicon.

(ii) Mo-Si on silicon has a composition-independent critical temperature for Mo concentrations between 72% and 77%, for a film thickness of 6 nm.

(iii) Mo-Si deposited on a passivated GaAs surface (passivation layer Al_2O_3) has the same critical temperature as Mo-Si deposited on silicon.

For all three substrates (silicon, passivated GaAs, and native GaAs), the superconducting properties follow the standard scaling with respect to film thickness and resistivity above the critical temperature.

The Mo-Si thin films have been used in the fabrication of SNSPDs in a meander-wire geometry. We find that:

(a) Mo-Si SNSPDs on both passivated and native GaAs demonstrate a plateau in the signal-bias response at wavelength 980 nm, indicating an excellent quantum efficiency. A plateau is observed up to a temperature of 2.2 K.

(b) Mo-Si SNSPDs on passivated GaAs have a higher critical current and a higher plateau extent than those on native GaAs.

(c) The SNSPD metrics (quantum efficiency, dark count-rate, timing jitter, and recovery time) of Mo-Si SNSPDs on GaAs are state of the art and match those of cofabricated Mo-Si SNSPDs on Si.

We have thereby demonstrated that Mo-Si, an amorphous superconductor, works well as a SNSPD on

GaAs. Our SNSPDs are based on a 6-nm-thick film of $Mo_{0.69}Si_{0.31}$. For the vertically coupled meander-wire geometry employed here, the quantum efficiency can be improved most simply by incorporating a Bragg mirror in the GaAs substrate. Marginal gains may be possible by optimizing the Mo-Si composition and nanowire geometry. However, the crucial next step is to integrate SNSPDs with GaAs photonic circuits, ideally also integrating quantum dots as single-photon emitters. Here, the switch from Nb-Ti-N to Mo-Si is likely be very beneficial in terms of fabrication simplicity and detector yield.

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