Ternary cold source transistors for multivalue logic applications

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A ternary cold source field effect transistor (T-CSFET) is proposed based on source density-of-state engineering, using a narrow-band-gap semiconductor at the source region. A current plateau at the subthreshold region is obtained in the transfer characteristics of T-CSFETs, namely an intermediate state with a constant current between on and off states. We meticulously study a two-dimensional T-CSFET based on a graphene-MoS_2 heterojunction by quantum transport simulations. It is shown that ternary states can be well distinguished with a current ratio between two adjacent states of over 10^3 at a low overall supply voltage of 0.6 V. The intermediate state is stable with a constant current in a gate voltage region over 0.2 V and can be modulated by varying the doping density. We also obtain ternary transfer curves for T-CSFETs based on one-, two-, and three-dimensional materials. Based on T-CSFETs, a two-bit ternary adder with hybrid logic is implemented and verified by circuit simulations. The proposed T-CSFETs exhibit excellent properties for multivalue logic, including high drive current, tunable multivalue states, stable and reliable operation, energy and area efficiency, and a variety of material systems.

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I. INTRODUCTION

The traditional von Neumann architecture, based on binary field effect transistors (FETs), is a key feature of current state-of-the-art information processing technology [1]. The computational efficiency of such a computing system is constantly improved by the relentless geometrical scaling of FETs. However, the reduction of device size is approaching the fundamental limit, which may slow down further improvements in the computing capability of the von Neumann architecture. Furthermore, the binary logic gates as the building block of the von Neumann system limit the improvement of data processing. Innovative approaches are much desired for increasing the functionalities and capabilities of computing systems. Multivalue logic (MVL) having three or more states has been considered as a promising alternative [2,3], because of the capability of delivering higher information density and reducing the number of operations. By moving from a binary logic system to a ternary logic system, the system complexity can be reduced to 63%($\log_3 2$) [4]. Therefore, the computational density, frequency of data reads, total latency, and power consumption can be improved in MVL systems.

Ternary logic as a typical MVL is the most promising approach due to its simplicity and similarity to current binary computing, and it has been mathematically proved that the ternary system is the most efficient [4]. As early as the 1970s, attempts were made to implement ternary logic by using binary MOSFETs through complex circuit designs [5,6], while high power consumption and interconnect delay are unavoidable. Then, ternary circuits based on different threshold voltage transistors were proposed [7,8]. However, it is necessary to implement multiple logic states in a single device to reach area and energy efficiency. Various ternary devices have been developed to realize efficient MVL circuits, such as quantum dot gated transistors [9,10], anti-bipolar transistors [11], negative transconductance devices [12], and negative differential resistor (NDR) devices [13,14].

In this work, a ternary cold source FET (T-CSFET) is proposed by source density-of-states regulation using gapped materials. A narrow-band-gap semiconductor is applied in the source region for realizing a plateau of current in transfer characteristics and achieving ternary states. Quantum transport simulations show that ternary states and high on-state currents of over 10^2 $\mu A/\mu m$ are achieved in monolayer MoS_2 FETs by using gapped graphene. It is also demonstrated that such a device can be constructed by using one-dimensional (1D) graphene nanoribbon, two-dimensional (2D) Ti_2Cl_4-MoS_2, and three-dimensional (3D) InAs-Si heterojunctions for both energy and area efficiency. Fundamental ternary logic operations are demonstrated by using T-CSFETs with the minimum number of gates compared with other ternary transistors [7,8]. Finally, a two-bit ternary full adder is designed with ternary logic

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on the basis of T-CSFETs to verify the functional integrity. We make a comparison between the T-CSFET and other multivalue logic devices, which shows the advantages of the T-CSFET, such as high drive current, low supply voltage, energy and area efficiency, and reliable ternary operation.

II. QUANTUM TRANSPORT SIMULATIONS

To simulate the quantum transport properties of T-CSFETs based on a graphene-MoS_2 heterojunction, we use the Dirac model combined with the nonequilibrium Green's function (NEGF) method. Graphene and monolayer (ML)-MoS_2 are 2D Dirac materials, and their low-energy Dirac cones can be described by a Dirac Hamiltonian [15,16]:

$$\widehat{H}_0 = at\left(\tau k_x\hat{\sigma}_x + k_y\hat{\sigma}_y\right) + \frac{\Delta}{2}\hat{\sigma}_z, \quad (1)$$

where a is the lattice constant, t is the nearest-neighbor intralayer hopping, and Δ is the band gap. $\hat{\sigma}$ denotes Pauli matrices accounting for the sublattice index of graphene and the two basis functions of ML-MoS_2. Such a model can simultaneously describe massless electrons in graphene and mass electrons in monolayer MoS_2 [16]. With the Dirac Hamiltonian, quantum transport properties are calculated by self-consistently solving the Poisson equation and Schrödinger equation with the nonequilibrium Green's function formalism [17]. We compare the I_D-V_G curves of 15-nm double-gate MoS_2 FETs, obtained using the Dirac and atomistic tight-binding Hamiltonian-based NEGF method [18]. The results indicate that the transfer characteristics closely align between the two methods, which proves that the two-band Dirac Hamiltonian can well describe the quantum transport behavior of MoS_2 devices.

The electrical properties of 2D and 3D materials and the transport characteristics of p-n junctions are calculated by first-principles quantum transport simulations based on NEGF density functional theory (DFT), implemented in Nanodcal software [19]. The used exchange-correlation function is the generalized gradient function of Perdew-Burke-Ernzerhof (GGA-PBE96), and the cutoff energy is set to 80 Hartree. The k-point samplings are $10 \times 10 \times 10$ and $1 \times 10 \times 10$ for the electrode and central scattering region of 3D InAs, respectively. The k-point samplings are $100 \times 12 \times 1$ and $1 \times 12 \times 1$ for 2D Ti_2Cl_4. All calculations are carried out at a temperature of 300 K. The band gap of ML-MoS_2 obtained by using the GGA is underestimated but large enough to suppress the off-state current in a MoS_2 transistor. It has been shown that the energy difference between energy affinities of monolayer MoS_2 by using the GGA and hybrid functionals is about 0.03 eV [20]. At the same time, the threshold voltage shift due to the band alignment difference can be modulated by metal gate work function engineering [21].

III. RESULTS AND DISCUSSION

A. Device structure and physical operation

The schematic device structure of our proposed cold-source principle-based ternary logic transistor is shown in Fig. 1(a) (taking n-type FET as an example). The difference between the structure and a conventional FET (CFET) is the addition of a cold-source structure with a narrow band gap in the source region. Such a device structure has the potential to be compatible with the current state-of-the-art process by selecting suitable source semiconductor materials. In the source region, the semiconductor band gap above the Fermi level is used to achieve the regulation of the density distribution of the injected electron states and realize ternary states. Figure 1(b) shows a schematic I_D-V_G curve of the T-CSFET in logarithmic coordinates. Different from CFETs with current increasing exponentially with V_G, there is a plateau region of drain current between on and off states. Therefore, there are ternary states in the proposed device. Moreover, due to the current plateau appearing in the subthreshold gate voltage region with low carrier concentration, electron-electron scattering rate tends to be small [22–25], yet it can lead to a notable decrease in carrier drift velocity [25]. This effect manifests in the device as a reduction in subthreshold current and a downward shift of the plateau current, which should be considered in actual device design.

The schematic working mechanism of T-CSFETs is illustrated in Figs. 1(c)–1(f). Figure 1(c) shows the band profiles of T-CSFETs at V_0 in Fig. 1(b). The energy band diagram of T-CSFETs can be divided into two parts: a narrow-band-gap cold source on the left and a general transistor on the right. For a CFET, the lowering of the top of the channel barrier E_{top} increases the current exponentially in the subthreshold voltage region. At V_0, the energy of E_{top} is larger than that of the band gap's top edge E_{C0} of the cold source. As the gate voltage is increased from V_0 to V_1, the current is increased exponentially as in CFETs. As the gate voltage reaches V_1 as shown in Fig. 1(d), the energy of E_{top} gets smaller than E_{C0}. As long as the channel is long enough, the tunneling current can be ignored and the drain current is mainly composed of the thermionic current over the channel barrier. Because there is a narrow band gap in the source, the current is determined by electrons with energy larger than E_{C0} as V_G is increased from V_1 to V_2, as shown in Fig. 1(e). Therefore, the drain current does not increase with V_G and there is a plateau region as shown in Fig. 1(b). As V_G is further increased to V_3, the energy of E_{top} gets smaller than the band gap's bottom edge E_{V0} of the cold source in Fig. 1(f). Then, the drain current is increased from V_3 and V_4 as shown in Fig. 1(b). It should be noted that the subthreshold swing (SS) can be smaller

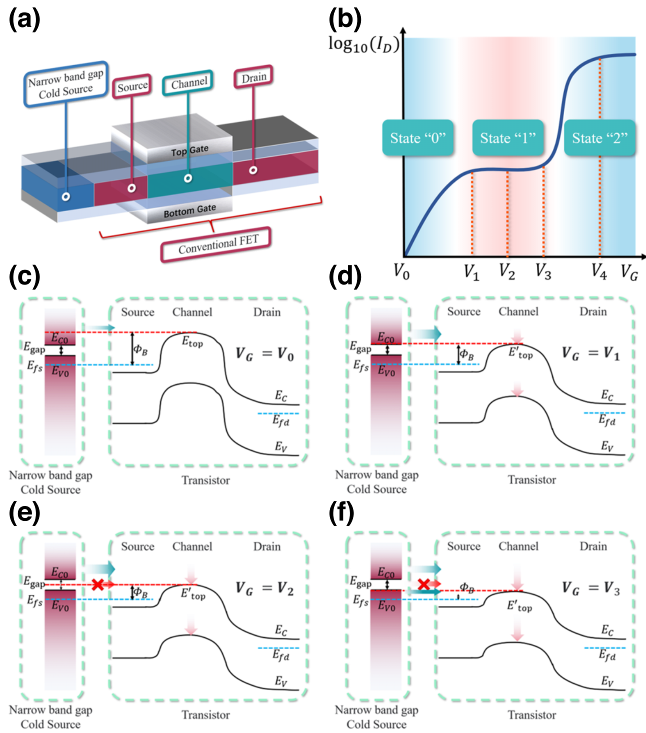

FIG. 1. Schematic device structure of T-CSFET and physical mechanism. (a) The device structure of cold-source principle-based ternary logic transistor, consisting of a narrow-band-gap cold source and a transistor. Note that V_G is applied to both the top and bottom gates with identical values. (b) Schematic I_D-V_G curve of T-CSFETs. There is a current plateau region as an intermediate state between on and off states. Schematic energy band diagrams at different gate voltages: (c) $V_G = V_0$, (d) $V_G = V_1$, (e) $V_G = V_2$, and (f) $V_G = V_3$.

than the thermionic limit of 60 mV/decade from V_3 and V_4 due to the cold source effect [15,26], which is beneficial for reducing the operation voltage.

The ternary states of T-CSFETs are affected by the band gap and the band gap's bottom edge of the cold source semiconductor. The band gap cannot be too large to realize ternary states and reduce the supply voltage. The energy of the valence band maximum (VBM) of the source semiconductor determines the location of the current plateau region, which should be between the on- and off-state currents. Therefore, the ternary states can be adjusted by modulating the band gap and doping density of the cold source semiconductor. Furthermore, an I_D-V_G curve with more current plateaus can be achieved by inducing more band gaps in the cold source material (see Supplemental Material for Fig. S1 [27], and Refs. [26,28]).

B. Device simulations of T-CSFETs

To manifest the proposed device mechanism, we perform quantum transport simulations of T-CSFETs based on a graphene-MoS_2 heterojunction. Figure 2(a) shows the

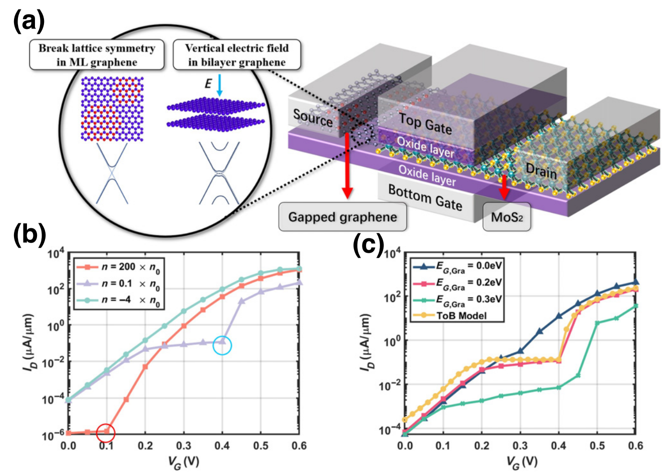

FIG. 2. Device simulations of T-CSFETs. (a) The device structure of MoS_2 FETs with a gapped graphene source. An energy gap can be induced in monolayer graphene by breaking the A-B site symmetry and in bilayer graphene by a vertical electric field. Note that V_G is applied to both the top and bottom gates with identical values. (b) Transfer characteristic curves of the device with gapped graphene $E_{G,\mathrm{Gra}} = 0.2$ eV at different doping densities ($n < 0$ for n-type doping and $n > 0$ for p-type doping). Note that V_G is applied at the top gate and bottom gate with the same value as in the simulation. (c) Transfer characteristics of the device with different graphene band gaps with a fixed doping ($n = 0.1 \times n_0$).

device structure of MoS_2 FETs with a graphene source. It is a double-gate structure with HfO_2 gate oxide layers, gapped graphene of 20 nm in the source region, and MoS_2 of 15 and 20 nm in the channel and drain, respectively. Graphene and monolayer MoS_2 are described by the two-band Dirac model, and the interlayer coupling is fitted with DFT results [15]. Graphene is gapless and has linear density of states (DOS) as a function of energy around the Dirac point. Therefore, a low-pass energy filter using graphene is enabled to reach a cold electron injection. The superexponential distribution of injected current is realized, and SS can break the thermionic limit of 60 mV/decade, which has been achieved experimentally [29]. It has been reported that an energy gap of about 250 meV can be induced in monolayer graphene by breaking the A-B site symmetry [30] and in bilayer graphene by a vertical electric field [31]. As gapped p-type graphene is applied as the injection source, high-energy electrons in the thermal tail can be more efficiently filtered and a steeper SS can be achieved.

Based on the above analysis, we simulate the electrical and quantum transport properties of the MoS_2 FETs with gapped graphene $E_{G,\mathrm{Gra}} = 200$ meV [as shown in Fig. 2(a)]. Figure 2(b) shows the transfer characteristic curves of the device obtained by varying the doping concentration. Note that the value of n indicates the average doping of electrons ($n < 0$) or holes ($n > 0$) at each lattice

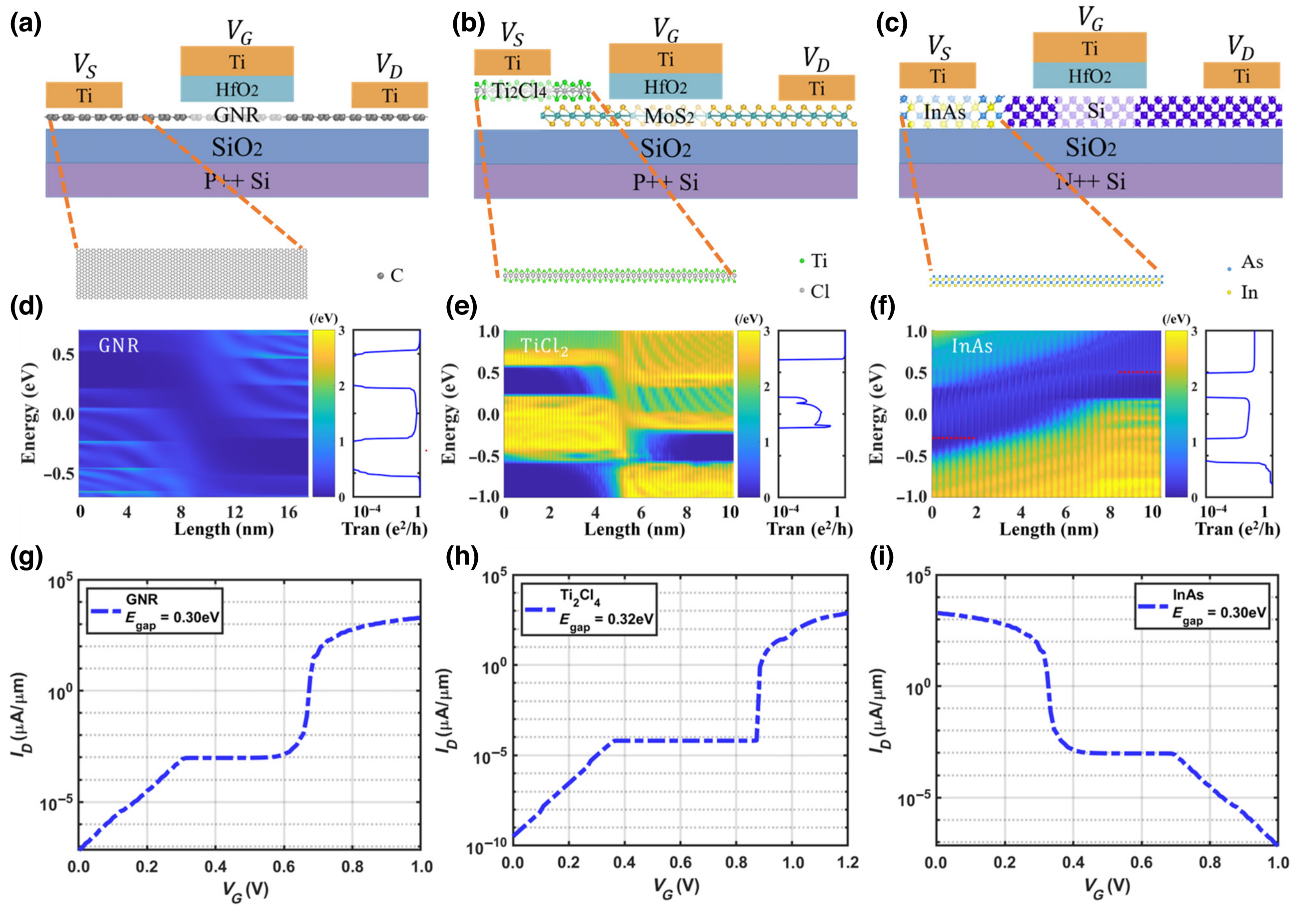

FIG. 3. T-CSFETs based on 1D, 2D, and 3D materials. Device structures of T-CSFETs using (a) 1D graphene nanoribbon heterojunction, (b) 2D Ti_2Cl_4-MoS_2 heterojunction, and (c) 3D InAs-Si heterojunction. *p-n* junctions based on narrow-band-gap semiconductors are applied as a cold source in T-CSFETs: crystal structure, LDOS, and transmission of (d) graphene nanoribbon with a width of 3.6 nm, (e) Ti_2Cl_4, and (f) InAs. Transfer characteristics of T-CSFETs: (g) graphene nanoribbon, (h) Ti_2Cl_4-MoS_2, and (i) InAs-Si.

point. When $n = -4 \times n_0$, the device is simply a conventional transistor. And when $n = 200 \times n_0$, the device is a typical cold-source transistor. There is a kink (marked with a red circle) in the I_D-V_G curve, which corresponds to where the top of the channel barrier E_{top} gets lower than the VBM of the graphene source. As the gate voltage is larger than the kink point, SS of about 28.3 mV/decade is obtained. We also study the impact of V_D on the current plateau (see Supplemental Material for Fig. S4 [27]). It is found that V_{DS} has little effect on the plateau due to excellent electrostatic control enabled by the 2D channel.

When the source doping is reduced to $n = 0.1 \times n_0$, it is interesting to find that there is a plateau region in the I_D-V_G curve as shown in Fig. 2(b), which is consistent with our schematic curve in Fig. 1(b). At the same time, the supersteep characteristics of the cold source are still maintained after the kink marked by the blue circle with SS reducing to 19.3 mV/decade. From the local density of states (LDOS) along the channel of MoS_2 FETs with gapped graphene at $V_G = 0$ V (see Supplemental Material for Fig. S2 [27]), it can be found that the top of the channel barrier is above the band gap of graphene, which is consistent with the band profile in Fig. 1(c). Therefore, the proposed switching mechanism of T-CSFETs is confirmed by device simulations. Ternary states can be optimized by changing doping and the band gap [Fig. 2(c), fixing $n = 0.1 \times n_0$] of the cold electron source. We also show the transfer characteristic curve of the top of the barrier (ToB) model fitted to the quantum transport simulation results in Fig. 2(c), which will be applied in the subsequent HSPICE circuit simulation. Based on the device switching principle, we can design T-CSFETs by using different narrow-band-gap semiconductors as the cold source. Figure 3 shows T-CSFETs based on 1D graphene nanoribbon [Fig. 3(a)], 2D Ti_2Cl_4-MoS_2 [Fig. 3(b)], and 3D InAs-Si [Fig. 3(c)] heterojunctions. The band gap of GNR decreases with the ribbon width. Therefore, a heterojunction with different widths can be applied to realize T-CSFETs. GNR with a width of 3.6 nm has a band gap of 0.30 eV and is applied as the injection source. Figure 3(d) shows the LDOS of

GNR p-n junction with $W = 3.6$ nm, which is calculated by using the NEGF formalism based on the tight-binding Hamiltonian model [17,32]. Electrons can tunnel through the junction and be confined between the VBM of p-type GNR and the conduction band minimum of n-type GNR. With the obtained transmission in Fig. 3(d), we can calculate the I_D-V_G curve by using the Landauer formula [17,33]. Similarly, we can construct T-CSFETs by using 2D and 3D materials as shown in Figs. 3(b) and 3(c). Figures 3(e) and 3(f) show the calculated LDOS and transmission of the 2D material Ti_2Cl_4 and 3D InAs p-n junctions by using the DFT-based NEGF method [19]. Monolayer Ti_2Cl_4 has an indirect band gap of 0.32 eV with anisotropic effective mass (see Supplemental Material for Fig. S3(a) [27]). The red line in Fig. 3(f) indicates the conduction band edge of InAs. Because the DOS distribution near the conduction band edge of InAs is much smaller than that of the valence band edge, the conduction band edge is less obvious in the LDOS (see Supplemental Material for Fig. S3(b) [27]). The tunneling transmission reaches 0.13 e^2 h^{-1} and the injected current can be as large as 7.28×10^2 μA/μm. The calculated direct band gap of bulk InAs is about 0.36 eV, and electron and hole effective masses are $0.03m_0$ and $0.57m_0$. Therefore, the InAs p-n junction can realize a large transmission of 0.05 e^2 h^{-1}. Transfer characteristics of Ti_2Cl_4-MoS_2 and InAs-Si are calculated with the obtained transmissions as shown in Figs. 3(h) and 3(i), respectively. The current of the plateau region is about 6.41×10^{-5} μA/μm at $0.35\ \mathrm{V} < V_G < 0.85$ V and 1.99×10^{-3} μA/μm at $0.41\ \mathrm{V} < V_G < 0.70$ V for Ti_2Cl_4-MoS_2 and InAs-Si FETs, respectively. Therefore, both kinds of devices can realize ternary states. Ternary logic gates can be built by using these devices.

C. Ternary logic gates

A ternary inverter is indispensable for building ternary circuits. The implementation of a ternary logic circuit requires three types of inverters, namely standard ternary inverter (STI), negative ternary inverter (NTI), and positive ternary inverter (PTI) [8]. The outputs (Y) of these ternary inverters are given by

$$Y_k = \begin{cases} k, & \text{if } X = 1 \\ 2 - X, & \text{if } X \neq 1, \end{cases} \tag{2}$$

where Y and X denote output and input; k is 0, 1, and 2 for NTI, STI, and PTI, respectively. Their truth tables are given in Fig. 4(a). Based on the T-CSFETs, we can use two types of structures to construct ternary inverters. The first structure is a ternary complementary-type inverter [T-CMOS; Fig. 4(b)] using two T-CSFETs (an n-type and a p-type T-CSFET), in which case we can shift the current plateau in the I_D-V_G curve by adjusting the doping at the source, and thus realize the three types of inverters (see

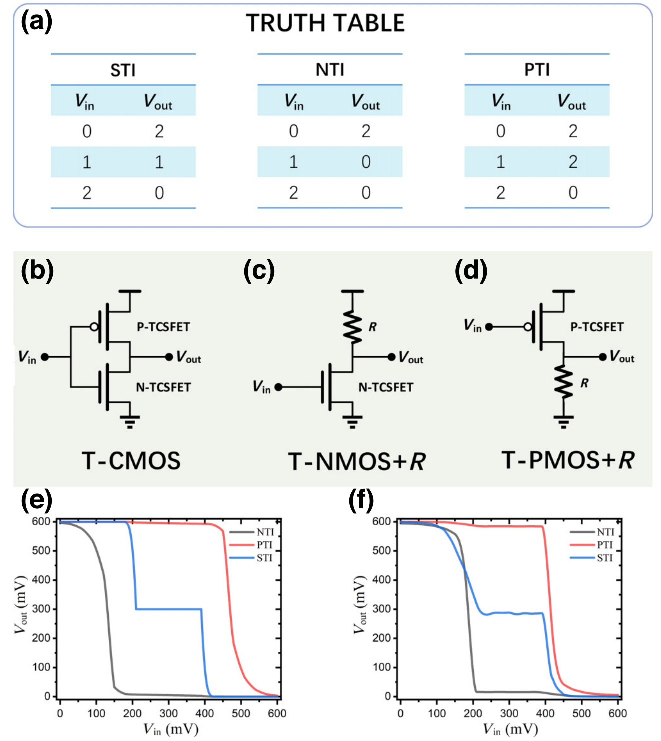

FIG. 4. Ternary inverter structures, truth table of STI, NTI, and PTI, and transfer characteristic curves. (a) The truth table of three types of ternary inverters: STI, NTI, and PTI. (b) Complementary inverter structure. (c) Resistive-inverter structure (n-type). (d) Resistive-inverter structure (p-type). Transfer characteristics of STI, NTI, and PTI based on: (e) the complementary inverter structure and (f) the two types of resistive-inverter structure.

Supplemental Material for Figs. S5 and S6 [27], where a more detailed description is shown). We can also construct ternary inverters by using a T-CSFET and a resistor (R), one with an n-type transistor in Fig. 4(c) and another with a p-type transistor in Fig. 4(d). Three types of inverters can be achieved by adjusting the resistance value of R. To the best of our knowledge, T-CSFETs require the least number of transistors and circuit elements (e.g., R) compared with other approaches to implement ternary inverters. For example, an STI based on conventional FETs has to be built with five transistors [34]. Therefore, power dissipation and integration are expected to be improved by using T-CSFETs. For the long term, an important issue affecting the development of ternary logic circuits is that an STI has relatively large static power dissipation because both pull-up and pull-down circuits of the output node are turned on when the input state of the STI is intermediate "1" [35]. The intermediate state current of the STI based on the threshold adjustment principle [36] or quantum confined principle [37] is close to the on-state current of the same order of magnitude. While, the intermediate state of T-CSFETs is in the subthreshold range, smaller than the on-state current by several orders of magnitude. Therefore,

the static power dissipation of the corresponding STI will be 2–3 orders of magnitude lower than that of multithreshold carbon nanotube field effect transistor (CNTFET) and quantum-confined FET at fixed on-current.

To simulate these inverters, a SPICE-compatible model of T-CSFETs has been developed. Figure 4(e) shows the transfer characteristic curves of the three inverters based on T-CMOS, simulated by using HSPICE. Figure 4(f) shows the transfer characteristic curves of the three inverters based on T-NMOS + R and T-PMOS + R.

We used an optimized combination to implement these three inverters (see Supplemental Material for Fig. S7 [27]). Since the device we show can achieve nearly 100% output swing, we set three states low "0," intermediate "1," and high "2" in the input voltage range 0–0.6 V corresponding to output voltages V_{out} of 0.001, 0.312, and 0.599 V. Moreover, from the voltage transfer characteristics (VTCs) in Figs. 4(e) and 4(f), we can see that the voltage gain at the adjacent state boundaries is much larger than the unit gain in both T-CMOS and T-MOS + R structure VTCs, which results in a larger static noise margin and is essential for achieving a stable and workable circuit.

The slope and width of the current plateau have a great impact on realizing an intermediate state in the transfer characteristic curve. If the current plateau is completely flat, ideal transfer characteristic curves for the three inverters can be obtained as shown in Fig. 4(e). However, the degradation of the current plateau region is inevitable due to electron-phonon or impurity scattering. Thus, it is crucial to estimate the impact of the slope of the platform on the ternary characteristics of the inverter (see Supplemental Material for Fig. S8 [27]). Our simulations reveal that the ternary characteristics of STI will gradually disappear as the slope of the platform increases until it becomes a binary inverter (see Supplemental Material for Fig. S8(b) [27]). We also find that three device parameters play important roles: (1) the operation voltage V_D, (2) the width of the plateau region: $|V_{\text{initial}} - V_{\text{end}}|$ (the voltage at the right end of the plateau minus the voltage at the left end), and (3) a parameter λ described the impact of V_D on I_D in the platform area (λ is inversely proportional to the effect of V_D on I_D) [see Supplemental Material for Figs. S8(c)–S8(e) [27]]. We conclude that the smaller these parameters are, the more pronounced is the ternary characteristic of STI, within the allowable range of the operation voltage V_D, the width of the current platform $|V_{\text{initial}} - V_{\text{end}}|$, and λ. To make the device work stably, V_D and $|V_{\text{initial}} - V_{\text{end}}|$ should not be too low. The above analysis can further guide us in the design of related devices and circuits (see Supplemental Material for Fig. S9 [27], where an example is shown).

D. Two-bit ternary adder

In addition to the basic inverters, the ternary logic circuit requires two additional circuit cells: ternary NAND and

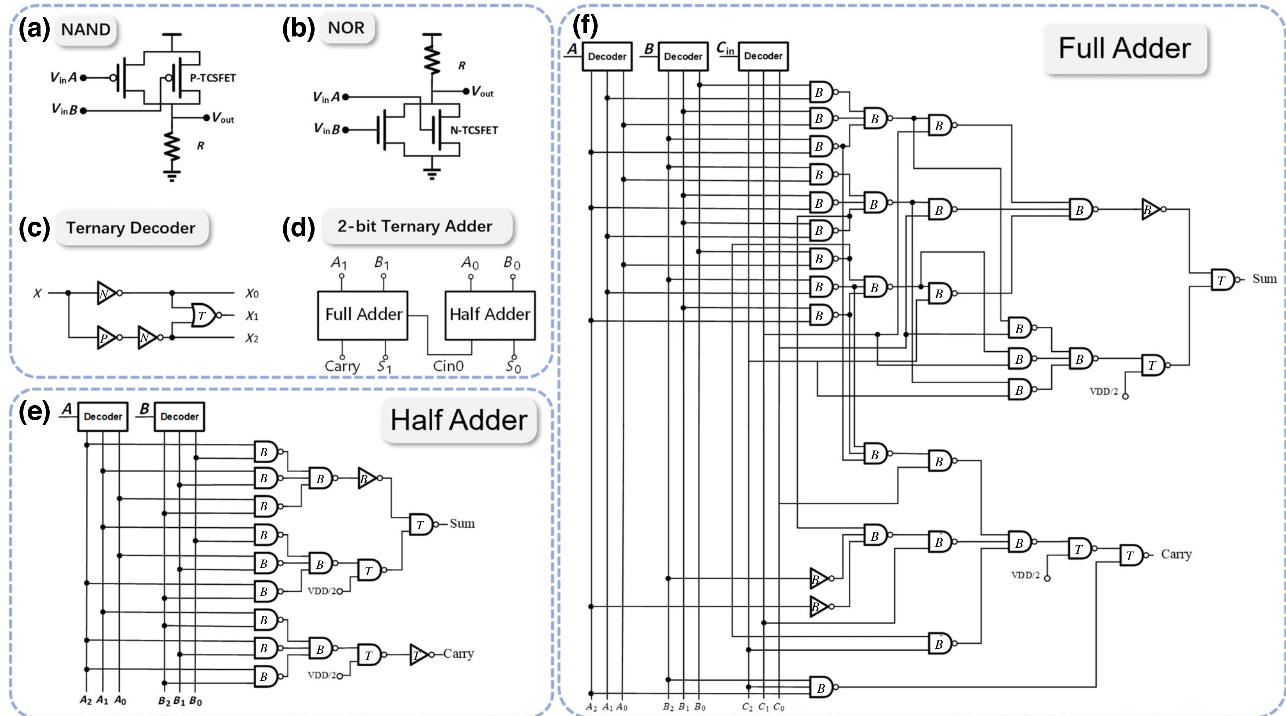

FIG. 5. The circuit diagram of ternary adder, decoder, and NOR/NAND. (a) Ternary resistive NAND. (b) Ternary resistive NOR. (c) Ternary decoder used in the adder. (d) Schematic of the complete 2-bit adder. (e) Ternary half adder. (f) Ternary full adder. Gates marked with B are binary and gates marked with T are ternary. Inverters marked with N are NTI and those marked with P are PTI.

NOR, as shown in Figs. 5(a) and 5(b). Ternary NAND and ternary NOR consist of two T-CSFETs and one resistor, which are similar to the quantum confined ternary FET [37]. In contrast, ten FETs have to be applied to realize the same function by using CNTFETs [7]. With the three basic inverters and these two circuit cells, we can implement the half adder and full adder of ternary logic, and finally combine them into a complete two-bit ternary adder. It is worth noting that we can actually build an adder of more bits or even try a full arithmetic-logic unit, but we just take a two-bit adder as an example. Figure 5(c) shows the ternary decoder, which consists of a PTI, two NTIs, and a NOR. Such a decoder converts the ternary input (X) into a high-level output and two low-level outputs as follows:

$$X_k = \begin{cases} 2, & \text{if } X = k \\ 0, & \text{if } X \neq k, \end{cases} \tag{3}$$

where k is a logic value (0, 1, or 2). A ternary half adder is designed to demonstrate the feasibility of realizing a ternary circuit using the proposed T-CSFETs in Fig. 5(e). The output of the decoder is binary and can be processed more efficiently by using binary logic. So, binary gates are used to perform a faster operation of outputs of the ternary decoder. After binary processing, ternary gates give final outputs. The half adder achieves the complete function of ternary input, binary processing, and ternary output. Such circuit design takes advantage of not only a large amount of information in the multivalue logic gates but also the computational speed of the binary logic circuit. Similarly, a full adder is designed as shown in Fig. 5(f).

A two-bit ternary adder is designed as shown in Fig. 5(d), which consists of a half adder and a full adder. To verify the function of the ternary adder, we perform circuit simulations by using HSPICE with the T-CSFETs model. The transient responses of the two-bit ternary adder are simulated with $V_D = 0.6$ V and a transient time of 0.1 ns. Voltage levels of 0, 0.3 and 0.6 V in Fig. 6 correspond to the logic states of "0," "1," and "2," respectively. For the waveforms of two-bit inputs A_1 A_0 and B_1 B_0 in Fig. 6(a), the S_1 S_0 and carry output waveforms are obtained in Fig. 6(b), which meet our design expectations. The circuit function is well verified with only a few "glitches" originating from timing errors, which can be easily eliminated with proper device optimization.

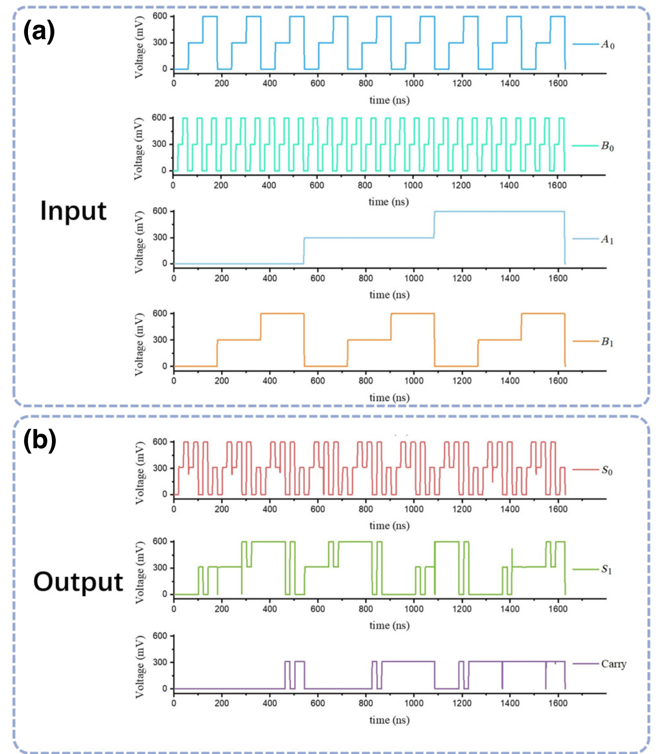

FIG. 6. Transient responses of two-bit adder input (A_0, B_0, A_1, B_1) versus output (S_0, S_1, Carry) obtained by HSPICE simulation.

E. Discussion

We make a comparison of MVL devices in Table I, mainly in terms of material systems, circuit implementation, and device characteristics. The original purpose of exploring new logic devices is to have the completeness of logic functions at the circuit level and the potential to build large-scale integrated circuits. In previous studies on MVL devices, only ternary logic devices based on the threshold adjustment principle have proposed a complete implementation scheme at both the logic gate level and the logic circuit level [41]. We have demonstrated the great potential of T-CSFETs as MVL devices in building large-scale logic circuits by circuit simulation and functional verification of a 2-bit adder, which have not been realized by other MVL devices. The T-CSFETs also demonstrate strong material compatibility, including 1D, 2D, and 3D materials. In terms of device characteristics, as shown in Table I, the T-CSFET is capable of achieving lower operating voltages. At the same time, there is a great potential to adjust the operating voltage through device design to obtain greater SNR. Furthermore, the T-CSFET can not only maintain a high on-state current but also ensure the intermediate state current at the subthreshold region (more than three orders of magnitude lower than the on-state current), which can further improve the advantages of T-CSFETs in power consumption as well as multivalue stability.

Compared with the mainstream binary logic, the size of the corresponding ternary combinational logic circuit increases because more information needs to be processed per bit. The circuit size increases linearly with the number of bits, but the amount of information that the circuit can process increases exponentially [35]. Furthermore, compared with a binary logic circuit, the capability of information transfer is more efficient in a ternary circuit with the same bits. Therefore, the number of information

TABLE I. Comparison of different ternary devices.

Type	Material	Number of transistors in STI/NTI/PTI	Demonstrated circuit	Operating voltage (V)	Out swing (%)	Current of state "1"[a]	On-state current	Year	Ref.
Cold source (this work)	CNT/CNR Graphene-MoS_2 (III-V)-Si	2/2/2	2-bit ternary adder	0.6	~100	$\sim 10^3$	10^2 μA/μm	2023	Simulation
Multithreshold	CNT	6/2/2	Ternary half adder	0.9	~98	N/A	N/A	2009	Simulation [7]
NDT	ReS_2-BP	1/(N/A)	Ternary inverter	4	~90	$\sim 10^{-2}$	10^{-4} A	2020	Expt. [38]
NDT	Organic semiconductor	2/(N/A)	Ternary inverter	50	~100	~0.8	10^{-6} A	2020	Expt. [3]
NDR	BP-ReS_2-HfS_2	N/A	SRAM cell	1.8	~50	~0.8	10^{-9} A	2020	Expt. [39]
Off-state constant I_D	Silicon	2/(N/A)	Two-stage cascaded inverter chain	1	~100	$\sim 10^{-3}$	10^{-1} μA/μm	2019	Expt. [40]
Quantized conducting states	ZnO composite	2/(N/A)	NMIN and NMAX logic	5	~95	$\sim 10^{-1}$	10^{-7} A	2019	Expt. [37]

[a]The magnitude of current in the intermediate state (state "1") is relative to the on current.
N/A stands for "not available".

accesses required to complete a computational task is significantly reduced, which in turn alleviates the storage wall problem in current von Neumann architecture computers.

It is also important to acknowledge that various scattering effects can potentially impede the performance of a practical device, including atomic defects [42,43] and electron-phonon scattering [44,45]. For T-CSFETs, it is crucial to achieve a current plateau in the subthreshold gate voltage region, which is determined by the band gap of the source material. The presence of atomic defects has the potential to induce gap states and narrow the band gap. Therefore, it is important to employ high-quality narrow-band-gap materials in the source, to prevent any compromise in the gate voltage region of the current plateau. Furthermore, the unavoidable electron-phonon scattering phenomenon can re-thermalize cold electrons in CSFETs [45], leading to a degradation in subthreshold swing. Even though sub-60-mV/decade switching is not a strict requirement for T-CSFETs, utilizing channel materials with low electron-phonon coupling can be beneficial for enhancing ternary properties.

IV. CONCLUSION

In summary, we propose a multivalue transistor based on the cold-source principle of source density of state modulation using a narrow-band-gap semiconductor. The ternary transfer current curves are obtained in T-CSFETs based on 1D, 2D, and 3D materials by using quantum transport simulations, with a current plateau region as an intermediate state between on and off states. It is shown that T-CSFETs based on a gapped graphene-MoS_2 heterojunction have well-distinguished ternary states with the current ratio between two sequential states of over 10^3. Promising on-state current of over 10^2 μA/μm is obtained at a bias voltage of 0.60 V. T-CSFETs are inherently advantageous for low-power applications because the supersteep effect of cold source is naturally incorporated. Our work provides an approach to realizing multivalue logic with abundant material systems, with great potential for the performance improvement of von Neumann architectures as well as energy and area efficiency.

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