

## Dual-sided charge-coupled devices

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Existing charge-coupled devices (CCDs) operate by detecting either the electrons or holes created in an ionization event. We propose an imager, the dual-sided CCD, which collects and measures both charge carriers on opposite sides of the device via a dual-buried channel architecture. We show that this dual detection strategy provides exceptional dark-count rejection and enhanced timing capabilities. These advancements have wide-ranging implications for dark-matter searches, near-infrared/optical spectroscopy, and time-domain x-ray astrophysics.

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## I. INTRODUCTION

Charge-coupled devices (CCDs) are broadly used as scientific instruments, offering unsurpassed imaging quality [1–4]. Existing CCDs collect and read only either the electrons or holes created in a bulk ionization event [4], while the charge carriers with opposite polarities are discarded. In this paper, we propose a device, the dual-sided CCD (DCCD), that enables both charge carriers to be measured, and we show that this detector has two advantages over standard single-polarity CCDs: improved rejection of dark counts (DCs) from various sources, including surface and spurious events, and enhanced timing capabilities. These advancements are critical for several scientific applications, including searches for dark matter [5–18], neutrinos [19–21], spectroscopy [22,23], and time-domain astrophysics [24–31].

In standard CCDs an event is detected by establishing an electrostatic potential that drifts the charge towards the “buried channel” [32], a potential extremum located close to one of the detector surfaces where the charge is stored away from gate insulating layers to avoid traps. The channel can be *p*-type, in which case it collects holes (*h*), or *n*-type, for electron (*e*) collection [4]. To collect *both* positive and negative charge carriers, a DCCD is equipped with channels of opposite polarities on the detector’s front and back, as illustrated in Fig. 1.

The advantages of such a design can now be made apparent. As shown in Fig. 1, bulk signal events populate both the front and back channels with opposite-polarity charges. Various DC sources, on the other hand, lead predominantly to *single-channel* events. Surface DCs, which are a leading background in state-of-the-art devices [4,7–9,14,33], occur thermally or from charge leakage in thin regions in between the buried channels and the surface detector gates where the traps from insulating layers are located [4,34–41]. Given the potential profile in these regions, such DCs only populate either the front or back-side channels with a hole or electron respectively, as any charge with the opposite polarity is drifted away towards the gates. Spurious or clock-induced charge generated during charge transfer, a dominant source of DCs in several devices [4,8,42–45], and all events that occur in the serial registers, transfer gates, or amplifiers, also lead to single-channel backgrounds. By discriminating such single-channel backgrounds from the dual-channel signals of bulk events, DCCDs can provide strong DC rejection.

Improved timing is also enabled by the readout of both charges. Standard CCDs have a time resolution that is typically limited by the time it takes to read out all the pixels of the array. In a DCCD this resolution can be significantly improved to be the time needed to read out a *single serial register* (a “row” of pixels). In megapixel devices this represents a three-order-of-magnitude improvement, and leads to time resolutions that can be as low as 10  $\mu$ s in EMCCDs [42] and 1 s in subelectron-noise Skipper-CCDs [8]. Enhanced timing is achieved by reading out the

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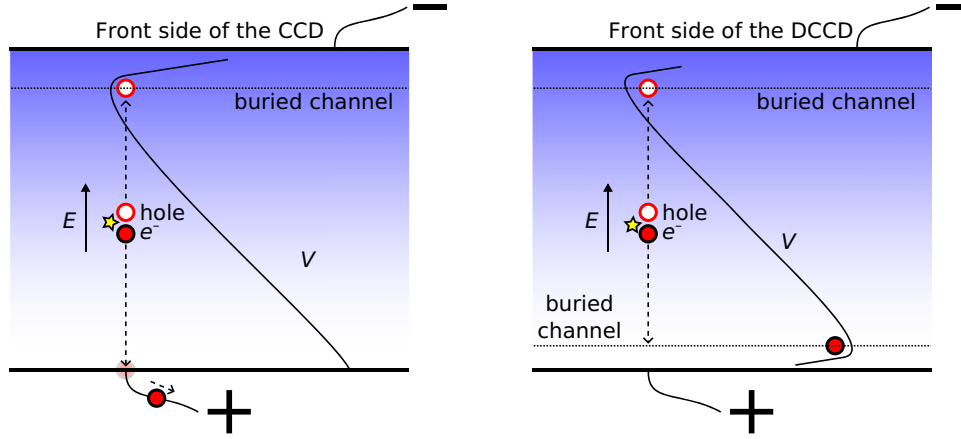


FIG. 1. Cross-section of a standard  $p$ -channel CCD collecting holes in its buried channel at the front of the sensor (left) and of a DCCD that collects holes at the front channel and electrons at the back channel (right).

device continuously and looking for correlations between the charges collected on the front and back channels. While these correlations can be obscured by event pileup, we show with simulations that this technique can be used in realistic applications.

We organize this paper as follows. We first discuss the basic design of a DCCD, device inversion, and present simulations demonstrating improved DC rejection and timing. We then discuss an example application of the DCCD as a dark-matter detector. We conclude by commenting on future directions. Natural units  $\hbar = c = 1$  are used throughout.

## II. DETECTOR ARCHITECTURE

### A. Dual buried channel

We design a DCCD starting from a standard three-phase [46], buried-channel [32], high-resistivity [47–49]  $p$ -channel [50–52] Si CCD [53]. In a  $p$ -channel CCD, a frontside buried channel to collect signal holes is formed with a gate insulator layer, placed on top of a layer of  $p$ -doped material, itself located atop the  $n$ -type (bulk) substrate. The channel  $p$ -doping density and the gate voltages are chosen so that for a depleted device, a potential minimum (the “buried channel”) is formed near the  $p$ - $n$  interface due to the interplay of the potential bias and opposing electric fields sourced by the negative ions in the  $p$ -Si, as seen in Fig. 1 (left). Signal holes are collected in this minimum.

To equip the device with a buried channel on the substrate’s backside, we add a backside gate, an insulator layer, and a layer of  $n$ -Si with a doping density and thickness commensurate with the frontside’s  $p$ -Si, as shown in Fig. 2. The addition of the  $n$ -Si on the backside allows for the formation of the backside buried channel; under

full depletion and for a negative front bias relative to the back gates, the positive ions of the  $n$ -Si induce an electric field that opposes that set by the bias, creating a potential *maximum* where signal *electrons* are collected, as in Fig. 1 (right). Intuitively, the addition of the backside’s  $n$ -Si mirrors the  $p$ -type structure on the front, but with an opposite polarity.

### B. Electrostatic potential profile

To demonstrate the formation of the buried channels, we examine the idealized situation where the dopant concentrations are spatially constant within each layer [54]. Figure 2 shows five material layers that from left to right correspond to: frontside oxide, frontside  $p$ -Si, bulk  $n$ -Si, backside  $n$ -Si, and backside oxide. We label these layers with the letters  $A$ ,  $B$ ,  $C$ ,  $D$ , and  $E$ , respectively, and solve for the electric fields across them. We work in a one-dimensional approximation along the depth of the DCCD. Using Gauss’s law and continuity of the normal component of the displacement field across dielectric interfaces, we obtain the electric fields as a function of the depth

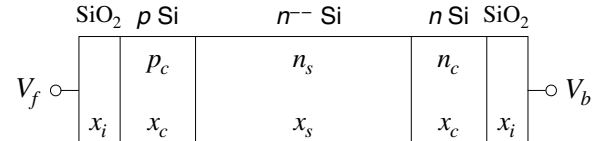


FIG. 2. Layers of a DCCD, from the front (left) to the back (right) of a pixel.  $V_f$  and  $V_b$  are front and backside gate voltages. The insulating layer, channel, and substrate widths are  $x_i$ ,  $x_c$ , and  $x_s$ . The  $p$ - and  $n$ -type doping concentrations of the channels and substrate are  $p_c$ ,  $n_c$ , and  $n_s$ .

coordinate  $x$  (with  $x = 0$  at the DCCD frontside):

$$\begin{aligned}
 E_A(x) &= E_{\text{SiO}_2}, \\
 E_B(x) &= \frac{\epsilon_{\text{SiO}_2}}{\epsilon_{\text{Si}}} E_{\text{SiO}_2} - \frac{qp_c(x - x_i)}{\epsilon_{\text{Si}}}, \\
 E_C(x) &= \frac{\epsilon_{\text{SiO}_2}}{\epsilon_{\text{Si}}} E_{\text{SiO}_2} - \frac{qp_c x_c}{\epsilon_{\text{Si}}} + \frac{qn_s}{\epsilon_{\text{Si}}}(x - x_c - x_i), \\
 E_D(x) &= \frac{\epsilon_{\text{SiO}_2}}{\epsilon_{\text{Si}}} E_{\text{SiO}_2} - \frac{qp_c x_c}{\epsilon_{\text{Si}}} + \frac{qn_s x_s}{\epsilon_{\text{Si}}} \\
 &\quad + \frac{qn_c}{\epsilon_{\text{Si}}}(x - x_c - x_s - x_i), \\
 E_E(x) &= \frac{\epsilon_{\text{Si}}}{\epsilon_{\text{SiO}_2}} E_D(x_i + 2x_c + x_s),
 \end{aligned} \tag{1}$$

where  $q = \sqrt{4\pi\alpha}$  is the electron charge ( $\alpha$  being the fine-structure constant). For the static dielectric constants we use the room-temperature values,  $\epsilon_{\text{Si}} = 11.6$  and  $\epsilon_{\text{SiO}_2} = 4.4$  [55].  $E_{\text{SiO}_2}$  is the (constant) electric field on the frontside oxide. These equations must be complemented with the bias voltage boundary condition [56]

$$\int_0^{2x_i+2x_c+x_s} dx E(x) = V_f - V_b, \tag{2}$$

which can be used to solve for  $E_{\text{SiO}_2}$ , resulting in

$$\begin{aligned}
 E_{\text{SiO}_2} &= -\frac{1}{2\epsilon_{\text{SiO}_2}(2x_i\epsilon_{\text{Si}} + (2x_c + x_s)\epsilon_{\text{SiO}_2})} \\
 &\quad \times [q\epsilon_{\text{SiO}_2}(n_c x_c^2 - 3p_c x_c^2 + 2n_s x_c x_s \\
 &\quad - 2p_c x_c x_s + n_s x_s^2) + q\epsilon_{\text{Si}}(2(n_c - p_c)x_c x_i \\
 &\quad + 2n_s x_s x_i) + 2\epsilon_{\text{Si}}\epsilon_{\text{SiO}_2}(V_b - V_f)].
 \end{aligned} \tag{3}$$

Using Eq. (3) in Eq. (1) gives the solutions for the electric field and the corresponding electrostatic potential across the DCCD.

With the above solutions we present the potential profile of a DCCD design example by taking a high-resistivity substrate with thickness  $200 \mu\text{m}$  and  $n$ -doping density  $n_s = 3 \times 10^{11} \text{ cm}^{-3}$  (resistivity  $\simeq 15 \text{ k}\Omega \text{ cm}$ ), channel with thickness  $x_c = 1 \mu\text{m}$  and dopings  $p_c = n_c = 10^{16} \text{ cm}^{-3}$ , and  $\text{SiO}_2$  insulators with thickness  $x_i = 50 \text{ nm}$ . The bias between the backside and frontside is taken to be  $V_b - V_f = 100 \text{ V}$ , while the reference frontside voltage is set to  $V_f = 0 \text{ V}$ . The resulting potential profile is shown in Fig. 3, where we see the emergence of a potential minimum and maximum on the front- and backside near the  $p - n^{--}$  and  $n^{--} - n$  junctions respectively, appropriately separated from the oxide interfaces. These distinct extrema correspond to the dual buried channels, which are the essential elements of our DCCD.

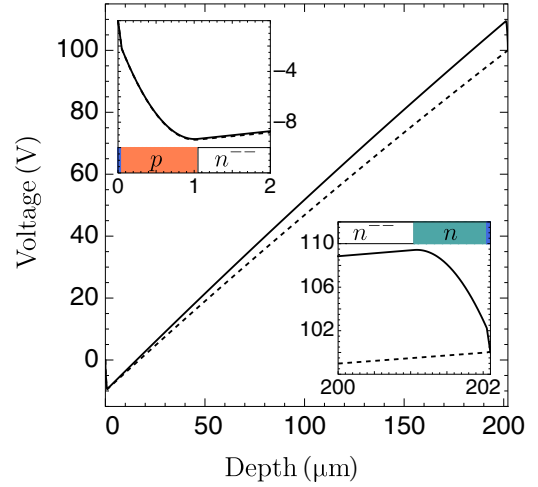


FIG. 3. Solid black: potential profile of a DCCD for  $n_s = 3 \times 10^{11} \text{ cm}^{-3}$ ,  $p_c = n_c = 10^{16} \text{ cm}^{-3}$ ,  $x_c = 1 \mu\text{m}$ ,  $x_i = 50 \text{ nm}$ ,  $V_b = 100 \text{ V}$  and  $V_f = 0 \text{ V}$  (cf. Figure 2). Front and back are located on the left and right of the plot. The upper-left and lower-right insets zoom in on the profiles around the potential extrema.  $p$ ,  $n^{--}$ ,  $n$  doped, and oxide regions are shown in orange, white, green, and blue. Dashed black: potential of a standard  $p$ -channel-only CCD obtained by removing the backside doping (setting  $n_c = n_s = 3 \times 10^{11} \text{ cm}^{-3}$ ) and oxide, shown for comparison.

Further insight into the solutions for the electrostatic potential can be obtained by taking advantage of the hierarchies between the substrate and channel or insulator thicknesses,  $x_c/x_s, x_i/x_s \ll 1$ , and between the substrate and channel doping concentrations  $n_s/n_c, n_s/p_c \ll 1$ , which allow us to find simple expressions for the channel locations and depths by expanding on these small ratios. First, we find that with the above hierarchies and at leading order in the expansion parameters, the front and back channels are located at the  $p - n^{--}$  and  $n^{--} - n$  junctions respectively, which is consistent with the results shown in Fig. 3, where we see that the potential extrema approximately align with the junctions. The depth of the potential of the front channel is given by the difference of the front gate voltage and the overall profile minimum  $V_{\min}$ , which at leading order is

$$V_f - V_{\min} \simeq qp_c \left( \frac{x_c^2}{2\epsilon_{\text{Si}}} + \frac{x_c x_i}{\epsilon_{\text{SiO}_2}} \right), \tag{4}$$

where  $\epsilon_{\text{Si}}, \epsilon_{\text{SiO}_2}$  are the permittivities of the substrate and oxide layers. The potential depth of the backside channel is similarly approximated by

$$V_{\max} - V_b \simeq qn_c \left( \frac{x_c^2}{2\epsilon_{\text{Si}}} + \frac{x_c x_i}{\epsilon_{\text{SiO}_2}} \right), \tag{5}$$

where  $V_{\max}$  is the maximum of the potential. Taking the design parameters of Fig. 3, these expressions lead to well

depths of about 10 V, approximately matching the results presented in the figure. Note that with the above approximations, both the physical position and potential depth of the channels are independent of the bias potential  $V_b - V_f$ , and are set instead by the channel widths, doping concentrations, and insulator properties as in a standard fully depleted single-sided CCD [49].

Note also that within the approximations, the depths of the front ( $p$ -type) and backside ( $n$ -type) wells in our DCCD are equal to the corresponding  $p$ - or  $n$ -type well depths of single-sided CCDs sharing the same  $p$ - or  $n$ -type channel design parameters. This can be seen by noting that the DCCD's front and backside well depths [Eqs. (4) and (5)] are independent of  $n_c$  and  $p_c$ , respectively. As an example, taking  $n_c \rightarrow n_s$ , our device reduces to a single-sided  $p$ -type CCD with a well depth that matches the frontside well depth of a DCCD that instead has  $n_c \gg n_s$ . This can also be seen in Fig. 3 by comparing the well depths of the solid (DCCD) and dashed-black (single-sided  $p$ -type CCD) lines.

For thin devices where substrate widths are of the order of  $\mathcal{O}(10)$   $\mu\text{m}$  the approximations (4)–(5) are numerically inexact, but we have checked using the exact electrostatic solutions [Eqs. (1)–(3)] that for such devices dual wells can still be easily designed with typical channel doping densities.

### C. Inversion

As in a standard CCD, the DCCD can be inverted to reduce surface DCs [35,57] by populating the Si-oxide interfaces with minority carriers. We envision that the minority carriers on the interface between the oxide and  $n$ -Si on the backside could be provided by  $p$ -type channel stops, or if these are depleted, by other  $p$ -Si contacts. Similarly, the minority carriers at the oxide and  $p$ -Si interface on the frontside could stem from the  $n$ -type front channel stops or contacts.

We illustrate the steps leading to inversion by considering a DCCD with design parameters as in the previous section, namely  $x_i = 50$  nm,  $x_c = 1$   $\mu\text{m}$ ,  $x_s = 200$   $\mu\text{m}$ ,  $n_c = p_c = 10^{16}$   $\text{cm}^{-3}$ , and  $n_s = 3 \times 10^{11}$   $\text{cm}^{-3}$ . We assume that the minority carriers from the channel stops or extra contacts are kept at 0 V. Starting from normal biasing conditions, as in Fig. 3 ( $V_f = 0$  V,  $V_b = 100$  V), we begin by decreasing the backside voltage down to negative values. We find from our electrostatic solutions [Eqs. (1)–(3)] that at  $V_b = -2.3$  V the potential at the  $n$ -Si/oxide interface is reduced to 0 V, as shown in Fig. 4. At this point holes from the channel stops or contacts flow into the interface with the oxide, pinning the potential at that value. As in a standard CCD in inversion, further reductions of the backside gate potential are screened by the interface charges so that the bulk potential remains unaffected, as represented by the dashed black lines in the figure, and the

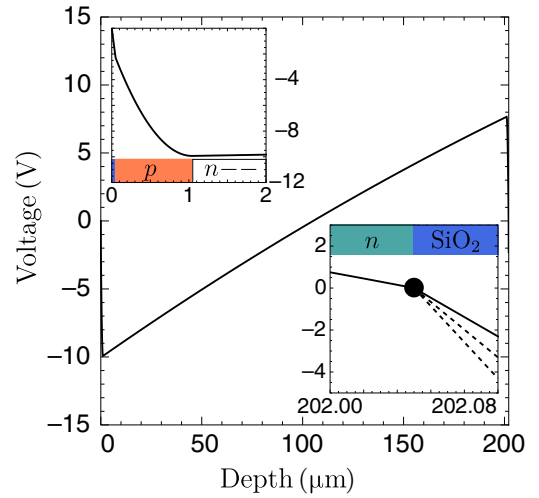


FIG. 4. Potential profile of a DCCD (with a geometry and material coloring as in Fig. 3) with a frontside gate potential equal to 0 V and a backside gate potential that has been reduced to invert the backside channel. The upper-left inset zooms into the front channel potential, which is noninverted, while the lower-right inset zooms into the  $n$ -Si/oxide interface at the inverted back channel. At that interface, the potential is pinned at 0 V, as shown by the black circle.

reductions are compensated by an increase in the magnitude of the oxide electric field. This leads to inversion of the backside channel.

At this point the frontside channel can be inverted by raising the frontside gate potential. To calculate the point of inversion, we solve the first four electrostatic equations in Eq. (1), which describe the electric field up to the interface with the backside oxide, subject to the boundary condition that the potential at the backside  $n$ -Si/oxide interface is pinned to 0 V,

$$\int_0^{x_f + 2x_c + x_s} dx E(x) = V_f - 0. \quad (6)$$

By solving these equations, we find that at  $V_f = 2.3$  V, the potential at the frontside  $p$ -Si/oxide interface reaches 0 V. Here the  $n$ -type minority carriers flow into the interface and screen further reductions in the frontside potential, as shown in Fig. 5. Note that the front and backside gate potentials required for front and back inversion are equal in magnitude but opposite in sign,  $V_f = -V_b = 2.3$  V, as expected from our symmetric design.

A DCCD offers the possibility of inverting both front and back channels, only the front channel, or only the back channel. This versatile operational capability could be valuable for the characterization of surface dark currents in CCDs.

Current CCDs with record low DCs are operated by first driving the device into inversion to fill interface traps [8,58]. The device is then driven back to the noninverted

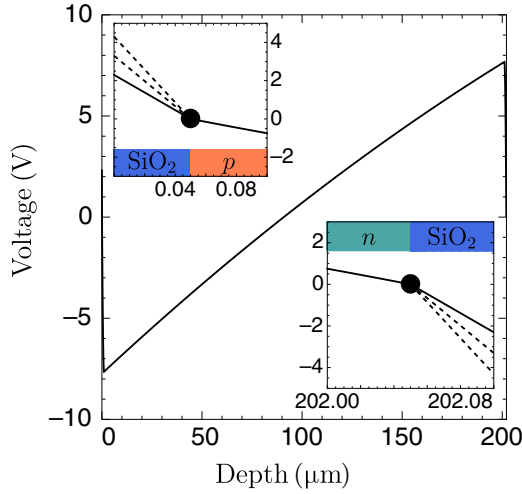


FIG. 5. Potential profile of a DCCD (with a geometry as in Fig. 3) with front and backside gate potentials that have been respectively raised and lowered to invert both front and back channels. The insets at the upper-left and lower-right zoom into the doped-Si/oxide interfaces at both inverted channels, where the potentials are pinned at 0 V as shown by the black circles.

state to benefit from the efficient channel charge transfer and reduced lateral charge diffusion in this mode [4,49]. Data is taken in noninverted mode, but while interface traps are still filled. This procedure allows one to exploit the main advantages of both inverted and noninverted operation, and is critical to reduce DCs and, for example, increase the sensitivity of the device for dark-matter detection. We envision that under normal operating conditions a DCCD would function in an analogous way: first the DCCD would be driven to dual-channel inversion to fill front and backside interface traps; and then data would be taken in noninverted mode to facilitate charge transfer in both channels and to reduce charge diffusion.

#### D. Readout

Charge stored in the channels is read out as in a standard CCD [4], so we comment only briefly on the additional design features that enable dual-charge readout. In a DCCD there are both front and backside gates with synchronized clocked voltages that move the charges along front and back vertical (“parallel”) registers (VR) into two distinct serial registers (SR), one designed to read holes at the front, and the other dedicated to electrons at the back. Charge is confined within the VR by separate sets of channel stops at the front and back. A schematic design of the device is shown in Fig. 6(left). In the DCCD, electrons and holes are shifted in *opposite directions* along the VR; this feature enables enhanced timing as discussed below. With this scheme, the order in which charges are read is illustrated in Fig. 6 (right). Additional schematics

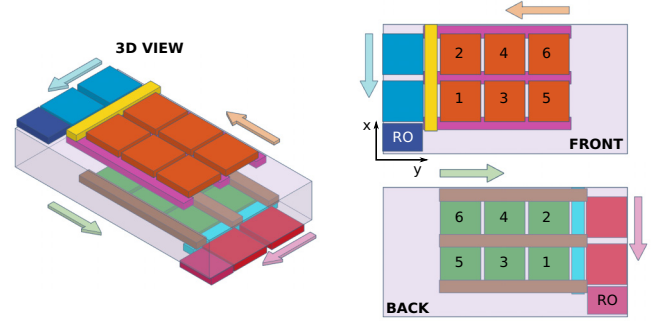


FIG. 6. View of a  $3 \times 2$  pixel DCCD. Front and backside pixels are shown in dark orange and green, channel stops appear in magenta and brown, and gates are shown in blue and red, respectively. Arrows indicate the direction of charge transfer towards readout. The numbers indicate the pixel readout order on each side. The  $x$  is the coordinate along both serial registers, and  $y$  along the vertical register of the front CCD. RO stands for readout.

are presented in Figs. 7 and 8, where we show transverse views along the different cross-sectional directions of the device and a three-dimensional representation of the device, respectively.

### III. DEVICE CAPABILITIES

The DCCD can be operated in timed exposure or continuous readout mode, with each mode presenting advantages that can be selected based on the specific application.

#### A. Timed exposure mode: DC rejection and other capabilities

DCCDs distinguish surface or spurious charge backgrounds from bulk signals by discriminating single versus dual-channel events. Such backgrounds are thus reduced to the rare cases where front and back DCs coincide at the same sensor location within the exposure time.

The single-channel DC rejection factor can be computed analytically under the large-CCD approximation (negligible edge effects) and for low occupancy (negligible DC overlap). Given a single-hole event in the front face, a coincident event is obtained if a corresponding single-electron event is registered in the back [59]. This occurs with a probability  $P_{n=1} = \lambda \exp(-\lambda)$ . The noncoincidence probability is then given by

$$P_{\text{noncoincidence}} = (1 - P_{n=1})^{n_{\text{pix}}} = [1 - \lambda \exp(-\lambda)]^{n_{\text{pix}}} \approx 1 - n_{\text{pix}}\lambda, \quad (7)$$

where  $\lambda$  is the expected number of single-channel DCs per pixel per exposure time,  $n_{\text{pix}}$  is the number of pixels around the frontside event that will be considered as a possible match in the backside, and the approximation is valid in the low-DC limit where  $n_{\text{pix}}\lambda \ll 1$ . The parameter



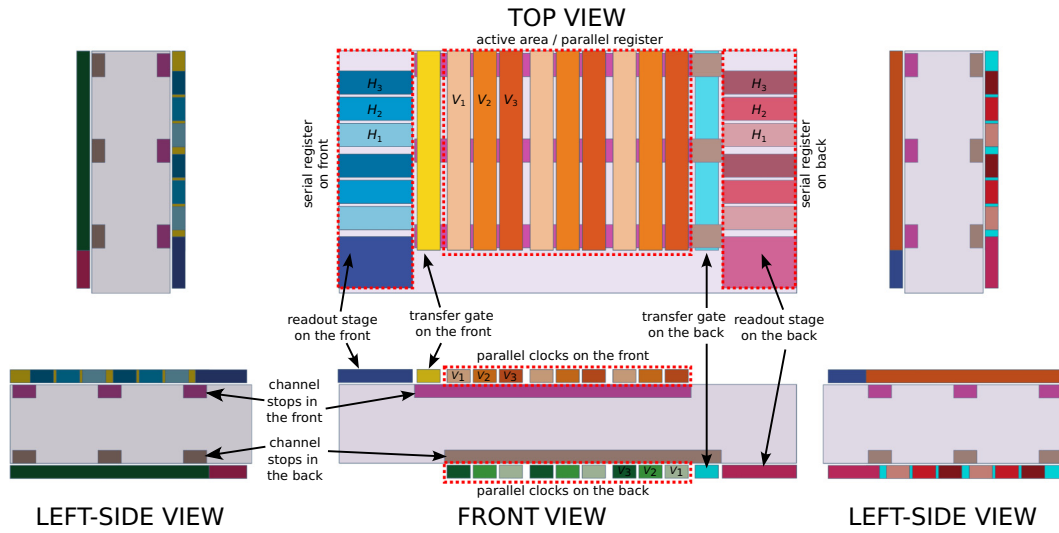


FIG. 7. Schematic view of a  $3 \times 2$  pixel DCCD with three-phase CCDs on each side. The parallel clocks on the front are shown in shades of orange and the ones in the back are in shades of green (as in all the other pictures in this paper). The three-phase gate voltages facilitating charge transfer down the vertical registers are labeled  $V_i$ ,  $i = 1, 2, 3$ , while the three-phase voltages used to transfer charge along the SR are labeled  $H_i$ ,  $i = 1, 2, 3$ .

$n_{\text{pix}}$  is introduced to account for the possibility that carriers created in a bulk event can move to adjacent pixels. The matching technique for these true events has to account for diffusion by enlarging the search “radius”  $r$  around the

collected carriers to find their complement on the other channel. The diffusion radius  $r$  defines a square centered on the event’s frontside pixel location, with side-length equal to  $2r + 1$ . For thin sensors diffusion is negligible and  $r = 0$ ,

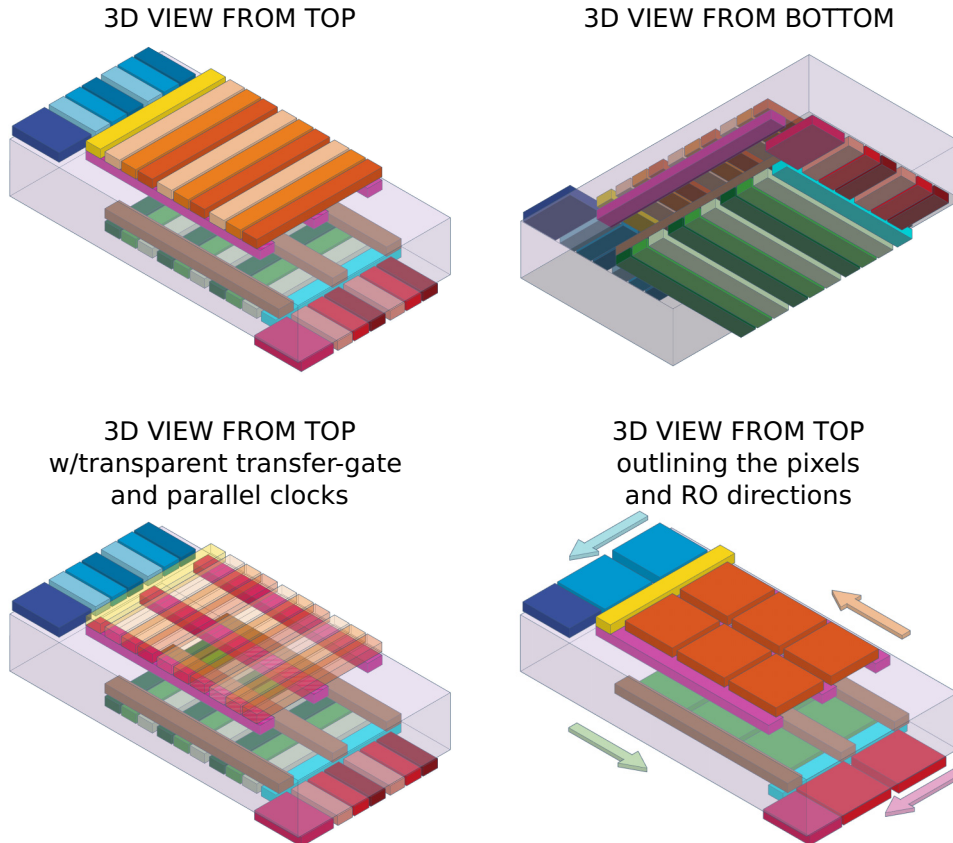


FIG. 8. Top two images: schematic 3D view of a  $3 \times 2$  pixel DCCD with three-phase CCDs on each side. Bottom left: same as top-left but with transparent front transfer gate and parallel clocks to show internal structure. Bottom right: schematic view with the pixels outlined. Arrows indicate the direction of charge transfer leading to readout. RO stands for readout.

but thick sensors can be several hundreds of micrometers across in which case diffusion can lead to inter-pixel migration. Following the results of [8], for sensors thicker than  $\approx 600 \mu\text{m}$ ,  $r = 2$  should typically be used. For timed exposure (TE) operation the range of values that  $n_{\text{pix}}$  is thus given by

$$n_{\text{pix}}^{\text{TE}} = \begin{cases} 1, & \text{no diffusion (thin sensor) } r = 0, \\ 9, & \text{1-pixel diffusion radius } r = 1, \\ 25, & \text{2-pixel diffusion radius } r = 2. \end{cases} \quad (8)$$

The coincidence probability sets the DC rejection factor, and is given by

$$\begin{aligned} P_{\text{coincidence}} &= 1 - P_{\text{noncoincidence}} \\ &= 1 - [1 - \lambda \exp(-\lambda)]^{n_{\text{pix}}} \approx n_{\text{pix}} \lambda, \end{aligned} \quad (9)$$

where again the approximation is valid for  $n_{\text{pix}} \lambda \ll 1$ .

To confirm our analytic results with a more realistic calculation that accounts for edge effects and DC overlaps, we perform single- $e/h$  DC Monte Carlo simulations on a  $1000 \times 1000$  pixel DCCD. The results are shown in Fig. 9, where we see the rate of dual-channel DCs from the coincidences of single-channel events as a function of their per-pixel rate within an exposure time  $\lambda$ , assumed to be the same on both sensor sides. The dual-channel rates are shown for different assumptions regarding the diffusion of bulk  $es$  and  $hs$ , that is, for different search radii  $r$ . The rates shown in the figure are thus the coincidences that occur within the search radius for each assumption. For each simulated point, the ratio between the horizontal and vertical coordinates represents the DCCD's single-channel DC rejection factor.

As expected, we find that the dual-channel rate for all diffusion scenarios is significantly lower than the single-channel rate, with a larger reduction for lower single-channel DCs, since this leads to a lower probability of coincidental occurrences. In the absence of diffusion the dual-channel rate is simply the per-pixel single-channel rate squared, as expected from coincidences within a pixel. When diffusion is added, the dual-channel DCs increase, since the allowed area for coincidences is larger, but we still find strong DC rejection. In all cases, we find that the coincidence DC rates obtained from the Monte Carlo analysis are accurately described by the analytic estimate in Eq. (9). Note that dual-channel surface DCs grow *quadratically* with exposure time, as longer exposures increase the coincidence probabilities. For DCs of the order of  $\lambda = 10^{-4}$  per pixel per day and day-long exposures as in [8], our results show that a DCCD could lead to a three-order-of-magnitude reduction of single-channel DCs.

Besides DC rejection, the DCCD can distinguish bulk events that occur during readout from those that occur

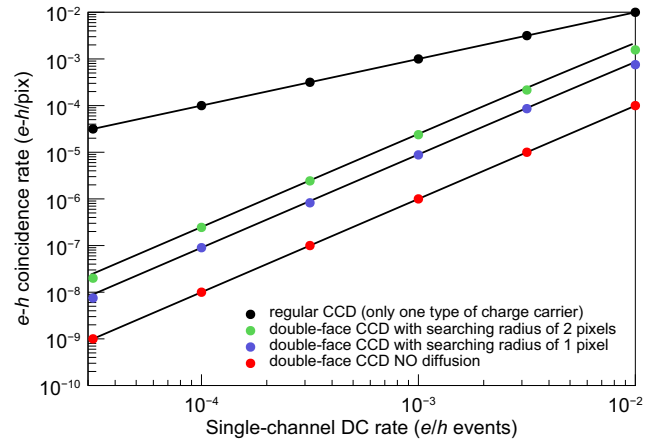


FIG. 9. Rate of coincident  $e-h$  events versus the per-pixel single-channel DC rate within an exposure time ( $\lambda$  in the text), assumed to be the same on both detector sides. Colored circles show the rates for different assumptions regarding bulk carrier diffusion; red corresponds to a search radius  $r = 0$ , blue is  $r = 1$ , and green is  $r = 2$  pixels. Black circles show the DC rates for a standard CCD. The plotted range of single-channel DCs represents realistic rates for day-long exposures [8]. The solid black lines are analytic calculations assuming an infinite CCD [Eq. (9)]. Note that in a DCCD the DC rates depend *quadratically* on the single-channel DC rate, since DCs are obtained only when front and back DCs coincide in the same sensor location.

during the exposure, as the former are registered as electrons or holes without a counterpart of opposite polarity within the same pixel. Charge-transfer inefficiencies are also single-channel issues, and can be mitigated using our dual-imaging strategy.

## B. Continuous readout mode: timing and DC rejection

When standard CCDs are read out continuously an ambiguity between the location of the interaction on the VR and its time arises, as events that occur on a pixel at a given time can be mimicked by events that occurred earlier upstream in the VR, leading to a loss of vertical localization [6,60]. DCCDs overcome this limitation by reading the front and back active areas in opposite directions. This allows one to disambiguate the absolute position of the primary interaction by looking for correlations in the recorded charge packages (up to event pileup, discussed below), as shown in Fig. 10.

For an event occurring at an absolute coordinate  $y$  in the CCD parallel direction (distance  $y$  in pixels between the VR pixel location and the frontside SR) and time  $t$  from the start of the readout, the times of arrival  $t_f$  ( $t_b$ ) of the corresponding holes (electrons) at the front (back) SR are given by

$$\begin{aligned} t_f &= y + t, \\ t_b &= L_{\text{VR}} - y + t, \end{aligned} \quad (10)$$

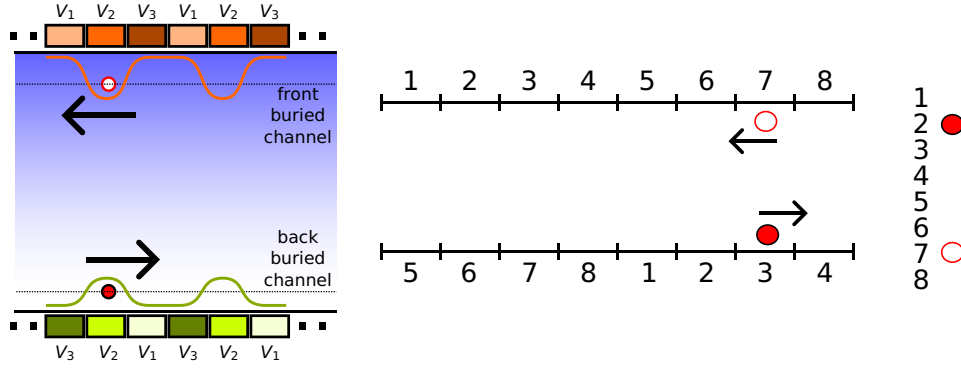


FIG. 10. Left: cross section of a DCCD, with electrons and holes, in the front and back VRs respectively, being moved in opposite directions towards readout.  $V_i$ ,  $i = 1, 2, 3$  are the three-phase voltages of a pixel. Right: in continuous readout, one can determine the event vertical-register position by matching the back and front charges. There is only one position that produces the recorded values (2 and 7 in this example).

where  $L_{VR}$  is the physical number of pixels of the CCD in the vertical or parallel direction (the number of pixels in the VR) and times are measured in integer numbers of VR pixel shifts required to place charges in the SR. As charges stay on a VR pixel for the time it takes to read out the SR,  $T_{SR}$ , times are thus quantified in units of  $T_{SR}$ . Given the measured  $t_f$  and  $t_b$ , from these equations we can reconstruct the event's position as

$$y = \frac{1}{2}(t_f - t_b + L_{VR}). \quad (11)$$

Furthermore, from the event's position and the time of arrival at the SR the event's timestamp is determined by

$$t = t_f - y = \frac{1}{2}(t_f + t_b - L_{VR}), \quad (12)$$

with a time resolution  $T_{SR}$  [61]. Thus, while an event's timing in a standard CCD is given by the time it takes to read the whole VR,  $T_{CCD}$ , in our DCCD this is *significantly improved* as  $T_{SR} \approx T_{CCD}/L_{VR} \ll T_{CCD}$ , especially in large devices where  $L_{VR} \gg 1$ . In megapixel arrays  $L_{VR} \simeq 10^3$ , and this represents a three-order-of-magnitude improvement with respect to conventional devices.

Correlations between electron and holes, however, are only unique up to event pileup. Pileup occurs when the time difference between the events matches the time it takes to move their charges between their VR locations, in which case their charge packets are summed. Either the  $h$  or  $e$  packets of different events can be summed, leading to overlapping events in the front- or backside images, respectively. This issue can be mitigated by correlating the front- and backside images [62]. A second type of pileup arises when events with the same number of  $es$  or  $hs$  occur in a VR within  $T_{CCD}$ , in which case multiple pairings between the  $e$  and  $h$  packets may be possible and the

event's location and time are lost in pairing ambiguities (but it is still possible to veto such events). Optical/near-infrared photons always lead to single  $e$ - $h$  pairs, so pairing ambiguities often arise if another such photon or DC falls in a given VR within  $T_{CCD}$ . X-ray events, on the other hand, rarely lead to the same number of  $e$ - $h$  pairs and are thus less prone to pairing ambiguities.

The above considerations indicate that our DCCD's timing is most effectively utilized in situations with low illuminations, where pileup is limited. To exemplify a concrete application, we present in Fig. 11 a GEANT4 [63] simulation in a  $70 \times 60$  pixel DCCD of three energetic events, one being spot-shaped, and two being tracklike, with the shortest one leading to isolated single  $e$ - $h$  events by, for example, secondary luminescence [14]. Given  $L_{VR} = 70$ , for the lower-left end of the shorter track we register  $t_f = 25$  and  $t_b = 45$ , which, using Eqs. (11) and (12), results in  $y = 25$  pixels and  $t = 0$  in units of  $T_{SR}$ . Similar arguments indicate that the secondary photons happened concurrently, from which they can be associated to the track, while the spot-shaped x ray and the longer track occurred at  $t = 20 T_{SR}$  and  $t = 60 T_{SR}$ , respectively. The spotlike event in the image recorded by the front CCD would be considered as part of the halo of the high-energy event in a standard device, but the timing provided by the DCCD allows it to be separated.

In continuous readout, single-channel DCs can mimic signal events when front and back DCs coincide within  $T_{CCD}$  in a given VR. Since these coincidences are more likely than the per-pixel or search radius ones leading to DCs in timed exposure operation (and given that continuous readout results in increased spurious charge [6,8]), in this mode the DC rejection capabilities are partially reduced when compared to timed exposure operation. In other words, the number of pixels  $n_{pix}$  that need to be considered for a front-back single-channel DC match [cf.



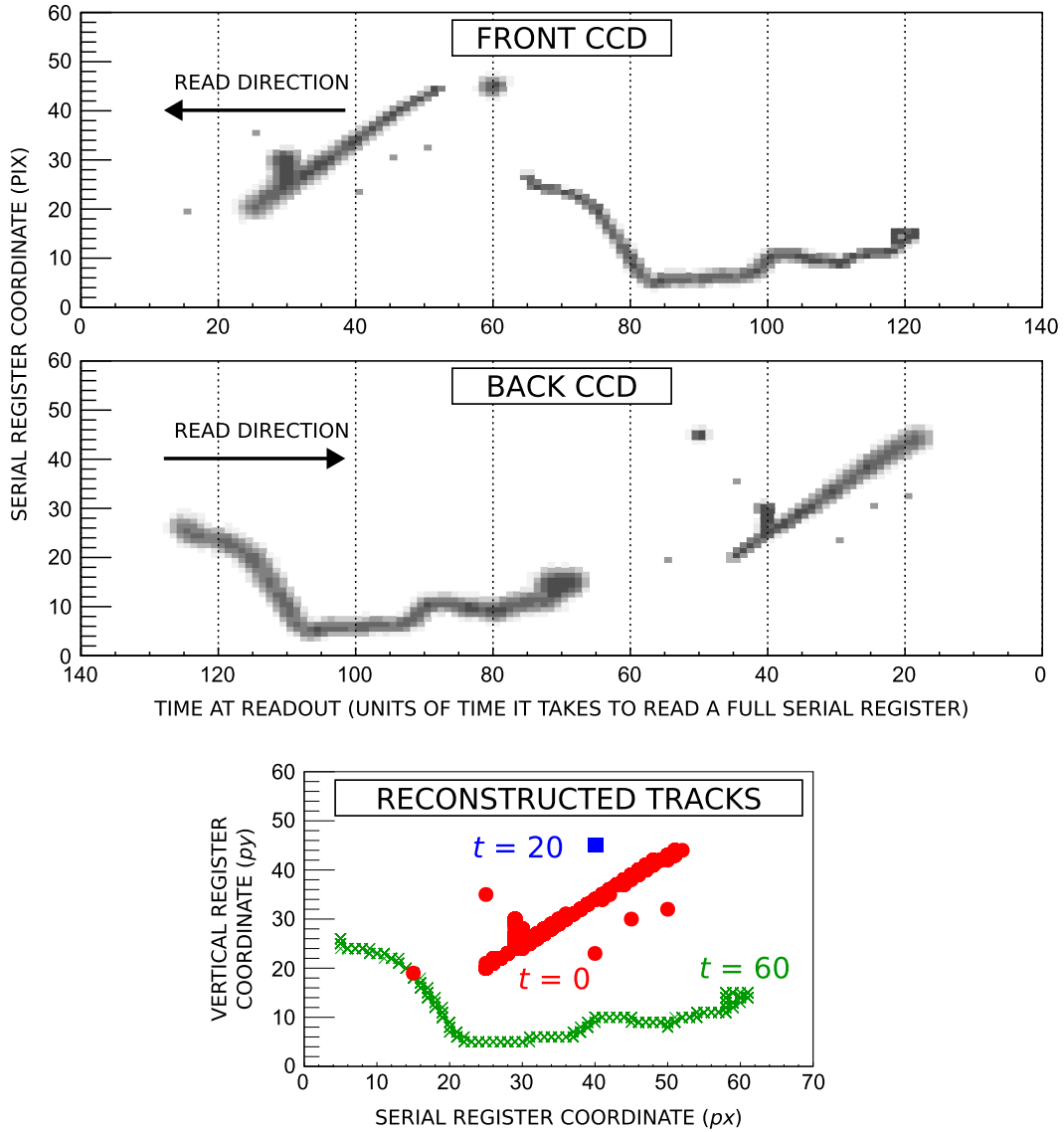


FIG. 11. Simulated events as seen by the front (top) and back (middle) readout stages of a DCCD. Serial and vertical registers are along the vertical and horizontal directions, respectively. Note that the diffusion of the charge carriers is mirrored. The lower panel shows the reconstructed image. The colors indicate the time of arrival in units of  $T_{SR}$ .  $px$  and  $py$  stand for pixel coordinate in the horizontal and vertical directions.

Eq. (9)] is *larger* in continuous readout mode than in timed exposure operation, and this results in a larger coincidence DC rate. Accounting for the coincidences within a whole VR, in continuous readout (CR) we have

$$n_{\text{pix}}^{\text{CR}} = \begin{cases} L_{\text{VR}}, & \text{no diffusion (thin sensor) } r = 0, \\ 3L_{\text{VR}}, & \text{1-pixel diffusion radius } r = 1, \\ 5L_{\text{VR}}, & \text{2-pixel diffusion radius } r = 2, \end{cases} \quad (13)$$

where  $L_{\text{VR}}$  is the VR length in pixels. Using Eqs. (8) and (13) in Eq. (9), we see that in the low-DC limit  $n_{\text{pix}}\lambda \ll 1$ , single-channel DC rejection in timed exposure mode is stronger than in continuous readout by a factor of  $L_{\text{VR}}$

(about  $10^3$  in megapixel arrays). Nonetheless, sizable DC rejection capabilities can still be achieved in continuous readout operation; for typical values  $\lambda = 10^{-4}$  per pixel per day with day-long exposures and  $L_{\text{VR}} \sim 10^3$  as in [8], one-order-of-magnitude single-channel DC suppression can be achieved in thin sensors under continuous readout.

#### IV. DARK-MATTER REACH

In this section, we compare the anticipated dark-matter (DM) detection capabilities of forthcoming large-exposure Skipper-CCD-based experiments, like [64], with those of

equivalent experiments that use instead dual-sided Skipper CCDs (Skipper DCCDs). To perform projections we follow the procedure in [33], briefly summarized here as follows. We consider experiments looking for DM scattering on electrons by measuring ionization signals in CCD pixels. We focus on models where DM scatters with electrons via a light mediator, that is, models with a scattering form factor  $F_{\text{DM}}(q) = 1/q^2$  where  $q$  is the momentum transfer [65]. We parametrize the strength of the scattering rate by the cross section on electrons  $\bar{\sigma}_e$  at a fixed momentum transfer  $q = \alpha m_e$ , where  $\alpha$  is the fine-structure constant and  $m_e$  the electron mass [65]. For a given  $\bar{\sigma}_e$  and DM mass, we compute the number of ionized electron-hole pairs in Si using QCDark [66]. Based on the number of ionized electron-hole pairs for a DM signal event within pixels of the CCDs, we divide the search into one- to four-electron bins; the precise definition of each signal bin and the corresponding analysis cuts follows closely the strategy used by the SENSEI experiment at the MINOS cavern [8].

We project limits when the rate of DM ionization events for any of the electronic bins exceeds the rate expected in the background-only hypothesis, accounting for statistical uncertainties at a 95% confidence level. The background hypothesis is obtained from the assessment of dark counts in Skipper CCD-based DM experiments presented in [33], and is summarized as follows. For the one-electron bin, following the analysis in [8] we drop backgrounds coming from spurious charge, as these are measured and removed from the analysis. Consistent with the measured data in [8] and the simulations performed in [33], we assume that the remaining one-electron rate has two components. First, it has a component due to low-energy Cherenkov photons with a rate  $R_{1e} = 185 \text{ g}^{-1} \text{ d}^{-1}$ . We assume that forthcoming detectors will be able to remove radiative backgrounds with improved radiopurity and shielding (see, for example, [64]), so we simply neglect this component. The second component is nonradiative in origin, is homogeneous across the whole CCD, and has magnitude  $R_{1e} = 300 \text{ g}^{-1} \text{ d}^{-1}$ . While its origin is unknown, as argued in [33] and in this paper, it is likely associated with detector DCs that occur on surfaces. Since DCs of this type can be mitigated by the dual-readout strategy proposed in this paper, we assume that this background component is suppressed in DCCDs by a factor of  $10^3$  with respect to its rate in standard (single-sided) Skipper CCDs, consistent with the estimates presented in Fig. 9. We acknowledge, however, that assuming that all DCs arise on the surface is a favorable assumption for our device, as it maximizes its DC rejection capabilities.

For the higher-electron bins, following the results in [33] we assume that the 2-, 3- and 4- electron background rates are dominated by coincidences of the aforementioned surface one-electron background events and spurious charge. As in the analysis of [8], we do not perform

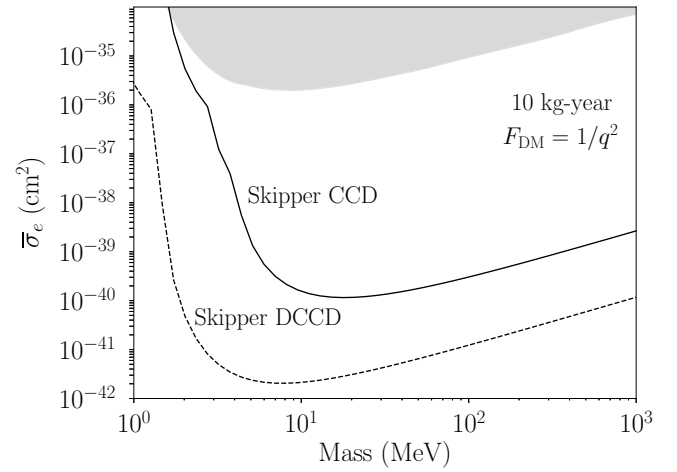


FIG. 12. Projected exclusion regions at 95% confidence for a light-mediator DM model (scattering form factor  $F_{\text{DM}} = 1/q^2$ ) for an experiment using standard single-sided Skipper CCDs (solid black) and the Skipper DCCDs proposed in this paper (dashed black). The detector exposure is taken to be 10 kilogram-years, and backgrounds are accounted for as described in the body of the text. Gray shaded regions are already excluded by existing direct-detection experiments, with leading constraints coming from the Skipper CCD-based experiments [8,13,67,68].

any background subtraction for these bins. This amounts to taking  $R_{2e} = 0.51 \text{ g}^{-1} \text{ d}^{-1}$ ,  $R_{3e} = 0.035 \text{ g}^{-1} \text{ d}^{-1}$ , and  $R_{4e} = 4.22 \times 10^{-6} \text{ g}^{-1} \text{ d}^{-1}$  in single-sided Skipper CCDs, correspondingly [33]. Since the one-electron dark count rate is dominated by surface events, and since spurious charge is associated with clock-voltage swings that also occur near detector surfaces [4], under our assumptions all multielectron events stem from coincidences of one-electron single-channel events. As a consequence, the DCCD is effective at suppressing multielectron backgrounds, and the  $10^3$  reduction of the single-electron backgrounds considered above translates into a  $10^{3n}$  reduction in the backgrounds for the  $n$ -electron bins,  $n = 2, 3, 4$ , with respect to the rates in single-sided Skipper CCDs.

We perform projections assuming an exposure of 10 kilogram-years, which is the order-of-magnitude target exposure of future Skipper CCD-based detectors [64]. Our results are presented in Fig. 12. The figure shows that experiments using Skipper DCCDs have the potential to deliver significant improvements in the reach to detect DM with respect to those based on standard single-sided Skipper CCDs, due to the DCCD's enhanced background mitigation capabilities. The most significant improvements are achieved for lower DM masses, as in these models the search is dominated by the low-energy bins that have comparatively larger backgrounds than the higher-electron bins. Quantitatively, we find that Skipper DCCDs could outperform the reach of standard Skipper CCDs by factors

of approximately  $10^3$ , 80, and 20 for DM masses of 1, 10, and 100 MeV, respectively.

## V. DISCUSSION

We have presented the basic design and capabilities of the dual-sided CCD (DCCD), a device that collects both the electrons and holes created in an ionization event to deliver improvements in DC rejection and timing with respect to standard CCDs. By performing simulations of realistic applications, we showed that a DCCD is able to typically provide three-order-of-magnitude improvements in DCs and timing with respect to existing megapixel devices.

This paper begins the study of dual-sided imagers, and opens up significant opportunities for research. First, the advancements brought by DCCDs have far-reaching implications for particle physics and astrophysics (see Introduction). Second, the DCCD architecture can be integrated with several existing CCD designs, further enhancing its relevance. A DCCD can be fabricated on thick, high-resistivity Si to improve the red response [48,49,69]. A Skipper DCCD can be designed to reduce readout noise [5,70–72]. A dual-sided electron-multiplying CCD (EMCCD) [42] could be fabricated to achieve submillisecond timing and would drastically reduce spurious charge [43–45]. Given the similarities between CCDs and CMOS imagers, several of the design features discussed here may also be applied in the context of CMOS detectors to reduce surface DCs [73]. Finally, this work motivates efforts to begin the fabrication of a DCCD, which can be manufactured based on existing and demonstrated designs for standard CCDs [64] by replicating these layouts on both sides of a Si wafer. A preliminary assessment of the fabrication timeline indicates that, subject to funding, a first working prototype could be available within 3 years.

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