Exploring the border traps near the valence band in the SiO_2-SiC system using above-band-gap optical excitation

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Studying near-valence-band (E_V) defects at the insulator–*n*-type 4*H*-SiC interface is challenging due to the low minority carrier concentration. Herein, we present a technique for characterizing the border traps near E_V in an *n*-type 4*H*-SiC MOS capacitor by generating holes using above-band-gap optical excitation (OE). A rise in capacitance was observed under OE (due to hole capture by border traps), remaining stable long after the optical stimulus was removed, resulting in a persistent photocapacitance effect. We show the dynamics of the capture process and perform a quantification of the captured holes in samples with thermally grown oxide and different postoxidation annealing treatments.

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I. INTRODUCTION

4*H*-SiC is one of the most important semiconductors in the field of power electronics. Due to the large band gap, high thermal conductivity, and high critical electric field, devices fabricated using SiC can be used for high-voltage or -current applications [1]. The distinct advantage of using SiC over other wide-band-gap semiconductors is the possibility to thermally grow the native oxide, SiO_2, similar to the case for silicon (Si). Studies of Si over the last four decades have resulted in optimized fabrication facilities and very precise processing steps for SiO_2 growth. Since Si and SiC share the same native oxide, the fabrication of SiC-based devices can be carried out at existing Si fabrication facilities with minor modifications [2]. Although the properties of the SiO_2-SiC interface with deposited oxide [3] have been studied extensively, a thermally grown oxide usually has lower porosity and higher critical field strength in comparison to the deposited oxide, which results in reduced gate-leakage current [4]. However, along with the many benefits that come with the thermal oxidation of SiC, there are some disadvantages as well. The SiO_2-SiC interface suffers from a high density of interface traps (D_{IT}), which is almost 2 orders of magnitude higher than the state-of-the-art SiO_2-Si interface [5]. This leads to reduced effective mobilities due to charge trapping [6]. In addition, thermal oxidation also results in a high density of traps in the oxide itself, which can lead to severe threshold-voltage variation and bias-temperature instabilities [7,8]. The impact of these so-called *border traps* [9–11] in SiO_2 is conventionally studied by applying gate stress (measure-stress-measure procedure [12]) for varying duration and performing a measurement of the shift of the threshold voltage [7].

Several other techniques have been used to study these border traps. For instance, in Refs. [13–15], conductance measurements were carried out on MOS capacitors as a function of frequency and temperature, whereas, in Ref. [16], emission from traps near the interface was observed under a pump-probe scheme, highlighting their energetic position in the band gap. In Ref. [17], the authors characterized the near-interface oxide traps at the conduction-band edge using the integrated charge method, which highlights the degrading behavior of these traps on the performance of SiC power MOSFETs. In most of these studies, the border traps near the conduction-band edge are studied; these usually capture electrons and lead to positive bias-temperature instability in a SiC MOSFET. On the other hand, the capture of holes in the border traps near the valence-band edge would lead to negative bias-temperature instability (NBTI). This can be facilitated by a negative gate bias, which is usually applied to prevent parasitic turn ON of a MOSFET [18] during application. However, studying the defects near the valence-band edge, which are likely to capture holes in a MOSFET and lead

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to NBTI, is challenging in an *n*-MOS device due to the absence of minority carriers. Therefore, in this work, we use above-band-gap optical excitation to generate minority carriers (holes) in the semiconductor that can tunnel across the SiO_2-SiC interface into the oxide and are captured by border traps. A persistent increase in the photocapacitance is observed, which allows us to study the border traps with energetic localization close to the valence-band edge (E_V). Three samples exposed to different thermal treatments were studied in this experiment to enable exploration of the impact of thermal oxidation and postoxidation annealing (POA) in NO and Ar environments on the border traps. The charge-capture dynamics at these relatively slow traps have been explored under the application of external bias and varying temperatures.

A. Sample details

For the experiments, three low-doped *n*-type 4*H*-SiC samples with 30-μm-thick epitaxial layers have been used. The doping density in the epilayers was 3×10^{15} cm^{-3}, as determined by capacitance-voltage (*C*-*V*) measurements. The epilayers were grown on highly doped SiC substrates ($\sim 8 \times 10^{18}$ cm^{-3}). After dicing the wafers into 1×1-cm^2 pieces, the samples were cleaned in Piranha solution followed by tetramethylammonium hydroxide. Finally, a short HF dip was performed to remove any native oxide. The cleaned samples then underwent dry thermal oxidation at 1300 °C (1300×) and two of the three samples also received a POA in either a NO or an Ar environment at 1300 °C (1300NO1300 and 1300Ar1300, respectively). The processing details are shown in Table I. Circular Al contacts of 1.5 mm in diameter and 100 nm thick were fabricated by optical lithography and electron-beam evaporation to create MOS structures.

B. Optical excitation experiment

Optical illumination was performed by either using a light-emitting diode (LED) from Omicron Laserage or by using a laser from Light Conversion. The output wavelength of the LED is (365 ± 5) nm and has a maximum output power of 500 mW. Most of the experiments with the LED were performed at 200-mW output power, unless mentioned otherwise. During the experiment with an LED, the small signal-capacitance measurements were performed using the Boonton 7200 system with a 30-mV peak-peak ac signal at 1 MHz. The samples were enclosed in a Sumitomo Cryo system, which prevented stray light from influencing the experiment and allowed the temperature of the sample to be changed. The laser used in some of our experiments has a tunable output wavelength between 320 and 2000 nm, which allowed us to optically excite the sample with sub-band-gap and above-band-gap light. The small signal-capacitance measurements were performed using an E4980A Precision *LCR* meter from Keysight with a 30-mV peak-peak ac signal at 1 MHz, at room temperature.

II. RESULTS

A. Light-induced charge trapping

Initially, the sample is set to a desired temperature and then a dc voltage is applied. The capacitance measurement is then performed to set the initial value of the capacitance. Under optical illumination with an ultraviolet LED emitting at 365-nm (∼3.4-eV) wavelength, above the 4*H*-SiC band gap, a rise in the small-signal capacitance is observed for the MOS capacitors. The rise time varies from a few seconds to a few hundred seconds, depending on the sample, the dc bias conditions, and the optical power. At the start of the experiment, a fast rise in capacitance is observed. As time progresses, the process slows down and eventually almost no rise is seen, and the effect is considered to be saturated. At this point, the LED is turned OFF, and a sudden drop of capacitance is observed followed by a slow decay. The measurement is considered to be complete when the capacitance stops changing for at least 1 min. This phenomenon is illustrated in Fig. 1(a) (full capacitance profile), Fig. 1(b) (capacitance rise), and Fig. 1(c) (capacitance decay). As can be seen, the measured capacitance after illumination is much higher than the reference value at the start of the experiment. This is true even when the LED is turned OFF and sufficient time (up to a few hours) is provided for the capacitance to decay. Before starting the next measurement, the MOS capacitor is reset to its original state by applying a positive dc bias to strong accumulation, followed by a 0-V bias. Sufficient time is allowed for the capacitance to stabilize before the next measurement is taken.

The change in capacitance after illumination and subsequent saturation is indicated as ΔC in Fig. 1(a). This suggests the occurrence of a charge-trapping phenomenon, leading to a quasipermanent change in the system, persisting even after the removal of the external stimulus. A short

TABLE I. Description of sample preparation and processing steps.

Sample name	Oxidation parameters	Oxide thickness (nm)	POA parameters
1300×	32 min at 1300 °C	48	...
1300Ar1300	30 min at 1300 °C	48	70 min at 1300 °C in Ar
1300NO1300	28 min at 1300 °C	56	70 min at 1300 °C in NO

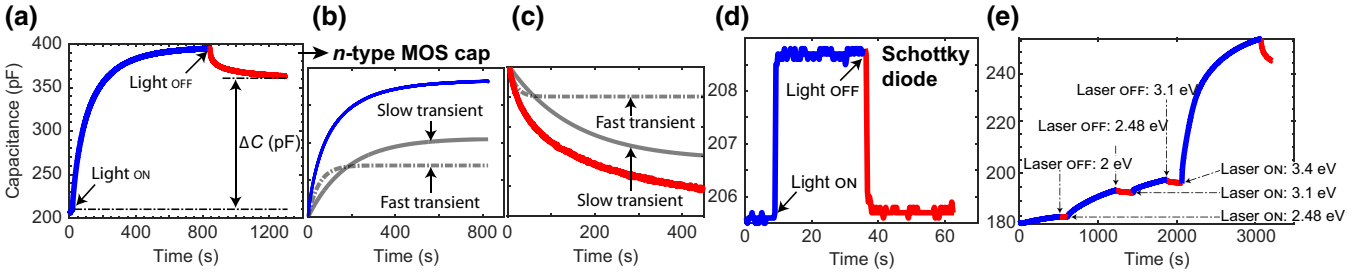

FIG. 1. Change in capacitance of the device 1300× (see Table I for sample details) as a function of time for an applied optical excitation for (a)–(c) the MOS capacitor and (d) the Schottky diode case. Panels (b),(c) show the rise and decay of the capacitance transient, respectively, for the MOS capacitor and illustrate the presence of a fast and a slow exponential component in the rise and decay. Results shown in (a)–(d) were performed with an LED. (e) Capacitance versus time under optical excitation using a laser with variable photon energy. Small increase in capacitance is observed during the OE experiment when $E_{\text{photon}} < E_g$. Increase in capacitance also persists after the laser is turned OFF. For $E_{\text{photon}} > E_g$, a rapid increase in capacitance is observed.

pulse of positive bias to the strong-accumulation region is sufficient to reset the MOS capacitor and bring the capacitance to almost the initial value. Both the rise and decay profiles of the capacitance consist of a slow and fast exponential component. This is shown in Figs. 1(b) and 1(c). While the fast component is represented by a time constant in the range of a few seconds, the slow component can take up to a few hundred seconds to saturate, depending on how the sample is processed. The fast component of the rise and decay transients is interpreted as a result of the generation and recombination of the electron-hole (*e*-*h*) pairs. The slow component, on the other hand, is likely a result of charge trapping and detrapping at defects in the SiO_2-SiC stack. The focus of this work is on the trap-related slow component.

At this point, we would like to separate defects into interface (near-interface) traps and bulk traps. As it has been shown that thermal oxidation of SiC not only introduces defects at and near the interface but also deeper into the semiconductor [19,20], it is possible that these bulk defect levels could capture the optically generated carriers and cause a change in measured capacitance. To study the impact of these bulk defects, the thermal oxide from the MOS capacitor was etched away and circular Ni contacts were deposited to prepare Schottky devices. These samples were then studied in the optical excitation (OE) experiment. The results are shown in Fig. 1(d). As the LED is turned ON, an instantaneous rise in the capacitance is observed, unlike the relatively slow rise that is observed for the MOS capacitor. Furthermore, the rise in capacitance is significantly smaller for the Schottky device (∼1% rise) in comparison to that for the MOS capacitor, where close to 100% increase in capacitance is observed. Another evident difference is in the decay behavior, where the capacitance falls sharply when the OE is removed, to almost the original value. In other words, no quasipermanent increase in the capacitance is observed for the Schottky device. This strongly indicates that no charge trapping occurs at the bulk defects and the semipermanent increase in capacitance observed for the MOS capacitor is due to charge trapping at the interface or the border traps.

To better understand the impact of interface and border traps on the capacitance under optical illumination, the samples were exposed to photons from a laser of tunable output energy. Laser excitation with photons of an energy (E_{photon}) lower than the band gap (E_g) of 4*H*-SiC results in a smaller increase of capacitance compared to photons with an energy higher than the band gap, as shown in Fig. 1(e). For $E_{\text{photon}} < E_g$, the interface traps can assist in the *e*–*h*-pair generation. Since this process is inefficient compared to band-band generation (discussed in the next section), under identical optical power, fewer holes are generated. The holes generated by trap assistance ($E_{\text{photon}} < E_g$) or band-to-band excitation ($E_{\text{photon}} > E_g$) can then tunnel from the 4*H*-SiC valence band to the border traps in SiO_2, leading to an increase in the measured capacitance. Therefore, in either case, the border traps present near E_V are mainly responsible for the capacitance change under illumination and the observed persistent photocapacitance effect.

B. Charge-trapping model

A model for the hole-trapping process is proposed to account for the observed light-induced ($E_{\text{photon}} > E_g$) changes in capacitance for the MOS capacitors shown in Figs. 1(a)–1(c). Figure 2(a) shows the band structure of the *n*-MOS capacitor at thermal equilibrium with no carriers in the depletion region and an electron surplus in the SiC bulk. Under OE with photons of energy higher than the band gap of the semiconductor, *e*-*h* pairs are generated on the SiC side of the MOS stack. For a *n*-type MOS capacitor with a positive flat-band voltage, the sample is in a depletion condition when no external bias is applied. Therefore, an electric field exists in the device, and thus, electrons generated by the LED drift away from the SiO_2-SiC interface, while the generated holes accumulate at the interface, as shown in Fig. 2(b). This leads to a drop in the

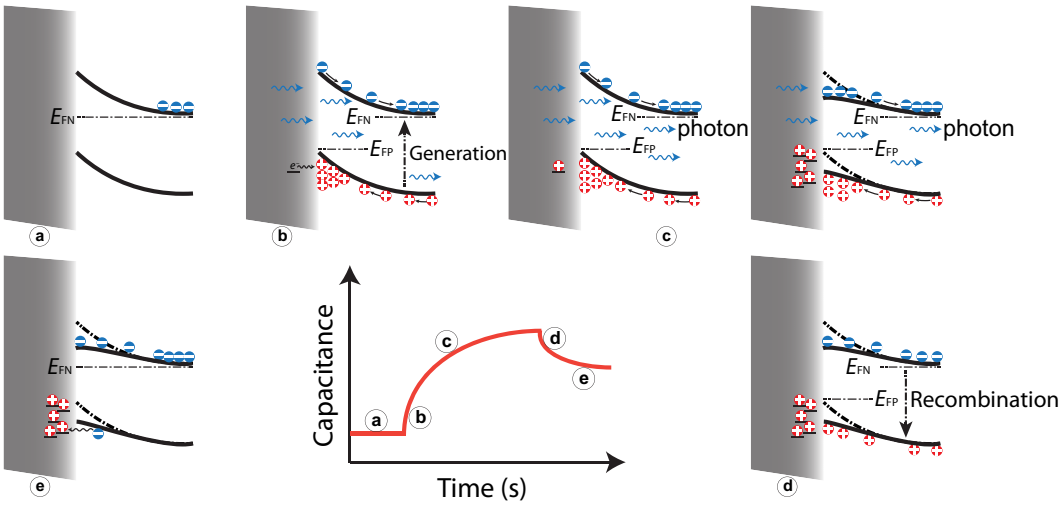

FIG. 2. Proposed model for the MOS capacitor to illustrate the generation, trapping, and recombination of charges under different operating conditions. Hole trapping at the border traps is proposed to be responsible for the rise in capacitance under the applied optical excitation.

depletion-region width, which results in a sudden rise in capacitance, as indicated by region (b) in the capacitance versus time diagram in the middle lower panel of Fig. 2. As the hole concentration increases with time, these accumulated holes can, via tunneling across the interface, be captured at the border traps in the oxide near the valence-band edge (E_V), see Fig. 2(c). With time, a positive charge builds up in the oxide, creating an electric field pointing in the opposite direction to the existing depletion field, resulting in a further reduction of the depletion-region width and an increase in the measured capacitance. The increase in capacitance is equivalent to the negative shift (reduction) of the threshold voltage. The trapped positive charges add to the external bias, resulting in a modulated equivalent bias experienced by the semiconductor. A model for the tunneling of charges from the semiconductor to the oxide and their capture at border traps, leading to a shift in the threshold voltage, is shown in Refs. [21,22].

As the optical excitation is removed, the *e-h* pairs recombine quickly, resulting in a drop in capacitance. This is shown in Fig. 2(d) and is indicated at region (d) in the capacitance versus time diagram in Fig. 2. The captured charges at the border traps possibly experience an increased barrier and do not tunnel back to the semiconductor. Therefore, although the capacitance drops slightly, it remains significantly higher than the pre-OE value, leading to the observation of a persistent photocapacitance effect. Similar effects have been observed in different material systems, e.g., strontium titanate [23], $Ga_xIn_{1-x}N_yAs_{1-y}$ [24], and GaN [25], where a persistent increase in conductance was observed after optical illumination. With time, the trapped charges can tunnel back to the semiconductor, but, based on the time constant of the decay transient, this phenomenon could take hours to a few days. On average, the decay time for the 1300× sample is in the range of 1×10^5 s, which is equivalent to 5–6 days. In Ref. [26], retention times as long as 1×10^9 years were estimated for 4*H*-SiC MOS capacitors, leading to the suggestion that SiC-MOS capacitors could be used as a nonvolatile memory element.

Under OE, as holes accumulate near the interface, the probability distribution of holes in the valence band is defined by a quasi-Fermi level (E_{FP}) near the valence-band edge. Since border traps in SiO_2 are assumed to be spatially located very close to the interface [27], the charge state of these traps would also be determined by their energetic position with reference to E_{FP} [28]. The border traps near E_V are expected to mainly capture holes [29]. This means that we expect a charge-state transition, e.g., from (0/+) or (−/0) if one hole is captured, or a negative-*U* transition like (−/+) or (0/2+) if two holes are captured. This would result in positive charge accumulation in the oxide, leading to an increase in capacitance. Furthermore, the persistent increase in capacitance at the end of the experiment provides evidence that the holes captured during OE do not find their way back to the semiconductor after the OE is removed. This phenomenon can be understood by a defect-configuration coordinate diagram, as shown in Fig. 3. When a charge carrier is trapped at a so-called deep-level defect, its wave function can be localized at the defect site. In this case, a change in the charge state of the defect can have a strong impact on the geometry of neighboring atoms [30]. Accounting for the deformation of the defect site due to the change in its charge state, a nonradiative multiphonon (NMP) approach can be employed to study the behavior of the border traps [31,32]. In this representation (illustrated in Fig. 3), the defect has two configurations: State 01, ground state, with an electron;

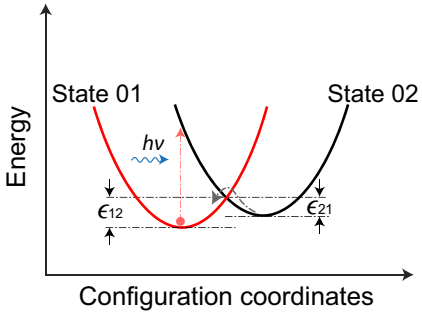

FIG. 3. Parabolic approximation in the nonradiative multiphonon (NMP) model to account for the deformation of the defect site. Upon optical excitation, the defect level can transform from State 01 (red parabola) into State 02 (black parabola). After optical excitation is removed, the barrier to transition from State 02 to State 01 is ϵ_{21}.

and State 02, excited state after the capture of a hole. As shown, the transition of State 01 to excited State 02 has a barrier of ϵ_{12}. If the incoming photon has sufficient energy, it could excite the defect and help overcome the barrier, as indicated by the red arrow in Fig. 3. After the capture of a hole, the defect reaches State 02, leading to charge build up in the oxide. After optical illumination is removed, for the defect to revert back to State 01, it must overcome a barrier of ϵ_{21}. In the absence of enough thermal energy, the defect would stay in State 02, leading to a quasipermanent charging of the oxide and a persistent increase in the capacitance after exposure to above-band-gap light.

C. Dynamics of the trapping process

To better understand the dynamics of charge trapping at the border traps, several OE experiments were performed on the samples at varying gate bias and ambient temperature. Figure 4(a) shows the rise transient as a function of gate bias for the thermally oxidized sample, 1300× (see sample details in Table I). At constant temperature, as a larger negative bias is applied to the sample, the capacitance rises more slowly. Therefore, the time constant of the rise in capacitance is a function of the applied gate bias. This dependence is exponential and is illustrated in Fig. 4(b). Similarly, for a fixed dc bias and with increasing temperature, the time constant associated with the rising capacitance transient increases [see Fig. 4(c)]. Similar dependencies of the rise-time constant on the temperature and dc bias are observed for the NO- and Ar-annealed samples. These two observations indicate that the hole-capture rate is a function of both bias and temperature. However, under the application of bias, as the sample moves from the flat-band condition to depletion, the pre-OE capacitance changes and moves along the *C-V* curve. Since the *C-V* curve is inherently nonlinear, the rise in capacitance under OE at different points on the *C-V* curve is not the same. Near the flat-band condition, the rise is faster when compared to that under the depletion conditions; this results in an increase in the rising-time constant with increasing negative bias. Due to this reason, comparing only the extracted time constant of the rising exponential for different biases may result in an inaccurate interpretation of the hole-capture rate.

Therefore, we have carried out a temporal evaluation to quantify the hole-capture rate during the OE experiment using

$$\frac{dQ_{ox}}{dt} = (C_{ox} - C_S(t))\frac{d\Psi_S}{dt}, \tag{1}$$

which establishes a relationship between the rate of change of charges in the oxide to the changing capacitance under optical illumination. The derivation of Eq. (1) is shown in the Appendix.

Using Eq. (1), the hole-capture rate is evaluated for the MOS capacitors at varying biases and the results are illustrated in Fig. 5. It was shown in Fig. 4 that the time constant of the rising transients increased as the negative bias was increased, which could be interpreted as a reduction in the hole-capture rate for reducing gate biases. This is,

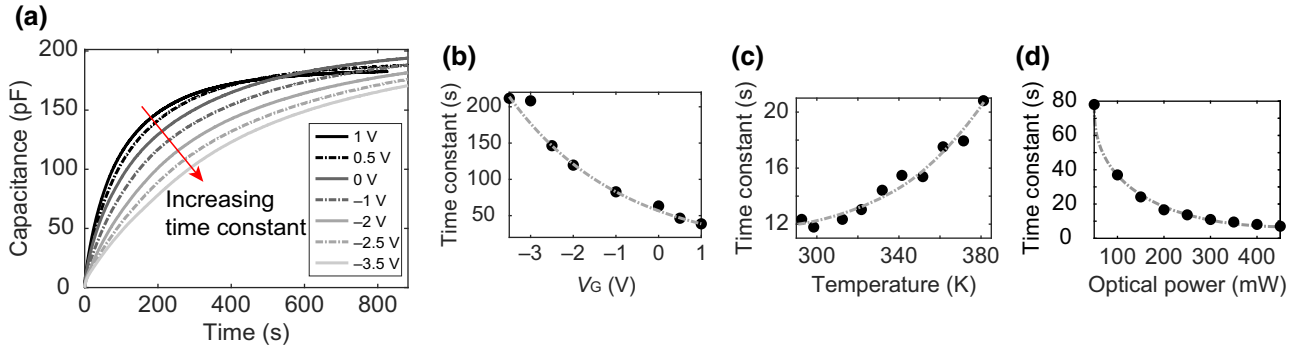

FIG. 4. (a) Rising capacitance of the 1300× sample upon the application of optical excitation using an LED as a function of applied bias. Extracted time constant is shown as a function of gate bias (b) and temperature (c). (d) Dependence of the time constant on the optical power is illustrated. Measurement is performed at 293 K and 0-V dc bias.

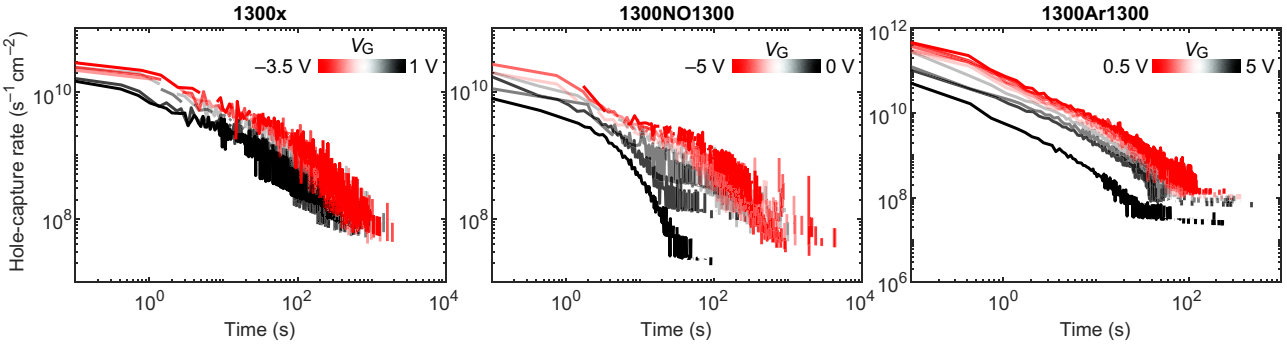

FIG. 5. Hole-capture rate evaluated as Q_{ox} from Eq. (1) for the thermally oxidized and annealed samples (left, 1300×; middle, 1300NO1300; right, 1300Ar1300) during the OE experiment with a fixed temperature of 293 K and variable bias. It is observed that, for all the samples, the capture rate increases as a larger negative bias is applied to the MOS capacitors.

however, not the case when the evaluation is performed using Eq. (1), and it is seen that the hole-capture rate increases for the thermally oxidized (1300×) and annealed samples (1300NO1300, 1300Ar1300) as a more negative gate bias is applied. This agrees well with the predictions from theory [31]. Moreover, a similar evaluation was performed for measurements performed at a fixed bias and varying temperatures, and the results are shown in Fig. 8 in the Appendix. The hole-capture rate seems to be only slightly affected by temperature for all three samples. Since the optical generation of *e-h* pairs in SiC and the tunneling process of holes across the interface are both temperature independent, the overall capture rate of holes is expected to be weakly dependent on or independent of temperature.

The dependence of the capture rate on the applied bias (V_B) is further investigated by technology computer aided design (TCAD) simulations. The doping concentration of the semiconductor is defined as $3 \times 10^{15}\,cm^{-3}$ in the simulation, which is equal to the doping concentration of the measured sample. The simulated band bending in the oxide and the semiconductor for varying external bias is shown in Fig. 6(a). After calculation of the potential profile in the MOS structure at −3-V external bias, a point is chosen at a distance of x_T nm from the SiO_2-SiC interface at an energy ΔE above E_V. As the external bias is varied from −3 to 1 V, ΔE changes from ΔE_2 to ΔE_1. This behavior is illustrated in the inset of Fig. 6(a). Figure 6(b) shows the schematic configuration-coordinate (CC) diagram for the capture of holes from E_V to the border trap. State 01 is the initial configuration of the defect level, which must transform into State 02 to capture a hole, where State 02 is aligned with E_V. This transition has a barrier ϵ_{12} at 1-V external bias. As the external bias is reduced to −3 V, the barrier is also reduced to ϵ'_{12}. Therefore, although the energetic difference (ΔE) between the valence-band edge and the defect level increases from ΔE_1 to ΔE_2 for increasing negative bias, the overall barrier is reduced from ϵ_{12} to ϵ'_{12}, leading to an increase in the capture rate of holes, as seen in Fig. 5.

D. Density of trapped charge at border traps

The concentration of trapped holes in the oxide can be quantified by monitoring the change in capacitance and voltage of the MOS capacitor during the OE experiment. As discussed above, under OE, a rise in capacitance from

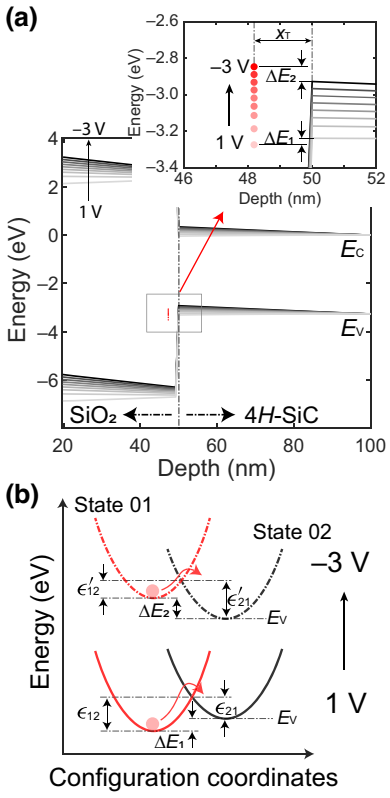

FIG. 6. (a) TCAD simulation of the oxide-semiconductor structure under varying gate bias. Inset, variation in the energy difference (ΔE) between a chosen defect level in the oxide and E_V, depending on the gate bias. (b) CC diagram for the border traps. Although the energy difference between the defect level and E_V increases from ΔE_1 to ΔE_2 for increasing negative gate bias, the energy barrier for the transition from State 01 to 02 reduces from ϵ_{12} to ϵ'_{12}.

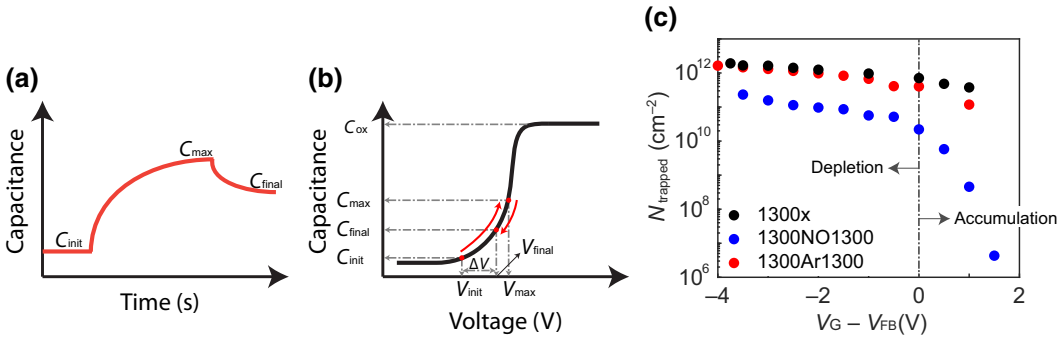

FIG. 7. (a) Representative example of the optical excitation experiment. (b) Capacitances C_{init}, C_{max}, and C_{final} are located on the C-V curve, and corresponding voltages are extracted. (c) Using information about the initial and final capacitances and voltage, the concentrations of trapped positive charges in the oxide are calculated and shown as a function of applied gate bias for the three samples.

the initial value, C_{init}, to the maximum capacitance, C_{max}, is observed; this is first caused by e–h-pair generation followed by a slow increase due to trapping of charges in the border traps. When the OE is removed, the capacitance drops from C_{max} to C_{final}, where C_{final} is much higher than C_{init} for the MOS capacitors studied herein. This is shown in Fig. 7(a). Looking at the C-V curve shown in Fig. 7(b), the change in capacitance is equivalent to traversing the C-V curve where the equivalent bias on the sample is changing. Therefore, when the final capacitance of the sample is C_{final}, the equivalent voltage on the sample is V_{final}. This means that, due to hole trapping by the border traps, the MOS capacitor experiences an effective increase in bias, which is given by $\Delta V = V_{final} - V_{init}$.

To calculate the number of trapped charges during the OE experiments, we have derived (derivation in the Appendix) the following:

$$\Delta Q_{ox} = \frac{\epsilon_0 \epsilon_{SiC} q N_D}{2}\left(\left(\frac{1}{C_S^{init}} - \frac{1}{C_S^{final}}\right) + \left(\frac{1}{(C_S^{final})^2} - \frac{1}{(C_S^{init})^2}\right) C_{ox}\right), \qquad (2)$$

which relates the number of trapped charges to the initial (before optical excitation) and final (at the end of the experiment) capacitance of the semiconductor. Using Eq. (2), we have performed an evaluation of the total number of trapped charges per unit area by using $N_{trapped} = \Delta Q_{ox}/(q \text{ area})$. However, this calculation is only valid while the MOS capacitor is under depletion conditions, as the relationship used between ψ_s and C_S is only valid for depletion. For this reason, the flat-band voltage (V_{FB}) is subtracted from the applied dc bias to clearly distinguish between the depletion and accumulation regions. The calculated values for the density of trapped holes ($N_{trapped}$) for the three samples (1300×, 1300NO1300, and 1300Ar1300) are plotted in Fig. 7(c). The thermally oxidized sample, which does not receive any postoxidation treatment (1300×), has an almost equivalent concentration of trapped oxide charges to that of the Ar-annealed sample (1300Ar1300), reaching a maximum of $N_{trapped} \approx 1 \times 10^{12}$ cm^{-2} under depletion conditions. This indicates that the oxide traps created near the valence-band edge during thermal oxidation are almost unaffected by the POA in Ar. The sample annealed under NO (1300NO1300), on the other hand, exhibits a substantially lower concentration of trapped charges in comparison to the 1300× sample by almost an order of magnitude, which suggests that annealing in a NO environment not only passivates the defects at the interface, leading to a reduction of the density of interface traps [33], but also causes a reduction in the border-trap density, leading to a reduction of the overall trapped charges in the oxide.

III. CONCLUSION

In this work, a method to characterize the border traps present near the valence-band edge of n-type 4H-SiC MOS capacitors is presented. The capacitance of the MOS structure is found to change under optical illumination and with varying bias and temperature. The measurements reveal a persistent photocapacitance effect, which is facilitated by the presence of border traps in the oxide and in the vicinity of the interface. A framework has been developed to calculate the concentration of trapped charges in the oxide responsible for the observed increase in capacitance. It was found that, immediately after thermal oxidation, the concentration of trapped charges was at its highest, while postoxidation annealing in an Ar environment reduced it slightly. A significant reduction, by almost an order of magnitude, is observed after postoxidation annealing under NO.

The charging dynamics of the border traps were also studied, and it was found that, for all the samples, the hole-capture rate increased as the bias was reduced, while the rate was almost independent of temperature. Comparing

the samples, it was observed that the capture rate was highest for the Ar-annealed sample (1300Ar1300), while the nonannealed (1300×) and NO-annealed (1300NO1300) samples had comparable hole-capture rates.

In conclusion, our findings demonstrate that the approach developed herein reveals in-depth information on the formation and dynamics of border traps near the valence-band edge in 4*H*-SiC *n*-type MOS capacitors. This could be pivotal in understanding and improving the bias-temperature instability in SiC power MOSFET devices.

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APPENDIX

1. Hole-capture-rate evaluation at varying temperatures

The OE experiment was performed on the thermally oxidized (1300×) and annealed samples (1300NO1300, 1300Ar1300) for a fixed dc bias of 0 V and varying temperature. Using Eq. (A7), the hole-capture rate was evaluated, and the results are shown in Fig. 8. Over the evaluated temperature range, the capture rate is fairly independent of the temperature for all three samples.

2. Derivation: Hole-capture rate

To quantify the hole-capture rate during the OE experiment, we have carried out the following evaluation. For a MOS capacitor, the applied gate voltage (V_G) drops partially in the oxide and in the semiconductor. By Kirchhoff's voltage law (KVL),

$$V_G + V_{FB} + V_{ox} + \Psi_S = 0, \tag{A1}$$

where V_G is the applied gate bias, V_{FB} is the flat-band voltage defined by the difference of the Fermi levels of the gate metal and the semiconductor, V_{ox} is the potential drop across the oxide, and Ψ_S is the potential drop across the semiconductor. Taking derivatives with respect to time on both sides,

$$\frac{dV_G}{dt} + \frac{dV_{FB}}{dt} + \frac{dV_{ox}}{dt} + \frac{d\Psi_S}{dt} = 0. \tag{A2}$$

Since V_G and V_{FB} are time independent,

$$\frac{dV_G}{dt} = \frac{dV_{FB}}{dt} = 0 \quad \text{and} \quad \frac{dV_{ox}}{dt} = -\frac{d\Psi_S}{dt}. \tag{A3}$$

Furthermore, applying charge neutrality to the MOS device, we find that $Q_G + Q_{ox} + Q_S = 0$, where Q_G is the charge on the gate metal, Q_{ox} is the oxide charge, and Q_S is the charge in the semiconductor. Again, taking derivatives with respect to time on both sides and by variable change in the derivative, we arrive at Eq. (A6), where the change of Q_G as a function of V_{ox} is defined as the oxide capacitance, C_{ox}, and the change of the semiconductor charge, Q_S, as a function of Ψ_S is defined as the semiconductor capacitance, C_S. By using the relationship established between Ψ_S and Q_{ox} ($dV_{ox}/dt = -d\Psi_S/dt$), Eq. (A6) can be modified to Eq. (A7). This equation establishes a relationship between the rate of change of charges in the oxide to the

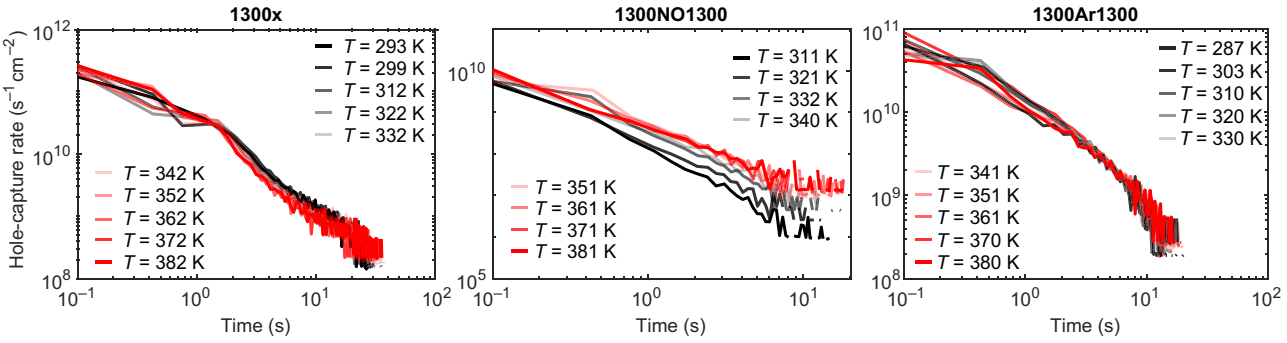

FIG. 8. Hole-capture rate evaluated for the thermally oxidized and annealed samples (left, 1300×; middle, 1300NO1300; right, 1300Ar1300) during the OE experiment with a fixed bias of 0 V and variable temperature. It is observed that the hole-capture process is fairly independent of temperature over the measured range.

changing capacitance under optical illumination.

$$\frac{dQ_G}{dt} + \frac{dQ_{ox}}{dt} + \frac{dQ_S}{dt} = 0, \tag{A4}$$

$$\frac{dQ_G}{dV_{ox}}\frac{dV_{ox}}{dt} + \frac{dQ_{ox}}{dt} + \frac{dQ_S}{d\Psi_S}\frac{d\Psi_S}{dt} = 0, \tag{A5}$$

$$-C_{ox}\frac{d\Psi_S}{dt} + \frac{dQ_{ox}}{dt} + C_S(t)\frac{d\Psi_S}{dt} = 0, \tag{A6}$$

$$\frac{dQ_{ox}}{dt} = (C_{ox} - C_S(t))\frac{d\Psi_S}{dt} \tag{A7}$$

3. Derivation: Density of trapped charges

Using KVL and charge neutrality in a MOS capacitor, as described in the previous section, we arrive at Eqs. (A8) and (A9):

$$V_G + V_{FB} + V_{ox} + \Psi_S = 0, \tag{A8}$$

$$Q_G + Q_{ox} + Q_S = 0, \tag{A9}$$

$$V_G - \frac{Q_{ox} + Q_S}{C_{ox}} + V_{FB} + \Psi_S = 0. \tag{A10}$$

V_G and V_{FB} are constant, while Q_{ox}, Q_S, and ψ_S vary from the start to the end of the experiment. Using Eq. (A10) before optical excitation (init) and after removing the optical illumination (final) and taking the difference of the two equations, we arrive at

$$\frac{(Q_{ox}^{final} - Q_{ox}^{init}) + (Q_S^{final} - Q_S^{init})}{C_{ox}} + (\Psi_S^{init} - \Psi_S^{final}) = 0. \tag{A11}$$

Rearranging the terms and using the relationship $\psi_S = (\epsilon_0\epsilon_{SiC}qN_D)/(2C_S^2)$ (depletion) yields Eq. (A13), which establishes a relationship between the stored oxide charge (ΔQ_{ox}) and the change in semiconductor capacitance:

$$\begin{aligned}\Delta Q_{ox} &= Q_{ox}^{final} - Q_{ox}^{init} \\ &= (Q_S^{final} - Q_S^{init}) + (\Psi_S^{final} - \Psi_S^{init})C_{ox}\end{aligned} \tag{A12}$$

$$\begin{aligned}\Delta Q_{ox} = \frac{\epsilon_0\epsilon_{SiC}qN_D}{2}\Bigg(&\left(\frac{1}{C_S^{final}} - \frac{1}{C_S^{init}}\right) \\ &+ \left(\frac{1}{(C_S^{final})^2} - \frac{1}{(C_S^{init})^2}\right)C_{ox}\Bigg)\end{aligned} \tag{A13}$$

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