Pure edge-dislocation half-loops in low-temperature GaN for V-defect formation

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Lateral injection of carriers through semipolar crystallographic planes into *c*-plane QWs is one of the new frontiers in III-N light-emitting diodes (LEDs), especially for long wavelengths. Strategic use of V-defects has proven to be the most promising method for lateral injection, and creating optimal V-defect structure and density is an important research area for reducing forward voltage and increasing wall plug efficiency. In this article, we present a novel method for forming V-defects in nominally unstressed low-temperature GaN through the generation of pure edge-dislocation half-loops. We present a detailed material science analysis of the loops via scattering-contrast electron microscopy. The loops have pure-edge character with Burgers vector $1/3\ \langle 11\bar{2}0\rangle$, and form in a sessile orientation on $\{11\bar{2}0\}$ *a*-planes. The two arms of the loops are inclined such that the extra half-planes face down toward the growth substrate. The dislocation loops can be used to intentionally form V-defects through conditions of kinetically limited growth: these conditions also favor nucleation of V-defects at ∼100% of other threading dislocations in the GaN templates. Patterned sapphire substrates (PSS) are one of the most important substrates for III-N LED growth because of their superior light extraction. However, due to its low threading dislocation density, PSS have not been used extensively for V-defect LEDs. This work provides a pathway for improved control of V-defect formation and density on LEDs grown on sapphire with the goal of enabling uniform lateral injection in these V-defect engineered LEDs with low forward voltage, including PSS for high light extraction.

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I. INTRODUCTION

Recent work on III-N light-emitting diodes (LEDs) has demonstrated that, as the indium composition and wavelength are increased, polarization barriers to carrier injection severely limit the ability of both electrons and holes to populate the quantum wells in *c*-plane LEDs [1–3]. This poses a significant challenge for red and green InGaN LEDs due to a low current injection, leading to high forward voltage and low carrier concentrations in the quantum wells (QWs). These barriers to carrier transport also make it extremely difficult to inject deeper QWs. Laterally injected III-N LEDs are the most promising solution to the problem of carrier injection at long wavelengths [4–7]. Because a significant portion of the potential barrier arises from the high polarization of the *c*-plane, injecting carriers through a semipolar or nonpolar plane in a "3D" device architecture is a promising solution to mitigate some of the forward voltage issues in long-wavelength InGaN [8,9]. So far, the literature on lateral injection LEDs focuses on the strategic use of naturally occurring V-defects as the pathway for lateral injection of electrons and holes. These naturally occurring defects are inverted hexagonal pyramids with six semipolar $\{10\bar{1}1\}$ faces. For green and red LEDs, the strain-induced polarization by the high In fraction *c*-plane QWs significantly increases the injection barriers. However, the In uptake is dramatically reduced on the semipolar sidewalls of the V-defects, which further enhances the ability of carriers to enter the QWs [10]. Furthermore, the Ga uptake is also greatly reduced leading to thinner sidewall QWs, which further facilitates carrier transport [11].

Dislocation generation and structural evolution in GaN films grown on sapphire are important for understanding and improving the performance of laterally injected InGaN LEDs [12,13]. GaN growth on sapphire usually starts with a low-temperature nucleation layer where small islands of highly defective GaN are initiated. Subsequent high-temperature growth results in nearly defect-free 3D islands, followed by island coalescence and planarization of the growth surface. The threading dislocations (TDs) form primarily during the 3D island growth and

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coalescence [14,15]. The TDs form to accommodate the slight misorientation of the high-temperature GaN islands [16].

Threading dislocations are of great importance in the formation of V-defects [17]. V-defects readily form on threading dislocations because the surface energy of a dislocation meeting the surface will cause a slight surface depression, which becomes the nucleation site for a V-defect under favorable growth conditions [18]. V-defects tend to form more readily on mixed-type TDs (with Burgers vector $\boldsymbol{b} = \pm(\boldsymbol{a_i} \pm \boldsymbol{c}) = 1/3\langle 11\bar{2}3\rangle$, where $\boldsymbol{a_i}$ and $\boldsymbol{c}$ are the lattice translations for the wurtzite GaN structure) compared with pure-edge TDs $\left(\boldsymbol{b} = \pm\boldsymbol{a_i} = 1/3\langle 11\bar{2}0\rangle\right)$ because the surface depression from a mixed-type dislocation is larger [19]. It has also been demonstrated that V-defects affect the way in which a threading dislocation bends. It is at least the case in mixed-type dislocations that the threading dislocation will bend onto one of the six semipolar faces after the V-defect has formed [11]. Because V-defects form more readily on mixed TDs, early work on V-defect-engineered LEDs was primarily from LEDs grown on (111)-Si substrates, which have a high fraction of mixed TDs compared with the pure edge [20–22]. V-defect engineered LEDs grown on sapphire are slightly more difficult because most of the TDs are pure edge and the threading dislocation density (TDD) is low, especially on patterned sapphire substrates (PSS) [23,24]. The latter is one of the most important substrates for III-N LEDs because of its high light extraction (>90%) [25].

During epitaxial growth, the corrugation potential is the energy needed for species to move between sites on a growth surface. A high corrugation potential means that adatoms tend to get "trapped" at local minima more easily, whereas a low corrugation potential means that adatoms can easily move across the surface and have high adatom mobility [26]. In GaN epitaxy, the corrugation potential varies significantly depending on the crystal plane and whether the growth is on the Ga-face (0001) or N-face $(000\bar{1})$. Ga-face-(0001) GaN has a much lower corrugation potential and, thus, it is much easier to attain step-flow growth. For growth on closed packed planes, such as {0001} for wurtzite structures or {111} for zinc blende structures, step-flow growth is essential to sustain the correct stacking sequence. Under conditions of very large terrace widths or low adatom surface mobility for growth on close-packed planes, stacking errors can occur due to 2D island growth distant from the step edges on a terrace: this may result in stacking fault (SF) formation where the SFs are bound by partial dislocations. Achieving defect-free, step-flow growth is predicated on the ability of adatoms to reorganize on the surface and move to step edges. Thus, when corrugation potential is high or when adatom has less thermal energy (i.e., low-temperature growth), we expect to see more defects (such as stacking faults) forming in the crystal [27,28]. This is the reason for significantly higher basal stacking fault concentration on N-face GaN and in growth on the *a*-plane and *m*-plane [29,30]. In nearly all epitaxial systems, low-temperature growth will see significantly higher formation of stacking faults and other defects, irrespective of stress, due to the lower adatom mobility [31,32].

The generation of new threading dislocations is rarely observed after the initial 2D to 3D growth and coalescence of islands for the *c*-plane growth of GaN under typical LED growth procedures. Some reports suggest that dislocations may form due to stress in alloy layers, grown coherently on underlying GaN layers, but the mechanisms for such dislocation formation are poorly understood [33]. There are few reports on half-loop generation in GaN layers without the presence of stressed InGaN or AlGaN layers [34,35]. A TD half-loop formation has been observed in previous reports on basal stacking faults [36]. The I_1 stacking fault in GaN, which is the one most observed, forms due to growth errors, which occur when surface mobility is low [37]. An I_1 basal stacking fault (BSF) formation is *not* fundamentally a stress-driven process. Instead, it is associated with low-temperature growth or a species like Al, which has relatively low surface mobility compared with In or Ga. There has been some recent work on how the generation of stacked I_1 BSFs can form stacking fault boxes, which have been shown to generate between 2 and 6 threading dislocations [38,39]. This occurs because the overlap of the I_1 BSFs will acquire Shockley-like partial dislocations and may lead to extra threading dislocations out of geometric necessity [40].

In this paper, we present evidence for pure-edge half-loop generation in low-temperature grown nominally unstressed GaN layers. The formation of the half-loops, which are missing planes of atoms in the crystal, is attributed to growth kinetics, low adatom mobility, and "growth errors" in the low-temperature grown GaN layer. In addition, we show clear evidence through scattering-contrast transmission electron microscopy (TEM) of the formation of V-defects on pure-edge-type TDs from the substrate and from half-loops. These results are highly relevant to V-defect engineering for lateral injection on sapphire, where most of the TDs are pure edge and where the TDD is often insufficient for complete lateral injection.

II. METHODS

The GaN samples, denoted by A and B, studied in this paper were grown by atmospheric pressure metalorganic chemical vapor deposition (MOCVD). The n-type GaN preparation layers were grown n-GaN on PSS templates from Enkris semiconductor. The templates consisted of 3 μm of unintentionally doped (UID) GaN and 2 μm of n-doped GaN ($[\mathrm{Si}] > 3 \times 10^{18}$ cm^{-3}). The MOCVD growth at our research university UCSB started with 500 nm of n-doped GaN ($[\mathrm{Si}] \sim 5 \times 10^{18}$ cm^{-3}) and then

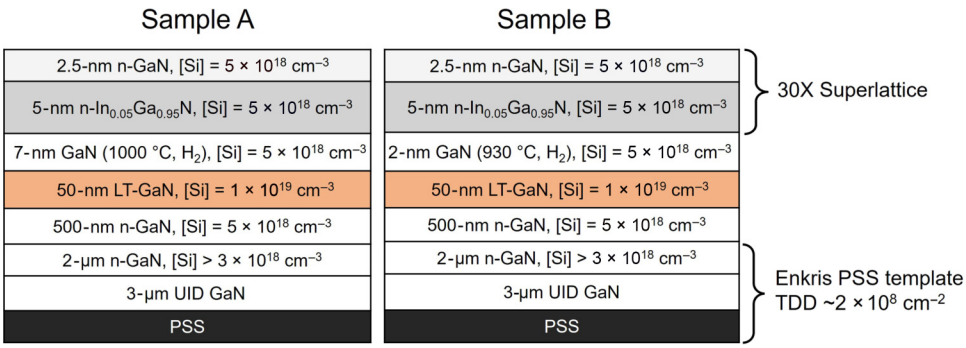

FIG. 1. Epitaxial structure of the LT-GaN templates used to generate half-loops and nucleate V-defects.

50 nm of low-temperature (LT) GaN grown at ∼800 °C with an N_2 carrier gas at a growth rate of 50 nm/min with a disilane flow of 7 sccm. After the low-temperature growth, the temperature was increased to ∼1000 °C for Sample A and 930 °C for Sample B. Next, 7 nm of GaN (Sample A) and 2 nm (Sample B) were grown in H_2 followed by a 30-period 5-nm $In_{0.05}Ga_{0.95}N$/2.5-nm GaN superlattice (SL) with [Si] ∼ 5×10^{18} cm^{-3} at ∼930 °C. The structures are shown in Fig. 1. No active region was grown on these samples.

Scattering-contrast TEM and high angle annular dark-field (HAADF) scanning TEM (STEM) were performed in both cross-section and plane-view configurations with two microscopes: one is a Thermo Fisher Scientific Talos G2 200X TEM/STEM system equipped with energy dispersive x-ray spectroscopy (EDS), another is a Thermo Fisher Scientific Spectra 200 S/TEM. Backscatter scanning electron microscopy (SEM) was performed using an FEI Nova Nano 650 FEG SEM. Cathodoluminescence (CL) measurements were performed using a Gatan MonoCL4 with mono- and pan-chromatic capabilities attached to a field emission scanning electron microscope (Thermo Fisher Apreo C LoVac SEM) operating at 5 kV with a beam current of 0.8 nA.

III. RESULTS

Figure 2 shows a plane-view backscatter (BS) SEM image of Sample A. Because the growths were stopped after LT-GaN and SL growth, the V-defects remain open and can be easily observed in plane-view SEM. The large V-defects can be seen as dark hexagons in the BS SEM

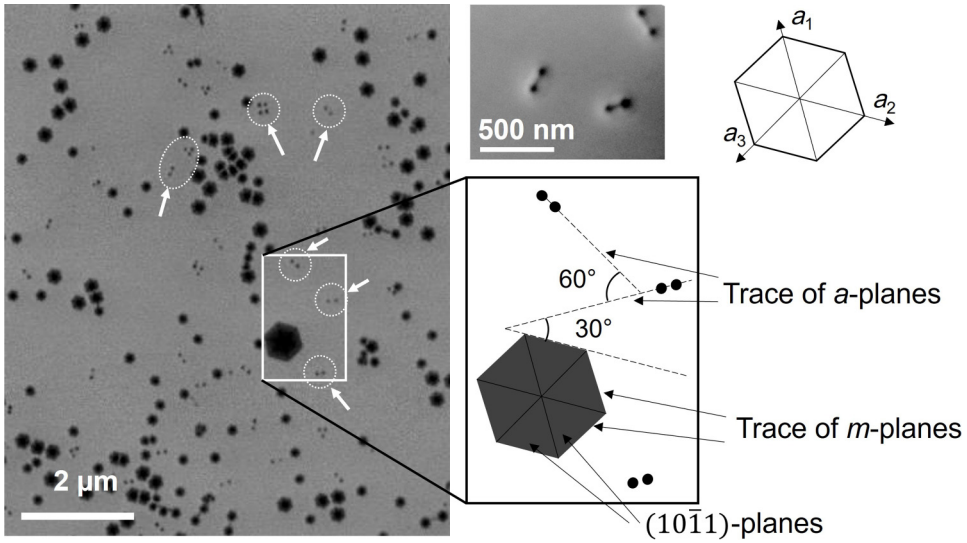

FIG. 2. Backscatter SEM images (left and higher magnification at top right) of the epitaxial surface of Sample A showing the large V-defects generated on mixed and pure-edge TDs. The small pairs of surface depressions correspond to half-loop generation; some of these pairs are indicated with a dashed circle and white arrow. It can be seen from the schematic that the pairs of surface depressions are aligned with the intersection of the *a*-plane and *c*-plane (trace of the *a*-plane) and are rotated 30° from the trace of the *m*-plane and the top of {10$\bar{1}$1}-plane sidewalls of the large V-defects [the dashed lines in the schematic correspond to the trace (intersection) of the *m*-planes and *a*-planes with the *c*-plane].

image. These large V-defects (100–800 nm in diameter) form on the TDs that are generated in the 2D–3D GaN growth. On PSS, the TDs cluster around sapphire pyramids, which is often reflected in the V-defect distribution. In addition, lines of V-defects are observed. These are most likely the result of rows of pure-edge TDs that form at coalescence boundaries during the 2D–3D high-temperature GaN growth. Furthermore, it is expected that there will be a size difference between mixed $(\boldsymbol{a}+\boldsymbol{c})$ and pure-edge TDs because the mixed TDs have a higher line tension where the TD meets the crystal surface and will form a larger initial surface depression. It is this larger surface depression that forms larger V-defects more readily. Here, we see both pure-edge and mixed TDs nucleating V-defects. This is confirmed later in the paper with cathodoluminescence and cross-sectional TEM.

In addition to the large V-defects, we observe pairs of small surface depressions where the direction separating the paired depressions coincides with the trace of the *a*-plane, i.e., $\langle 10\bar{1}0\rangle$ *m*-directions. V-defects have $\{10\bar{1}1\}$ sidewalls which, viewed from above, are parallel to the trace of the *m*-plane intersection with the *c*-plane, i.e., $\langle 11\bar{2}0\rangle$ *a*-direction. These small defect pairs, or in some cases triplets and quadruplets, lie 30° from the trace of *m*-plane (which are traces of *a*-planes) as illustrated in Fig. 2. Triplet formation has not been predicted in the literature for half-loop formation in GaN.

Figure 3 shows cross-sectional HAADF images of a half-loop forming in an LT-GaN layer in Sample A. An edge dislocation loop initiates with a small U-shaped dislocation in the LT-GaN layer lying on the *a*-plane. Above the U-shape, two pure-edge threading dislocation arms split off and then began to separate in a climblike geometry in the GaN before the SL growth. It appears that the climblike behavior is initiated when the growth temperature is increased from 800 °C to 1000 °C. This would suggest that there is an energetic driving force for climblike behavior, but it only occurs if there is sufficient adatom mobility during the MOCVD growth. The TDs separate further in the SL and eventually generate a pair of small depressions on the surface. It is notable that the half-loop forms during homoepitaxial growth and not in a stressed InGaN or AlGaN layer.

To examine the nature of the dislocation, scattering-contrast TEM was carried out, as shown in Fig. 4. The dislocation shows faint contrast in $\boldsymbol{g}=\bar{1}100$ [Figs. 4(a) and 4(b)], and is nearly invisible in $\boldsymbol{g}=000\bar{2}$ [Figs. 4(c) and 4(d)], indicating that the Burgers vector is vertical to $\boldsymbol{g}=\bar{1}100$ and $\boldsymbol{g}=000\bar{2}$, i.e., the Burgers vector is $1/3\langle 11\bar{2}0\rangle$, a pure **a**-type dislocation. The weak beam dark-field image (DF) with $\boldsymbol{g}=1\bar{2}1\bar{2}$ show a narrow U-shape, as shown in Fig. 4(e). Taken in the opposite diffraction vector, the U-shape is wider, as shown in Fig. 4(f). This is a typical feature of loop dislocation [41]. The images in Figs. 4(e) and 4(f) of loop dislocation are either inside or outside of the real core position depending on the value of $(\boldsymbol{g}\cdot\boldsymbol{b})s$, where *s* is the deviation parameter. In 1g/3g weak beam conditions, *s* is positive and a change in the sign of $\boldsymbol{g}$ will change $(\boldsymbol{g}\cdot\boldsymbol{b})s$; as a result, one image shows a narrow U, while another image shows a wider U with opposite $\boldsymbol{g}$.

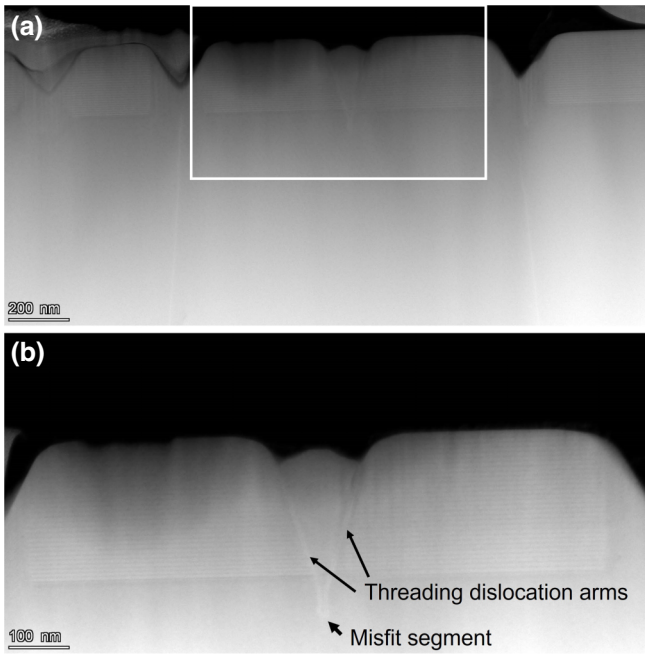

FIG. 3. (a),(b) Cross-sectional HAADF TEM images showing the half-loop formation and the climblike behavior of the TDs in the *m*-direction. In (a), several V-defects can be seen forming on TDs from the initial GaN on sapphire growth, while (b) displays the higher magnification image indicated by the white box in (a).

Figure 5 shows plane-view DF scattering-contrast TEM images of a half-loop forming on the *a*-plane. Strong dislocation contrast is observed in all directions except for $\boldsymbol{g}=10\bar{1}0$. Since no contrast is observed when $\boldsymbol{g}\cdot\boldsymbol{b}=0$, this indicates that the Burgers vector $\boldsymbol{b}$ is $1/3\langle 11\bar{2}0\rangle$, oriented in the *a*-direction. The dislocation lies on the *a*-plane and has a climblike geometry. The sense of climb is in the *m*-direction.

Figure 6(a) shows a schematic in 3D of the half-loop in GaN. The misfit segment is shown at the bottom, with two TD arms extending and terminating in small depressions that meet the crystal surface. The missing half-plane with an *a*-direction and a Burgers vector $\boldsymbol{b}=(1/3)[11\bar{2}0]$ is shown. Figure 6(b) is a HAADF plane-view image of the surface of the crystal where the half-loop structure meets the crystal surface and forms two small surface depressions. Figures 6(c) and 6(d) show close-ups of each side of the half-loop structure. A circuit was drawn around the end of dislocation, as indicated by the black dots and arrows in Figs. 6(c) and 6(d). Here, it is obvious that the half-loop is the result of the removal of a single plane of atoms along the *a*-plane.

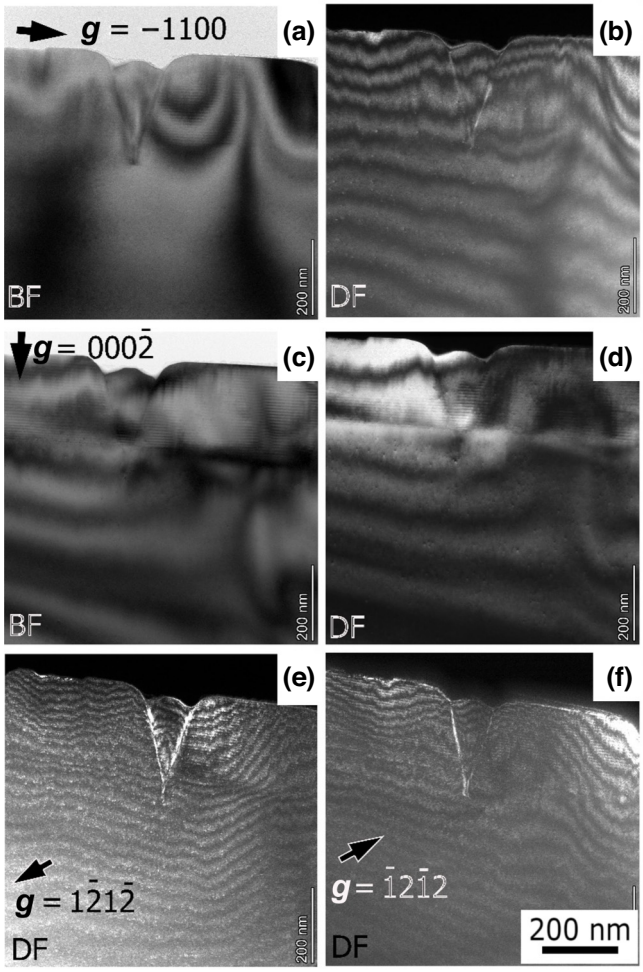

FIG. 4. (a),(b) Scattering-contrast TEM in bright-field (BF) and dark-field (DF) configurations, respectively, with an in-plane g vector. Only a faint contrast is observed in $\boldsymbol{g} = \bar{1}100$ diffraction conditions. (c) BF and (d) DF show scattering-contrast TEM with a zone axis g-vector. The dislocation is invisible in $\boldsymbol{g} = 000\bar{2}$ conditions showing only residual contrast. This analysis shows that the Burgers vector has an a-component and is a pure-edge type. (e) The narrow spacing of lower U-shape lines shown in $\boldsymbol{g} = 1\bar{2}1\bar{2}$ weak beam diffraction condition and (f) wider spacing shown in $\boldsymbol{g} = \bar{1}2\bar{1}2$ confirm that the dislocation is an a-type pure-edge half-loop.

Figure 7 shows the comparison between an SEM image [Fig. 7(a)] and a panchromatic CL image [Fig. 7(b)]. The primary conclusion from these images is that all the dark spots in Fig. 7(a) have corresponding dark spots in the CL image [Fig. 7(b)]. This means that all V-defects are nucleated on threads and there are few, if any, threads without a V-defect. The half-loops can be seen as small dark dots in Fig. 7(a) and pairs of brighter dots in Fig. 7(b). Since the V-defects, formed both from the substrate and half-loop TDs, remain unfilled, they appear partially brighter in the CL image in Fig. 7(b) due to increased light extraction from the V-defect sidewalls. The V-defect

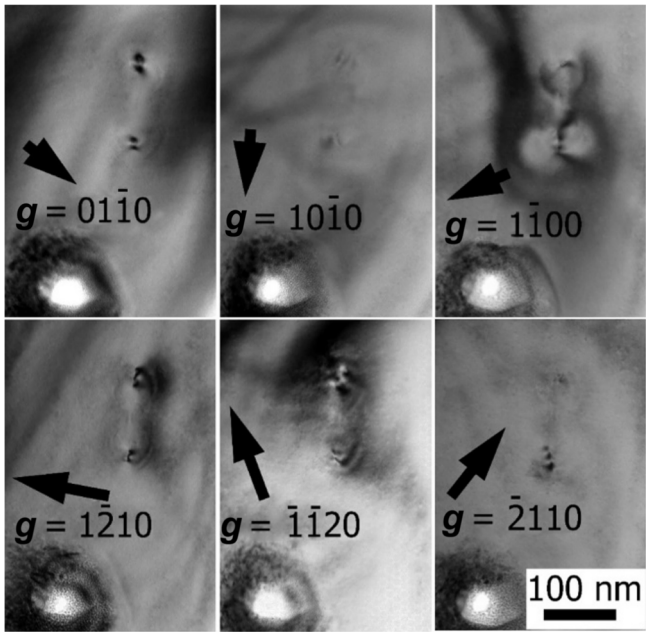

FIG. 5. Plane-view TEM with different diffraction conditions. A strong contrast is seen in all directions except when $\boldsymbol{g} = 10\bar{1}0$, or cases parallel to the a-plane and perpendicular to the a-direction.

density was $\sim 2 \times 10^8$ cm^{-2} and the half-loop density was $\sim 1 \times 10^8$ cm^{-2} for Sample A. Ongoing work in our group has shown that the half-loop density can be changed with growth conditions and will be the subject of a future publication.

Figure 8 shows a half-loop and large V-defect from Sample B. Figure 8(a) exhibits a lower magnification image where the half-loop V-defect can be compared with another large V-defect originating from a TD from the substrate. Figures 8(b) and 8(c) display how the surface depressions on either side of the half-loop turn into a single large V-defect. Figure 8(c) shows clear evidence that semipolar growth is occurring on the sides of this V-defect, closely resembling images of semipolar QWs in previous work [11,24]. Figure 8(d) shows high-resolution HAADF STEM images in the region of the half-loop formation. From both HAADF STEM imaging and scattering-contrast imaging, we were unable to determine the extended defect structure at the initiation site of the half-loop: this is a topic of ongoing investigation. Half-loop formation has been observed from basal plane stacking faults, so it is highly probable that Fig. 8(d) shows stacking faults with half-loop formation [36]. Compared with Sample A, the climblike geometry is less pronounced in Sample B, which likely assisted in opening a single large V-defect rather than two smaller ones, as was observed in Sample A. It is plausible that there were initially two small pits on each TD arm, but they merged into a single large V-defect. The only growth difference between samples A and B was the thickness and

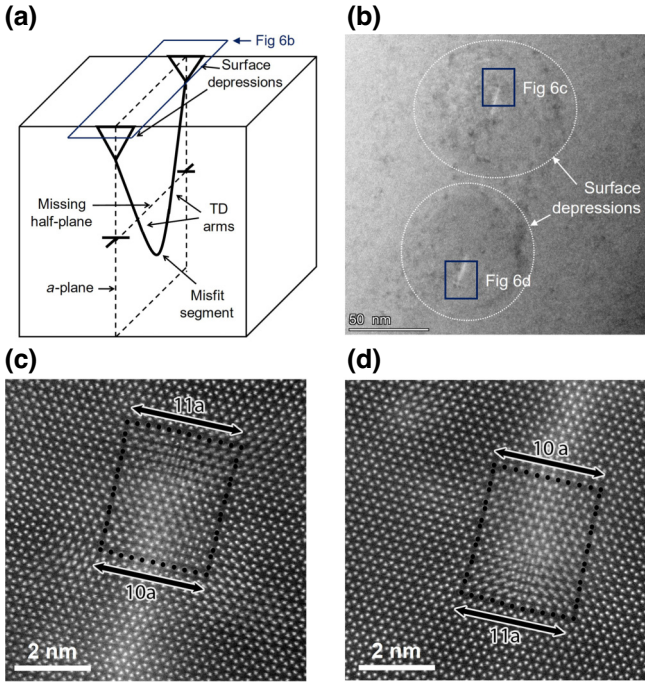

FIG. 6. (a) Schematic of half-loop formation and missing plane in a GaN film. (b) Plane-view of HAADF TEM image showing the two TD arms in the foil (bright contrast) and the surface depressions indicated with white circles and the top of the TD arms, which appear as white lines in TEM. The orientation of (b) with respect to the half-loop is indicated by the blue box of the schematic in (a). (c),(d) High-resolution HAADF TEM images of the top and bottom of the half-loop arm, respectively, as indicated by the boxes in (b). The orientation of (c) and (d) are indicated by the blue boxes in (b). The hexagonal structure of the GaN can be clearly seen. The missing plane of atoms is obvious by counting atomic spacings above and below the half-loop arms, which is indicated by the black dots and arrows.

growth temperature of the GaN spacer grown between the LT-GaN and the SL layers, with Sample A having a higher temperature and thicker layer.

This supports the hypothesis that the climblike behavior of TD arms is dependent on surface kinetics and adatom

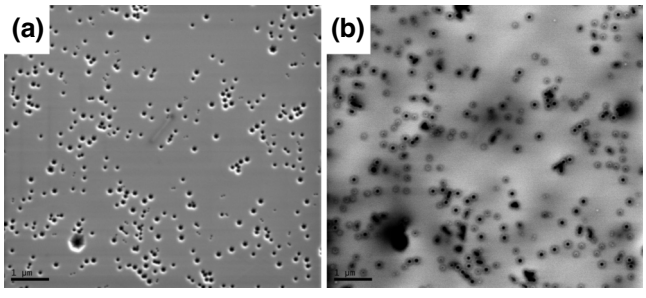

FIG. 7. (a) SEM and (b) panchromatic CL images of Sample A showing the large V-defect formation on ∼100% of existing threads and the new pure-edge half-loops that generate smaller depressions, which may turn into V-defects for lateral injection with the correct growth conditions.

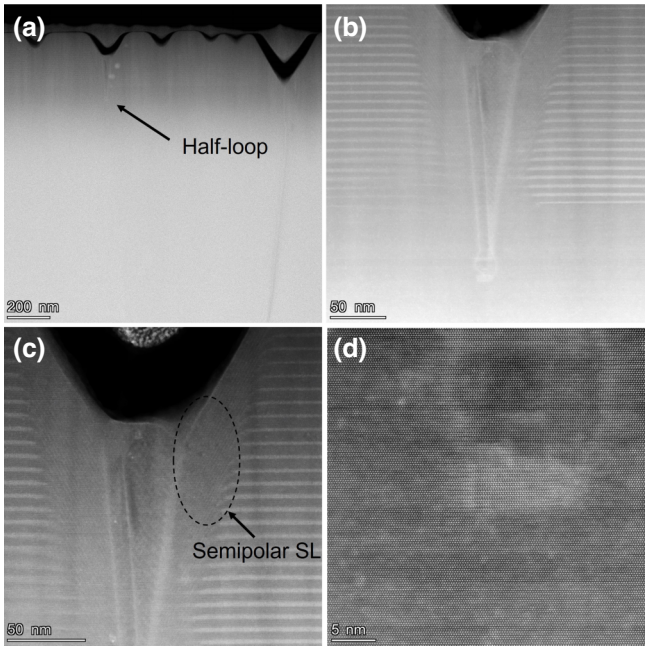

FIG. 8. (a) HAADF cross-sectional TEM image of a half-loop-type structure forming in an LT-GaN layer in Sample B. (b),(c) Close-ups of the half-loop and V-defect formation from the half-loop. From these images, it can be seen that rather than opening two V-defects, the surface depressions at each end of the half-loop combine to form a single large V-defect. From (c), we see clear evidence that the semipolar growth is occurring on the sidewalls of the V-defect, while (d) shows the extended defect structure of the initiation of the dislocation half-loop.

mobility. Based on previous work in our group [11], forming large V-defects before the active region is beneficial for lateral injection so, while Sample A provides a simpler case study for homoepitaxial half-loop formation in GaN, Sample B produces V-defects that are more likely to be favorable for lateral injection.

Figures 9(a) and 9(b) show bright-field (BF) and dark-field (DF) scattering-contrast images of the large V-defect generated half-loop in Sample B, respectively. Figures 9(c) and 9(d) display scattering-contrast TEM with $\boldsymbol{g} = 0002$ (zone axis) and $\boldsymbol{g} = \bar{1}100$, respectively, and show three large V-defects (labeled as 1, 2, and 3) forming in the LT-GaN layer. What is notable is that each V-defect in Figs. 9(c) and 9(d) form a different type of TD. V-defect 1 is the same large V-defect from Figs. 9(a) and 9(b) and forms on the half-loop. The residual contrast in the zone axis suggests these TD arms have no c-component to their Burger's vector and are, thus, a pure-edge type. V-defect 2 forms on a mixed component ($\boldsymbol{a}+\boldsymbol{c}$ Burgers vector) TD from the underlying GaN layer, as can be seen by the strong contrast under both diffraction conditions. V-defect 3 shows only residual contrast in the zone axis, which indicates that this is a pure-edge TD from the substrate. In both V-defects 2 and 3, the TD appears to end but this

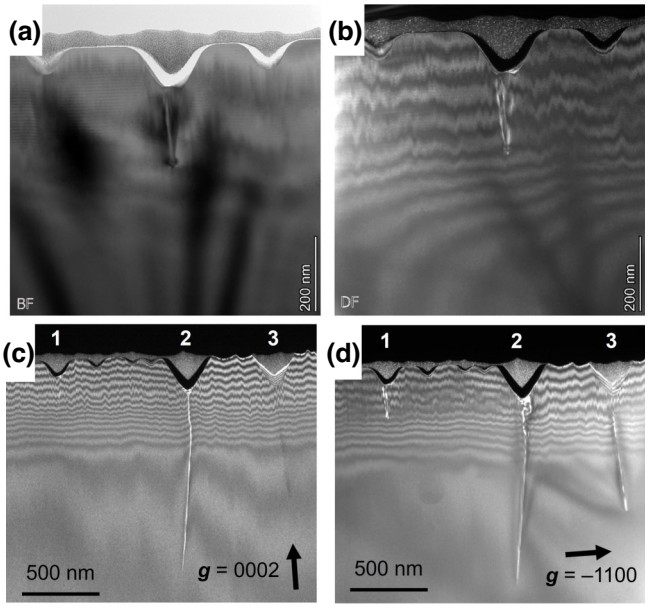

FIG. 9. (a) BF and (b) DF scattering-contrast TEM images of the large V-defect origination from a half-loop generated in LT-GaN. This V-defect will likely be beneficial for lateral injection in a full LED structure. (c),(d) DF scattering-contrast TEM images with three distinct types of large V-defects for lateral injection. V-defect 1 is generated from a pure-edge half-loop from the LT-GaN. V-defect 2 is created from a mixed (**a** + **c**)-type TD (shows contrast in both diffraction conditions) originating from the substrate, and V-defect 3 is formed on a pure-edge-type dislocation from the substrate.

is simply due to it extending out-of-the-plane of the TEM sample. These TDs are generated in the early 2D to 3D GaN growth. A V-defect formation on mixed-type TDs happens most readily and is the most widely studied in the literature. V-defects on mixed TDs are generally larger due to the larger surface depression that occurs when a mixed TD meets the GaN surface. Mixed TDs appear in higher frequency in GaN on Si compared with GaN on PSS or flat sapphire, which is one of the reasons for the success of V-defect LEDs in GaN on Si [6,7]. Few reports in the literature show clear evidence of V-defect formation on pure-edge TDs, so this is a significant result. For GaN growth on sapphire, most of the TDs are usually pure-edge type, so this result is especially important for the V-defect engineering of LED grown on sapphire. The important takeaway from Fig. 9 is that we have demonstrated the ability to form large V-defects on any type of TD, including those generated in the preparation layers. This provides a versatile toolbox for V-defect LED engineering on any substrate.

IV. DISCUSSION

V-defects can open on existing threading dislocations under conditions of kinetically limited growth. In these samples, the high growth rate combined with the reduced growth temperature, limits adatom diffusion into the surface depression at the top of the threading dislocations, which enhances the V-defect formation. Under these conditions of kinetically limited growth, the relative growth on different planes can be described by kinetic Wulff plots [42]. It is the varying growth rates between the *c*-plane and $\{10\bar{1}1\}$ that favor V-defect growth once nucleated.

The generation of new threads via low-temperature growth is less understood. As discussed in the introduction, recent work has shown the formation of pure-edge dislocations from overlapping I_1 BSFs where the new threads are generated from the geometry of the stacking fault boxes, bound by partial dislocations [38,39]. This hypothesis would explain why these form in low-temperature GaN with a rapid growth rate since low surface mobility favors I_1 BSF formation. It is important to note that BSFs should only form during island growth, not during step flow. However, it is possible to have local island growth if the terrace width becomes too wide. It is plausible that the low-temperature growth conditions are disrupting step-flow growth sufficiently enough to create small regions of island growth, which are responsible for BSF formation. This might also explain why the BSFs form in clusters and overlap to form more complex extended defects.

Due to the high disilane flow, there is a possibility of SiN nanomasking at threading dislocations and the creation of half-loop formation. There are reports of SiN nanomasks forming under high Si doping. [43]. While the traditional method for SiN nanomasking has shown a reduction in TDD via lateral overgrowth through pinholes in the SiN, it is possible that a partial SiN mask could create the type of growth perturbations needed to generate TDs [44]. It is notable, however, that SiN nanomasking usually occurs during growth interrupts where only NH_3 and disilane are flown. The half-loops in the samples in this work were generated during the continuous flow of TMG. In addition, no Si was observed in the STEM EDS at the half-loop nucleation site.

Half-loop formation during homoepitaxy has rarely been observed in GaN. There is increasing interest in the strategic use of V-defects for lateral injection of LEDs. Most of the early work on V-defect LEDs was undertaken on Si because of the relatively high threading dislocation density ($>1 \times 10^9$ cm^{-2}) compared with growth on PSS. Typical PSS has a TDD $<1 \times 10^8$ cm^{-2} and high TDD PSS rarely exceeds 3×10^8 cm^{-2}. Full device simulations of V-defect LEDs show the importance of achieving a high V-defect density in long-wavelength V-defect engineered LEDs [9]. Because the lateral carrier diffusion length is ~100 nm in GaN with alloy fluctuations, the V-defects need to be, on average, a few hundred nanometers apart in order to obtain lateral injection across an entire LED [45]. This requires V-defect densities of $\sim 1 \times 10^9$ cm^{-2}, which is achievable on (111)-Si and flat sapphire but is

difficult to achieve using the existing TDs on PSS. If the separation between V-defects is larger than the carrier diffusion length, only partial lateral injection can be achieved. The formation of half-loops and the subsequent nucleation of V-defects provides a promising pathway to create sufficiently high V-defect densities on PSS. In addition, the demonstration of V-defect formation on pure-edge dislocations (both from the substrate and generated in the LT-GaN layer) is critical for the V-defect engineering of LEDs grown on sapphire, where most of the TDs are the pure-edge type.

V. SUMMARY

In this work, we provide a rigorous analysis of homoepitaxial half-loop formation in low-temperature GaN layers. Analysis of the half-loops with BS SEM and plane-view TEM showed that they occur on *a*-planes. Scattering-contrast TEM showed that they have no *c*-component in their Burgers vector and are, thus, pure-edge-type dislocations. The half-loops consist of a U-shaped dislocation segment that bends upward to form two TD arms, which exhibit climblike behavior. Moreover, where the TD arms meet the surface, they form surface depressions that form a large V-defect under kinetically limited growth conditions. In addition, the low-temperature GaN layer used to nucleate V-defects was successful in nucleating ∼100% of existing TDs into large V-defects based on cathodoluminescence images. Previous papers have reported only mixed component TDs opening into V-defects, but here we demonstrate both mixed and edge TDs can undertake this opening. These results were confirmed through scattering-contrast TEM. The results of this paper are aimed at creating more favorable V-defect structures and densities on sapphire substrates to enable lateral carrier injection through V-defect engineering for light-emitting diodes.

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