

Fluxonium qubits in a flip-chip package


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The strong anharmonicity and high coherence times inherent to fluxonium superconducting circuits are beneficial for quantum information processing. In addition to requiring high-quality physical qubits, a quantum processor needs to be assembled in a manner that minimizes crosstalk and decoherence. In this paper, we report on fluxonium qubits packaged in a flip-chip architecture, where a classical control and readout chip is bump bonded to the quantum chip, forming a multichip module. The modular approach allows for improved connectivity between the qubits and control and readout elements, and separate fabrication processes. We characterize the coherence properties of the individual fluxonium qubits, demonstrate high-fidelity single-qubit gates with 6-ns microwave pulses (without DRAG), and identify the main decoherence mechanisms to improve on the reported results.

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I. INTRODUCTION

Superconducting circuits are one of the leading quantum computing platforms due to the orders-of-magnitude growth in coherence times [1,2] and a path to scalability derived from existing CMOS technologies [3]. To date, superconducting quantum processors composed of many tens of qubits have been demonstrated [4,5]. A fault-tolerant quantum computer capable of solving classically intractable problems would require millions of physical qubits [6]. This number can be lowered by improving the qubit performance. Nevertheless, the need for scaling up remains.

A major obstacle to scaling is the overhead related to routing the multitude of lines for qubit control and readout in a planar architecture. The main challenges arise from signal crosstalk between qubits and the conflicting requirement of coupling high- Q qubits to lossier control and readout circuitry. Additionally, we expect that alternative qubit control methods will be necessary to realize large-scale quantum processors, since the power consumption and physical overhead of conventional analog microwave control is daunting. One example is single flux quantum (SFQ) technology, where the qubits are controlled using

digital voltage pulses [7,8], which would greatly reduce the level of instrumentation overhead.

A way to scale up from the planar level is to utilize multiple circuit layers; separating the quantum and classical circuitry [9–11]. One approach is the flip-chip package, where a carrier chip responsible for qubit control and readout is bump bonded to the quantum chip (flip-chip), which is flipped such that it faces the carrier. The two chips are separated by vacuum or a chip interposer, and the qubit control lines and readout resonators couple capacitively or inductively to the qubit.

The modular approach allows classical and quantum elements to be fabricated separately, thereby protecting the qubits from unnecessary exposure to additional fabrication processes. It also improves device yield, since defective qubits do not affect the functionality of the carrier chip, and vice versa. Furthermore, instead of routing signals from the perimeter of the chip, interconnects can be made through its plane, reducing the overlap between individual circuit elements [12]. The flip-chip package is also optimal for digital qubit control using SFQ pulses because the quasiparticles [13,14] generated on the active carrier chip by the SFQ circuits are isolated from the quantum chip [15]. To date, flip-chip packaging has been explored on transmon [16] and capacitively shunted flux [17,18] qubits, demonstrating that the qubit performance is not limited by this architecture [19–23].

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Over the past decade, the fluxonium circuit [24] has emerged as a promising platform for superconducting quantum computing due to its extremely high coherence and strong anharmonicity [25,26]. The latter gives fluxonium a clear advantage over the transmon since the concern of state leakage errors [27] is mitigated when using arbitrarily short gates. Recent demonstrations of high-fidelity single- and two-qubit gates [28–33] have given way to exploring methods of scaling up fluxonium-based systems [34]. One such method that has not been experimentally realized is embedding fluxonium in a multichip module (MCM).

As an initial step, we present results on uncoupled fluxonium qubits embedded on a quantum chip (flip-chip), which is bump bonded to a carrier chip for control and readout. We demonstrate comparable qubit performance in this configuration to previous work on fluxoniums in 2D planar chips and 3D cavities [25,35]. Additionally, we characterize the leading sources of decoherence and the single-qubit gate fidelities in this device.

II. FLUXONIUM MULTICHIP MODULE

Our device consists of four uncoupled fluxonium circuits (labeled fluxoniums 1–4, see Fig. 1) fabricated on a silicon chip, which is bump bonded to the carrier chip with 5- μm spacing. The passive carrier chip houses corresponding microwave control lines, dc lines for flux biasing, and $\lambda/4$ coplanar waveguide (CPW) resonators [36] for readout. The fluxonium circuit design is the same as in Refs. [25,26], and can be further optimized for this packaging method. All four circuits contain 138 large-area Josephson junctions in their superinductance arrays. The spectrum of the fluxonium circuits is varied by changing the Josephson energy E_J . Fluxoniums 1 and 2 were designed to have about twice larger E_J than 3 and 4. We targeted a qubit frequency of at least 1 GHz at the half flux sweet spot ($\Phi_{\text{ext}}/\Phi_0 = 0.5$) in order to reduce the thermal population in the $|1\rangle$ state and for a shorter gate duration.

Images of the device are shown in Fig. 1. The capacitance between the two ends of the fluxonium, as well as to the readout resonator and control line, was

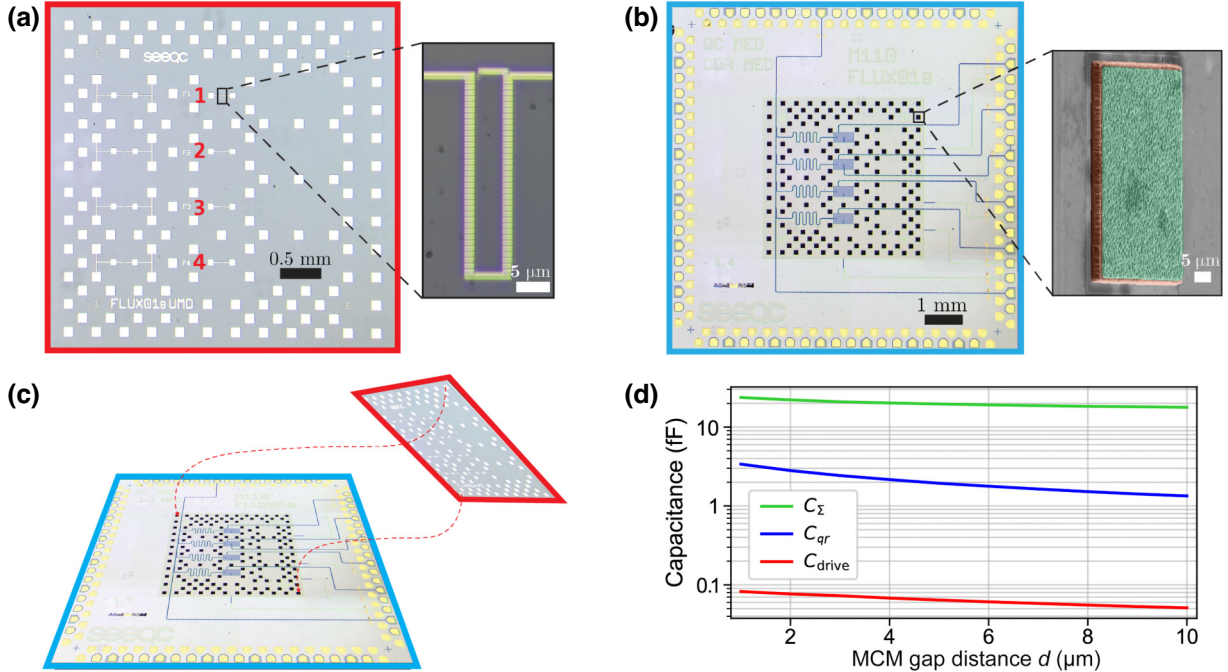


FIG. 1. (a) The $5 \times 5 \text{ mm}^2$ quantum chip (flip-chip), which houses four uncoupled fluxonium circuits with varying circuit parameters. The fluxoniums are labeled 1–4 (top to bottom). Aluminum pads are shown, which align with the 5- μm -high pillars on the carrier chip. Inset is a closeup of a fluxonium circuit. (b) The $10 \times 10 \text{ mm}^2$ carrier chip with classical circuitry for qubit control and readout. A single transmission line inductively couples to four $\lambda/4$ CPW resonators with fundamental frequencies in the 6–7 GHz range, which capacitively couple to each fluxonium for readout. Additionally, there are four qubit drive lines and four dc lines to flux bias the fluxonium loops. Inset is a false-color SEM image of one of the $120 \times 120 \mu\text{m}^2$ pillars. Orange (green) region is the 5(1) μm -thick aluminum (indium) layer. (c) Schematic of the configuration of flip-chip and carrier chip, which forms the multichip module. The flip-chip faces the carrier and the aluminum pads are aligned with the aluminum pillars on the carrier chip. The two chips are then bump bonded together to construct the MCM (see Appendix E). The pads on the carrier chip are wire bonded to a printed circuit board (PCB), which connects to the coaxial cables in the dilution refrigerator (see Appendix F). (d) Ansys Q3D simulation of total fluxonium shunt capacitance C_Σ , fluxonium-resonator coupling capacitance C_{qr} , and fluxonium-drive line coupling capacitance C_{drive} versus MCM gap distance d .

simulated with Ansys Q3D [see Fig. 1(d)]. Both ends of the fluxonium are ungrounded and the capacitance to the carrier ground plane contributes the majority of the fluxonium capacitance. To reduce this capacitance to meet our $E_C/h = 1$ GHz target, we removed the ground plane from a $300 \times 600 \mu\text{m}^2$ area of the carrier centered over the fluxonium. To account for the presence of the flip-chip on resonator frequencies, the CPWs that comprise the resonators were simulated with Sonnet [37].

The bare fluxonium Hamiltonian reads [24]

$$\hat{H}_{\text{fl}} = 4E_C \hat{n}^2 + \frac{1}{2} E_L \hat{\varphi}^2 - E_J \cos \left(\hat{\varphi} - 2\pi \frac{\Phi_{\text{ext}}}{\Phi_0} \right), \quad (1)$$

where the operators $\hat{n}, \hat{\varphi}$ represent the displacement charge across the capacitance in units of Cooper pairs and the superconducting phase across the inductance, respectively. They obey $[\hat{\varphi}, \hat{n}] = i$. Additionally, the resonator

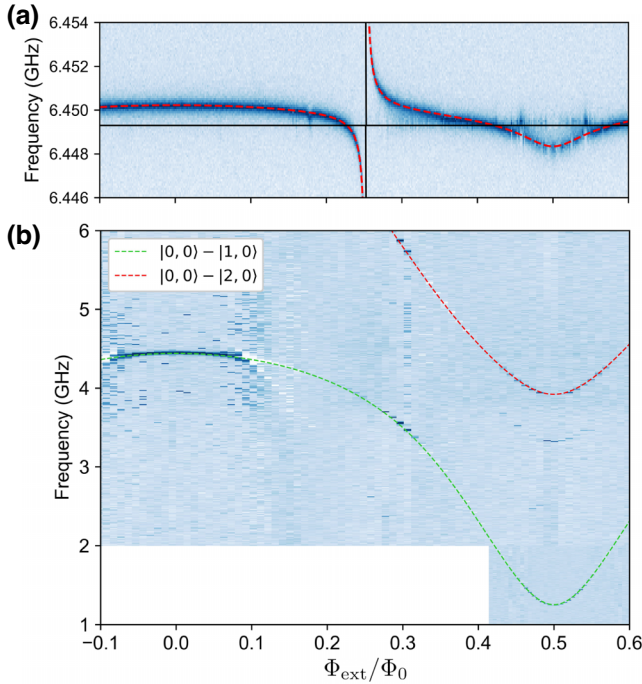


FIG. 2. Spectroscopy of fluxonium 3 over approximately half a flux period. State $|j, k\rangle$ indicates j excitations in the fluxonium circuit and k excitations in the resonator. (a) One-tone spectroscopy of the readout resonator showing the avoided level crossing between the bare fluxonium circuit state $|2, 0\rangle$ and the fundamental mode of the resonator $|0, 1\rangle$. Dashed red curves are the theoretical fit to the coupled fluxonium-resonator Hamiltonian, yielding $\omega_r = 2\pi \times 6.4493$ GHz and $g = 2\pi \times 86$ MHz. Horizontal and vertical solid black lines are the resonator and bare fluxonium $|0\rangle - |2\rangle$ transition, respectively, for $g = 0$. The level splitting between states $|2, 0\rangle$ and $|0, 1\rangle$ is given by $2g| \langle 2|\hat{n}|0\rangle | \approx 2\pi \times 31$ MHz. (b) Two-tone spectroscopy of the fluxonium circuit depicting the qubit ($|0, 0\rangle - |1, 0\rangle$) and ground to second excited state ($|0, 0\rangle - |2, 0\rangle$) transitions. Dashed curves represent the same fit as in (a).

TABLE I. Summary of relevant parameters for each fluxonium circuit under study at half flux quantum $\Phi_{\text{ext}}/\Phi_0 = 0.5$.

Fluxonium	3	4
E_J/h (GHz)	2.50	2.36
E_L/h (GHz)	1.14	1.14
E_C/h (GHz)	0.89	0.89
$\omega_{01}/2\pi$ (GHz)	1.252	1.330
ω_{12}/ω_{01}	2.14	1.99
T_1^{max} (μs)	77	58
$T_2^{E, \text{max}}$ (μs)	38	33
$\langle T_1 \rangle$ (μs)	55.1	33.6
$\langle T_2^E \rangle$ (μs)	27.5	23.2
T_ϕ (μs)	36.6	35.4
$\omega_r/2\pi$ (GHz)	6.4493	6.1391
$g/2\pi$ (MHz)	86	85
$\chi_{01}/2\pi$ (MHz)	1.39	0.63
$\kappa/2\pi$ (MHz)	0.391	0.269
$\tan \delta_C (\times 10^{-6})$	1.6	2.0
$n_{\text{th}} (\times 10^{-2})$	1.2	2.0

at frequency ω_r has the familiar Hamiltonian term: $\hat{H}_r = \hbar\omega_r(\hat{a}^\dagger\hat{a} + 1/2)$, and the Hamiltonian term for fluxonium-resonator coupling in the dispersive regime [38,39] is given by $\hat{H}_c = -\hbar g \hat{n}(\hat{a}^\dagger + \hat{a})$, where g is the fluxonium-resonator coupling rate. The spectroscopy data in Fig. 2 were fit to the numerical diagonalization of Hamiltonian: $\hat{H} = \hat{H}_{\text{fl}} + \hat{H}_r + \hat{H}_c$ in the LC oscillator basis.

We extensively characterized fluxoniums 3 and 4 since they met our 1-GHz qubit frequency target, and focus on fluxonium 3 in the main text. The parameters for both circuits are summarized in Table I. We began our analysis of fluxonium 3 with one- and two-tone spectroscopy of the resonator and fluxonium circuit [Figs. 2(a) and 2(b), respectively]. Dispersive readout of the qubit was performed using the corresponding resonator at frequency ω_r , capacitively coupled to the fluxonium circuit with empirically determined coupling rate $g = 2\pi \times 86$ MHz. The fit yields Josephson energy $E_J/h = 2.50$ GHz, inductive energy $E_L/h = 1.14$ GHz, and charging energy $E_C/h = 0.89$ GHz. The qubit transition frequency at the sweet spot is $\omega_{01} = 2\pi \times 1.252$ GHz. We used a Hilbert space of 25 fluxonium levels and five resonator levels in the fits.

The fitted values for E_C and g correspond to interchip distances d of 2.3 and 1.3 μm , respectively. The discrepancy between the two distances can be explained by the fact that we did not account for lateral chip offsets nor chip tilt in the simulation, and C_{qr} depends more strongly on these variables than C_Σ does. In general, a larger interchip distance will make the capacitances less sensitive to tilts, offsets, and variations in d itself.

III. QUBIT PERFORMANCE

We measured the energy relaxation time T_1 by applying a π pulse to the qubit and varying the readout delay.

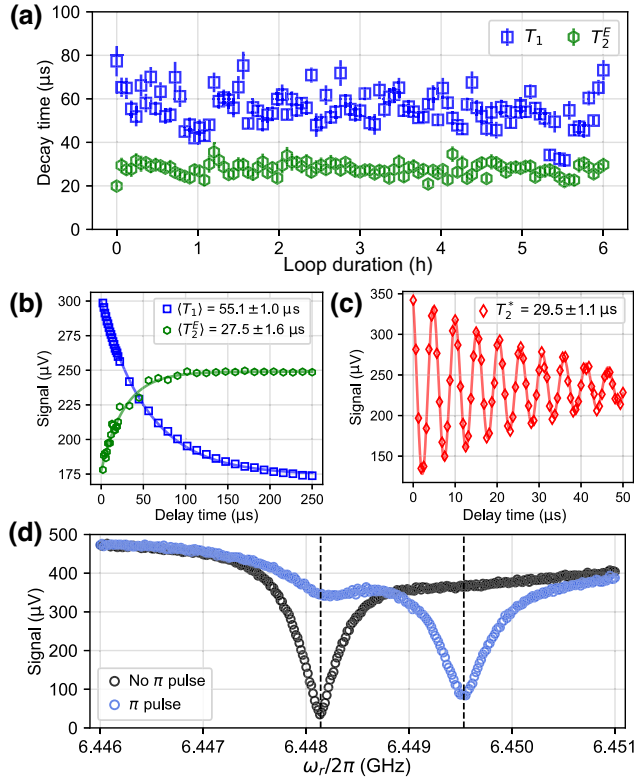


FIG. 3. Measurements of the fluxonium 3 qubit transition at $\Phi_{\text{ext}}/\Phi_0 = 0.5$. (a) Interleaved T_1 and T_2^E loop taken over 6 h. (b) T_1 and T_2^E signals averaged over all 101 measurements in loop, fitted to decaying exponentials. The fitted decay time constants are the mean relaxation time $\langle T_1 \rangle = 55.1 \pm 1.0 \mu\text{s}$ and Hahn-Echo coherence time $\langle T_2^E \rangle = 27.5 \pm 1.6 \mu\text{s}$. (c) A single Ramsey measurement fitted to an exponentially decaying cosine function, yielding $T_2^* = 29.5 \pm 1.1 \mu\text{s}$. (d) One-tone spectroscopy of the readout resonator with (light blue data) and without (black data) a π pulse applied to the qubit to flip the qubit state. Dashed vertical lines denote the center frequency of each fitted Lorentzian function. The difference of the two frequencies is the qubit dispersive shift $\chi_{01} = 2\pi \times 1.39 \text{ MHz}$.

At maximum, $T_1 = 77.3 \pm 7.0 \mu\text{s}$ [see Fig. 3(a)]. The effective dielectric loss tangent $\tan \delta_C$ of the total circuit capacitance $C_\Sigma = e^2/2E_C$ corresponding to this maximal T_1 at qubit frequency 1.252 GHz is approximately 1.6×10^{-6} . This value is similar to those reported in 3D fluxonium devices fabricated with the same materials and process [25], as well as in planar 2D architectures [35]. The effect of the MCM configuration on T_1 may vary, however, depending on the carrier ground plane geometry and the interchip distance. By optimizing the materials and fabrication process [26,40], a reduction in $\tan \delta_C$ by a factor of 2 is within reasonable expectation.

For calculating $\tan \delta_C$, it follows from Fermi's golden rule that the decay rate between eigenstates $|j\rangle$, $|k\rangle$ due to dielectric loss [41] in the capacitor at a finite temperature

T reads [25,35,42]

$$\Gamma_{jk}^{\text{diel}} = \frac{8E_C}{\hbar} |\hat{n}_{jk}|^2 \tan \delta_C \left[1 + \coth \left(\frac{\hbar\omega_{jk}}{2k_B T} \right) \right]. \quad (2)$$

Here, $\hat{n}_{jk} \equiv \langle j | \hat{n} | k \rangle$ is the fluxonium charge matrix element between states $|j\rangle$ and $|k\rangle$ in units of Cooper pairs. The loss tangent $\tan \delta_C$ is the inverse quality factor of the dielectric. We used Eq. (2) to calculate corresponding loss tangents for fluxoniums 3 and 4, given their maximal T_1 values at the sweet spot. We assume a qubit temperature of $T = 20 \text{ mK}$, the approximate base temperature of the dilution refrigerator. Note that due to $\omega_{01} > 1 \text{ GHz}$ in our experiments, the extracted $\tan \delta_C$ depends weakly on the temperature. For example, $T = 60 \text{ mK}$ would correspond to $\tan \delta_C = 1.0 \times 10^{-6}$. Since $\tan \delta_C$ can depend weakly on frequency, the reported values for fluxoniums 3 and 4 should be interpreted as the value at their qubit frequencies (see Table I).

The coherence time T_2 was measured via Ramsey and Hahn-Echo experiments. In the Ramsey method [43], two $\pi/2$ pulses are applied to the qubit, and the time delay between them is swept. Readout immediately follows the second $\pi/2$ pulse. This pulse sequence yields Ramsey fringes with an exponentially decaying envelope with decay constant T_2^* , the Ramsey coherence time. In the Hahn-Echo sequence [44], a π pulse is inserted between the two $\pi/2$ pulses. This refocusing π pulse reverses any phase accumulation due to low-frequency drifts during the first half of the sequence [45]. By increasing the number of refocusing π pulses, known as a Carr-Purcell-Meiboom-Gill (CPMG) sequence [46], the qubit will become more sensitive to noise at successively higher frequencies [47]. At maximum, we measured $T_2^* = 29.5 \pm 1.1 \mu\text{s}$ and Hahn-Echo coherence time $T_2^E = 36.3 \pm 4.0 \mu\text{s}$ [Figs. 3(a), 3(c)].

We performed an interleaved T_1 , T_2^E loop to obtain statistics on the relaxation and coherence times of fluxonium 3, and found $\langle T_1 \rangle = 55.1 \pm 1.0 \mu\text{s}$ and $\langle T_2^E \rangle = 27.5 \pm 1.6 \mu\text{s}$. $\langle T_2^E \rangle < \langle T_1 \rangle$ reveals significant pure dephasing of the qubit. We defined the dephasing time as $T_\phi = 1/(1/\langle T_2^E \rangle - 1/2\langle T_1 \rangle)$, yielding $T_\phi = 36.6 \pm 2.5 \mu\text{s}$. The exponentially decaying Hahn-Echo and Ramsey signals [Figs. 3(b) and 3(c), respectfully] rule out $1/f$ flux noise [48,49] as the predominant dephasing source. When we applied multiple refocusing pulses in a CPMG sequence, the measured decay time did not increase, indicating dephasing due to white noise (see Appendix B). It is therefore most likely that the pure dephasing of the qubit is caused by thermal photons in the resonator [50]. Based on the measured qubit dispersive shift χ_{01} and resonator linewidth κ [see Fig. 3(d) and Table I], $T_\phi = 36.6 \pm 2.5 \mu\text{s}$ corresponds to an average thermal photon number of $n_{\text{th}} = (1.2 \pm 0.1) \times 10^{-2}$ and an effective resonator temperature

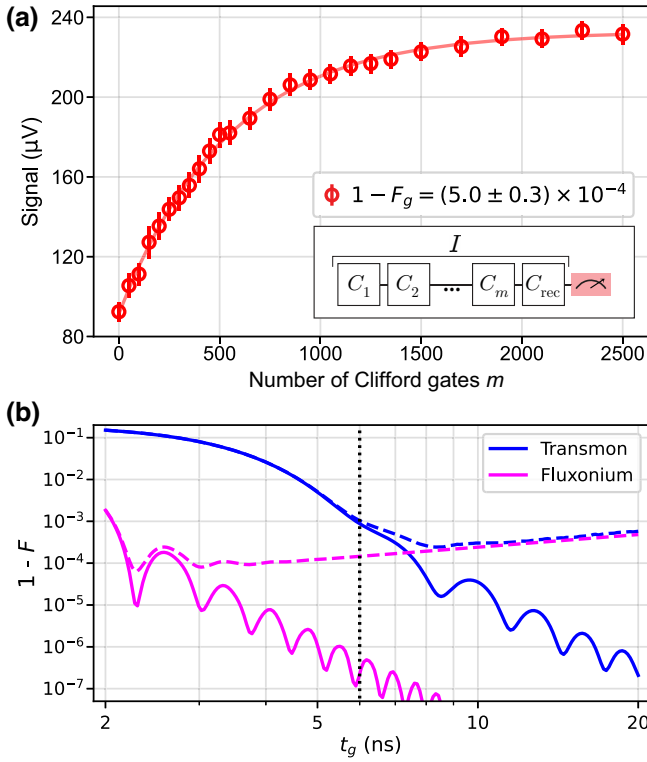


FIG. 4. (a) Single-qubit randomized benchmarking on fluxonium 3. The red data points are the result of averaging over 32 randomizations of the RB sequence. The fit yields an error rate per Clifford of $r_{\text{Cliff}} = (9.2 \pm 0.6) \times 10^{-4}$. (b) Simulated $X/2$ gate error rate $1 - F$ versus gate duration t_g for fluxonium 3 and a transmon (see main text) with (dashed curves) and without (solid curves) decoherence. When including decoherence, we used the measured T_1 and T_ϕ for fluxonium 3, given in Table I. Basic (no DRAG), cosine-envelope pulses were used in the simulation. The dashed black line corresponds to the gate duration (6 ns) used in our experiments.

of $T_{\text{res}} = 70 \pm 1$ mK (see Appendix A). Our measured values for n_{th} and T_{res} agree with those reported in transmon and flux qubits [51–53].

We completed our study of the fluxonium MCM by characterizing the single-qubit gates using randomized benchmarking (RB) [54,55]. The Clifford gates were generated by the gate set $\{I, X, Y, \pm X/2, \pm Y/2\}$; we defined the identity gate I as no pulse. An RB sequence is shown as an inset in Fig. 4(a). The physical pulses making up the $\pm X/2, \pm Y/2$ gates were cosine-envelope microwave pulses with total gate duration $t_g = 6$ ns. The X, Y gates were composed of two concatenated $X/2, Y/2$ gates.

Figure 4(a) shows the results of the RB experiment on fluxonium 3, along with the fit, which yields an average Clifford gate error rate of $r_{\text{Cliff}} = (9.2 \pm 0.6) \times 10^{-4}$ and an average gate error rate of $r_g = r_{\text{Cliff}}/1.833 = (5.0 \pm 0.3) \times 10^{-4}$. Given $T_2^E \approx 30$ μs , and the average Clifford gate duration of $t_g^{\text{Cliff}} = 13$ ns, we estimate the coherence

limit for the Clifford gate error rate to be $t_g^{\text{Cliff}}/T_2^E \approx 4.3 \times 10^{-4}$. Comparing this estimate to the measured r_{Cliff} , we conclude that at least half of our gate error can be attributed to imperfect calibration. Additional pulse optimization, such as DRAG [56], can help approach the coherence limit. More details on the microwave pulses and measurement of the individual gate error rates from interleaved RB [55] are found in Appendix C.

In Fig. 4(b), we simulated the gate error rate $1 - F$ versus total gate duration t_g of a $X/2$ gate for fluxonium 3 (anharmonicity $\alpha = 1.42$ GHz) and a transmon ($E_J/h = 15$ GHz, $E_C/h = 0.3$ GHz, $\alpha = -0.345$ GHz). The anharmonicity is defined as $\alpha = (\omega_{12} - \omega_{01})/2\pi$. The solid curves are the gate error rate with no decoherence in the system, where state leakage outside of the computational subspace is the dominant error source. The dashed curves include relaxation and dephasing using the measured T_1 and T_ϕ of fluxonium 3. Details of the simulation are provided in Appendix C.

For $t_g = 6$ ns in our experiments, the simulated coherence limit on the $X/2$ gate error rate is 1.5×10^{-4} . Given the measured $X/2$ error rate (see Table II) of 3.1×10^{-4} , we estimate that 48% of the gate error is due to decoherence. The discrepancy between the measured gate error rate and the coherence limit can be attributed to the 1 GSa/s sampling rate of the AWG. In the simulation, we assume a nearly continuous pulse envelope, while in practice this cannot be achieved as we approach $t_g = 1$ ns.

Crucially, Fig. 4(b) shows that it is impossible to reach the same gate error rates using basic (no DRAG) 6-ns microwave pulses on a typical transmon qubit, even without decoherence. Due to fluxonium’s higher anharmonicity, such a short gate time is accessible. Only at a gate duration of around 3 ns does the error rate become dominated by state leakage. Consequently, we could achieve a state-of-the-art gate fidelity in this device, despite a lower coherence time.

IV. CONCLUSION

In conclusion, we have packaged fluxonium qubits in a multichip module, and demonstrated performance on par with the previously cited experiments in 2D and 3D packages. An effective resonator temperature of 70 mK and average thermal photon number $n_{\text{th}} = 1.2 \times 10^{-2}$ is sufficient to explain the measured T_ϕ . By optimizing the readout line filtering and attenuation, along with reducing χ_{01}/κ , we expect the coherence time to approach the $2T_1$ limit.

Despite the high level of pure dephasing, a single-qubit gate fidelity greater than 0.999 was possible by using 6-ns pulses. A conservative goal of doubling the reported T_ϕ , without any improvement of T_1 , would push the coherence limit on the gate fidelity to above 0.9999. Fast gates, calibrated in a straightforward manner, are a

key advantage of fluxonium, where the anharmonicity is about an order of magnitude larger than in transmons. Our results on the first fluxonium MCM may be useful for scaling the next generation of fluxonium-based quantum processors.

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APPENDIX A: READOUT

1. Qubit-resonator interaction

Each fluxonium circuit is capacitively coupled to a $\lambda/4$ CPW resonator, which is housed on the carrier chip. The fluxonium-resonator coupling rate g was found empirically by fitting the spectroscopy data in Fig. 2. The pull on the resonator frequency due to bare fluxonium state $|j\rangle$, known as the dispersive shift of state $|j\rangle$, is given by [57]

$$\chi_j = g^2 \sum_k |\hat{n}_{jk}|^2 \frac{2\omega_{jk}}{\omega_{jk}^2 - \omega_r^2}. \quad (\text{A1})$$

The dispersive shift of the transition between states $|i\rangle$ and $|j\rangle$ is then $\chi_{ij} = \chi_i - \chi_j$. Crucially, Eq. (A1) shows that the qubit transition can have a large dispersive shift due to the contributions of the higher levels where $\omega_{jk} \simeq \omega_r$, despite the large detuning between ω_{01} and ω_r . Figure 5 uses Eq. (A1) to plot χ_{01} across half a flux period for fluxoniums 3 and 4. Red diamonds are measured χ_{01} at various external flux biases, showing excellent agreement between theory and experiment. The simulation uses 25 fluxonium levels, 20 of which are used in the summation to find χ_{01} .

In our system, the fluxonium-resonator coupling rate g in Eq. (A1) is given by

$$g = \frac{1}{2} \frac{C_{\text{qr}}}{C_{\Sigma} C_r} \frac{1}{\sqrt{\zeta_q \zeta_r}}, \quad (\text{A2})$$

where $\zeta_q = R_q/2\pi \sqrt{8E_C/(E_L + E_J)}$ and $\zeta_r = \sqrt{L_r/C_r}$ are the fluxonium and resonator characteristic impedances, respectively. $R_q = h/(2e)^2$ is the resistance quantum.

2. Thermal photon dephasing

The qubit dephasing rate due to thermal photons in the cavity is given by

$$\Gamma_{\phi}^{\text{th}} = \frac{n_{\text{th}} \kappa \chi_{01}^2}{\kappa^2 + \chi_{01}^2} \quad (\text{A3})$$

in the low photon number n_{th} limit [51,58]. Plugging in the values of κ , χ_{01} , and T_{ϕ} for each fluxonium (see

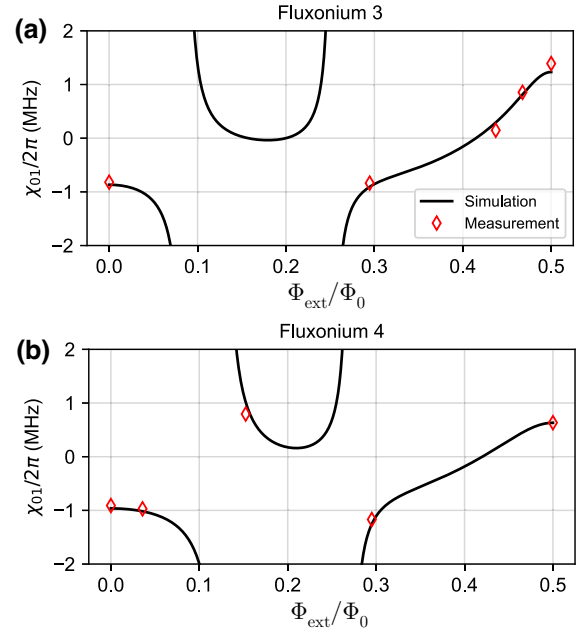


FIG. 5. Simulated qubit dispersive shift χ_{01} for fluxoniums 3 (a) and 4 (b) using Eq. (A1) and the parameters in Table I. We include measured values of χ_{01} at various external flux biases.

Table I), we find the average thermal photon numbers $n_{\text{th}} = (1.2 \pm 0.1) \times 10^{-2}$ and $(2.0 \pm 0.2) \times 10^{-2}$ for fluxoniums 3 and 4, respectively. These values correspond to resonator temperatures of 70 ± 1 mK and 75 ± 2 mK for fluxoniums 3 and 4, respectively.

APPENDIX B: COHERENCE ANALYSIS

1. $1/f$ flux noise

$1/f$ flux noise is known to be a leading cause of pure dephasing in flux-sensitive qubits, with a noise spectral density [45,48,49,53,59]:

$$S_{\Phi}(\omega) = 2\pi \frac{A_{\Phi}^2}{\omega}, \quad (\text{B1})$$

where A_{Φ} is the flux noise amplitude at 1 Hz. The dephasing rate due to first-order $1/f$ flux noise is given by

$$\Gamma_{\Phi} = A_{\Phi} \sqrt{\ln 2} \frac{\partial \omega}{\partial \Phi_{\text{ext}}}. \quad (\text{B2})$$

This leads to a T_2^E measurement signal decaying with a Gaussian envelope, with decay constant $T_{\phi}^{\Phi} = 1/\Gamma_{\Phi}$. This is the case when fluxonium is flux biased off of the sweet spot. On the sweet spot, the first-order sensitivity to $1/f$ flux noise vanishes, and we observe an exponentially decaying echo signal [25]. To determine A_{Φ} in our experimental setup, we measured T_2^E at various Φ_{ext} in fluxonium 3 (see Fig. 6). The observed dependence of T_2^E versus

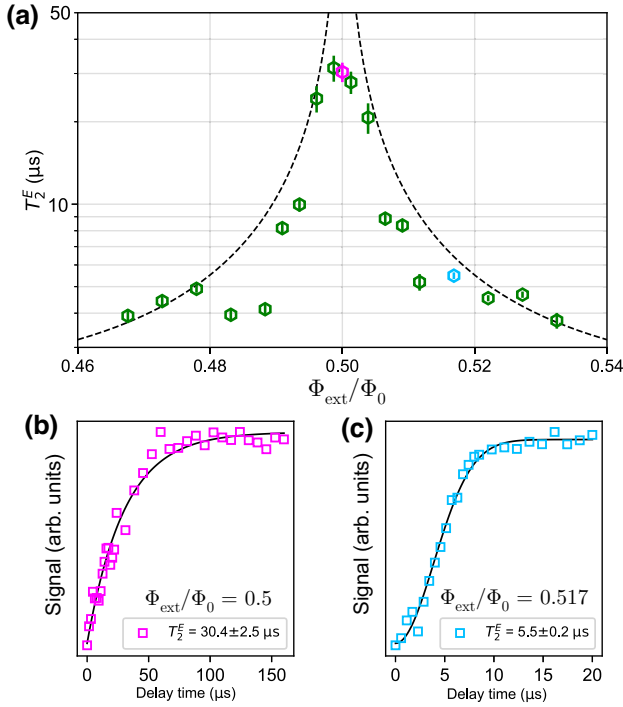


FIG. 6. (a) T_2^E versus external magnetic flux Φ_{ext} . The data are fit to a decaying Gaussian function off sweet spot and to a decaying exponential at the sweet spot. Dashed black curve represents the simulated values for first-order flux noise-induced dephasing time $T_\phi^\Phi = 1/\Gamma_\Phi$ for flux noise amplitude $A_\Phi = 5.5 \mu\Phi_0/\sqrt{\text{Hz}}$ at 1 Hz. At the sweet spot, the first-order limit diverges, and coherence is mainly limited by energy relaxation and uncorrelated (white) noise. (b) Measurement trace at the sweet spot. The data are fit to a decaying exponential and the decay constant corresponds to the magenta point in (a). (c) Measurement trace at a flux bias point off the sweet spot. The data are fit to a decaying Gaussian and the decay constant corresponds to the blue point in (a).

external flux bias corresponds to $A_\Phi = 5.5 \mu\Phi_0/\sqrt{\text{Hz}}$, which is similar to the previously cited work.

2. CPMG

By increasing the number of refocusing π pulses N in a Hahn-Echo sequence (where $N = 1$), the qubit will be more sensitive to noise at successively higher frequencies [45,60]. This is known as a Carr-Purcell-Meiboom-Gill (CPMG) sequence [46], where the additional refocusing π pulses act as a bandpass filter centered at a frequency determined by N and the free evolution time [47,53]. If the noise spectrum is white within the region we sweep our filter, we expect the measured decay time to remain constant with an increasing number of π pulses. If the noise spectral density $\propto 1/f$, we expect T_2 to rise for $N > 1$. Given the results of our CPMG experiment shown in Fig. 7, we concluded that thermal resonator photons are the main dephasing source at the sweet spot.

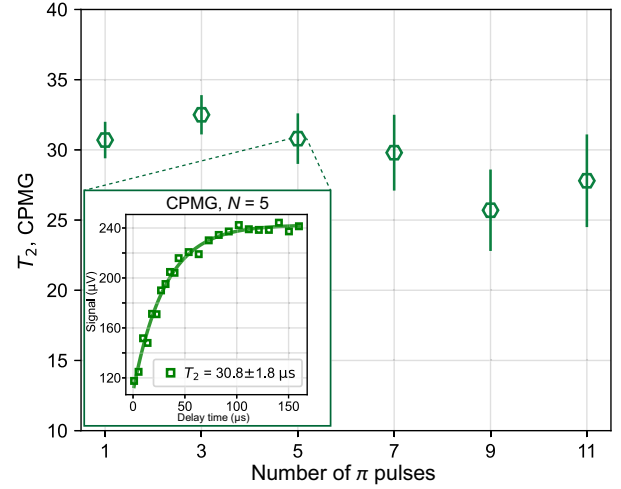


FIG. 7. CPMG experiment on fluxonium 3 where we sweep the number of refocusing π pulses N from 1 to 11. The resulting measurement traces are then fitted to a decaying exponential function and the decay constant is plotted. We find that there is no significant correlation between the number of pulses and T_2 in this range. Inset shows the measurement trace and fit for five intermediate π pulses.

APPENDIX C: SINGLE-QUBIT GATES

1. Microwave pulses

The $X/2$ and $Y/2$ pulses were synthesized with a Keysight M3202 AWG and a Rohde & Schwarz SGS100A Vector Modulation rf source for low-frequency IQ modulation. We used cosine-envelope pulses with an envelope function:

$$f(t) = \frac{\epsilon}{2}[1 - \cos(2\pi t/t_g)], \quad (\text{C1})$$

where ϵ is the drive amplitude and t_g is the total gate duration. We set $t_g = 6$ ns in our experiments. The cosine envelope is chosen over Gaussian to avoid truncation at the edges. The X (Y) pulses consist of pairs of concatenated $X/2$ ($Y/2$) pulses. We tuned the qubit drive frequency ω_d by taking Ramsey measurements with varying ω_d . After obtaining the $\omega_d = \omega_{01}$, we performed a pulse train measurement to determine the optimal pulse amplitude. The pulse train consisted of sweeping the amplitude for a train of 4, 16, 36, 64, 100, and 144 pulses. The resulting trace of each measurement is effectively a Rabi oscillation, where the Rabi frequency increases with the number of pulses in the train. The amplitude corresponding to the same phase in the Rabi oscillations across all the trains is the optimal pulse amplitude. After performing initial randomized benchmarking experiments, the pulse amplitude was further fine tuned using the ORBIT procedure [61].

2. Single-qubit randomized benchmarking

We benchmarked the single-qubit gates in fluxoniums 3 and 4 using randomized benchmarking (RB) [54]. In the RB sequence, m randomly chosen Clifford gates are applied to the qubit before applying a single recovery gate, such that the entire sequence is tantamount to an identity operation. In practice, due to decoherence and suboptimal pulse parameters, the RB signal decays with the number of Clifford gates in the sequence m as

$$A + Bp^m, \quad (\text{C2})$$

where p is the depolarization parameter, and A, B are constants. We extract p by fitting the measured RB signal to Eq. (C2) (see Fig. 4). The average error rate of a single-qubit Clifford operation r_{Cliff} is then given by

$$r_{\text{Cliff}} = (1 - p)/2. \quad (\text{C3})$$

Since each Clifford operation is composed on average of 1.833 physical gates (we do not count the identity gate), the average physical gate fidelity is

$$F = 1 - r_{\text{Cliff}}/1.833. \quad (\text{C4})$$

We estimated the lower limit on the gate error rate by taking t_g/T_2^E .

To determine the individual gate fidelities we performed interleaved randomized benchmarking [55]. The error rates of each gate, $1 - F_g$, are given in Table II. In the interleaved RB sequence, a given gate is interleaved between each Clifford operation. The resulting curve follows the same decay profile as the standard RB, but with a depolarization parameter p_g . The gate error is then given by

$$r_g = (1 - p_g/p)/2 = 1 - F_g, \quad (\text{C5})$$

where p is the depolarization parameter obtained from the initial RB and F_g is the fidelity of the interleaved gate.

3. Gate simulation

The simulation results shown in Fig. 4(b) were obtained as follows. We truncated the fluxonium and transmon Hamiltonians to consider only the five lowest energy eigenstates. We then define a pulse with driving frequency $\omega_d = \omega_{01}$, and envelope given by Eq. (C1), and compute the evolution operator U governing the time dynamics of

TABLE II. Gate error rates $1 - F_g$ of each Clifford-generating gate obtained from interleaved RB for fluxonium 3. The relative error of each error rate is approximately 10%.

Gate	X	X/2	-X/2	Y	Y/2	-Y/2
$1 - F_g (\times 10^{-4})$	8.1	3.1	2.6	6.1	2.1	5.9

the circuit when the pulse is applied. Sweeping the gate time t_g , we optimize the amplitude ϵ and drive frequency ω_d of the pulse using sequential least-squares programming to minimize the gate error rate $1 - F$, where the gate fidelity F is defined as [62]

$$F = \frac{1}{6} [\text{Tr}(U^\dagger U) + |\text{Tr}(U^\dagger U_{\text{ideal}})|^2], \quad (\text{C6})$$

where $U_{\text{ideal}} = R_X(\pi/2)$, or a $X/2$ gate. Note that U is nonunitary due to driving of higher energy circuit transitions.

To simulate the gate error with decoherence, we used the Lindblad master equation to model the evolution of the density matrix ρ with the optimal pulse parameters obtained from the simulation without decoherence. We included two collapse operators representing relaxation from qubit excited to ground state, and pure dephasing between the qubit states, following the procedure presented in Ref. [63].

APPENDIX D: FLUX BIAS CROSSTALK

We performed resonator spectroscopy on both fluxoniums 3 and 4 while tuning their respective external flux biases. We constructed a flux crosstalk matrix (Fig. 8) to quantify the mutual inductance between the flux bias line of fluxonium 3 and fluxonium 4's superinductance loop, and vice versa. The mutual inductance between the fluxonium circuit loop and flux bias line for fluxoniums 3 and 4 is 2.27 and 2.23 mA/ Φ_0 , respectively. This is determined using the diagonal elements of the flux crosstalk matrix. The mutual inductance between fluxonium 4 and fluxonium 3's bias line is 430 mA/ Φ_0 . Fluxonium 3's resonator frequency did not shift over the current range of fluxonium 4's bias line, therefore this mutual inductance is negligible.

APPENDIX E: FABRICATION

1. Quantum chip

We fabricated the device on a high resistivity silicon substrate. *Cleaning*: The chip is prepared by sonicating it in acetone, then isopropyl alcohol (IPA) for 3 min each. *Electron Beam Resist Application*: 1 drop of MMA EL-13 electron beam resist is applied to the chip, then spun at 5000 rpm for 1 min. The resist is then baked on a hotplate for 1 min at 180°C. A second layer of resist is then applied: 1 drop of 950 PMMA A3 electron beam resist spun at 4000 rpm for 1 min before baking at 180°C for 30 min. *Electron Beam Lithography*: The circuit is written with a 100 kV Elionix Electron Beam Lithography system, using a beam current of 1 nA. *Resist Development*: Mask is developed for 2 min in a 3:1 IPA:DI solution at 6°C. The chip is lightly shaken back and forth by hand at around 1–2 Hz while in the developer. *Metal Deposition*: Chip is loaded into a Plassys deposition system and the loadlock is

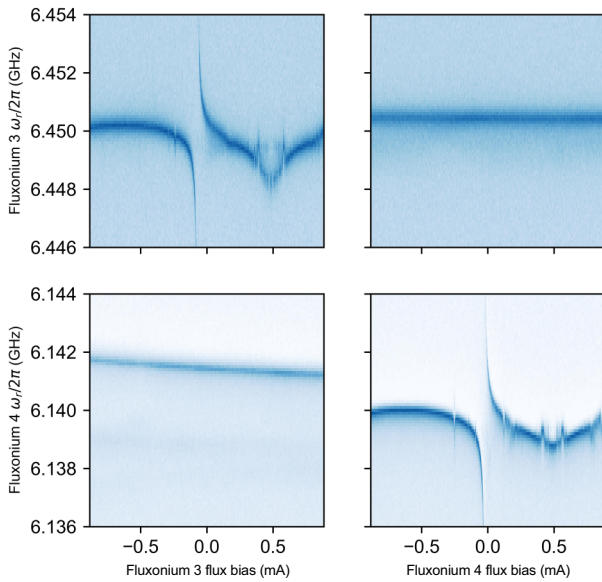


FIG. 8. Flux crosstalk matrix between fluxoniums 3 and 4. Spectroscopy of fluxoniums 3 and 4 resonators is performed while sweeping the current applied to each bias line on the carrier chip.

pumped on for 20 h until the pressure reaches 1.3×10^{-7} mBar prior to deposition. The deposition is comprised of the following steps: (1) 20 s Ar etch at each deposition angle ($\pm 23.83^\circ$). (2) Deposit Ti into the chamber at 0.1 nm/s for 2 min. (3) First Al deposition: 20 nm is deposited at 1 nm/s at an angle of 23.83° . (4) 10 min of oxidation at 100 mBar. (5) Second Al deposition: 40 nm is deposited at 1 nm/s at an angle of -23.83° . (6) 20 min of oxidation at 10 mBar (capping). *Resist Liftoff*: Chip is bathed in acetone for 3 h at 60°C . Then it is sonicated in the acetone for 5 s, followed by 10 s of sonication in IPA. Finally, chip is blown dry with N_2 .

2. Carrier chip

The process is based on SEEQC's two-niobium-superconducting-layer recipe for quantum applications [64]. The process involves substrate preparation, niobium (Nb) sputtering, plasma-enhanced chemical vapor deposition (PECVD) of $\text{SiO}_2/\text{SiN}_x$, chemical mechanical polishing (CMP), photolithography, and dry etching. The substrate is a high resistivity 6-inch (150 mm) silicon wafer.

It is first cleaned by spin scrubbing with acetone and spin rinse drying with IPA. Then the native oxide on the wafer is removed by BOE prior to loading into the deposition chamber. Once the chamber reaches a base pressure of 1.3×10^{-7} mBar, Nb is deposited by dc sputtering with target thickness 200 nm. The coplanar microstrip lines, feedthroughs, resonators, and qubit control lines are then patterned in this layer. All the patterning for this process

is done using a maskless laser writer capable of resolving 600-nm features with an *i*-line resist process. Then the Nb is inductively coupled plasma (ICP) etched in chlorine chemistry optimized for good selectivity to silicon. Moreover, an endpoint detection was implemented to minimize the overetch into the substrate and to keep the overetch to within 10 nm. Next, the resist is stripped in an acetone sonicating bath, followed by 600 nm of low-loss PECVD SiN_x deposited with CMP to planarize the layer. The wafer is then coated with PECVD SiO_2 of thickness 150 nm for an interlayer dielectric. The vias to the bottom Nb layer are then patterned and dry etched, which opens access to the wiring, grounds, bump, and contact pad connections. Then a second Nb layer of thickness 300 nm is deposited, followed by patterning of the wiring, ground straps, and contacts. The Nb is then dry etched in reactive ion etcher (RIE); at this step the exposed dielectric is completely dry etched from the wafer to minimize the dielectric participation ratio. After this step, there is only dielectric remaining under the wiring and ground straps. Next, the contact pads are patterned: trilayer Mo/Pd/Au of thickness 40/100/200 nm is deposited and lifted off. Finally, the bump layer is patterned: Al/In of thickness $5 \mu\text{m}/1 \mu\text{m}$ is deposited and lifted off. The carrier chips of size $10 \times 10 \text{ mm}^2$ are then diced out and ready for flip-chip bonding.

3. Multichip module

The multichip module was assembled using a Karl Suss/Microtec FC 150 Flip-Chip Bonder. The tool holds the chip and carrier on two vacuum chucks while adjusting the relative position of alignment marks viewed through a two-objective microscope assembly. The bonder was calibrated immediately before MCM assembly, such that the lateral misalignment between chip and carrier is within $1 \mu\text{m}$. The chip and carrier are aligned parallel to within $25 \mu\text{rad}$, as specified by the tool.

The MCM was assembled by a cold-compression process with a force of 294 N/mm^2 , held constant for 2 min. Distributed over the 152 square bumps, each $120 \mu\text{m}$ wide (8.8% of the total flip-chip area), this force is equivalent to 197 g per bump. Postbond measurement of bump height on other MCMs has indicated that this force compresses the top μm layer of indium, but does not significantly compress the underlying aluminum bump, such that the aluminum acts as a hard stop to control interchip spacing. After bonding, a small amount of low-temperature microelectronic-compatible epoxy was applied to the corners of the chip, away from critical circuit components, to maintain integrity of the MCM during sample handling and installation.

APPENDIX F: EXPERIMENTAL SETUP

The experiment was performed in a BlueFors LD400 dilution refrigerator (DR) at a base temperature of

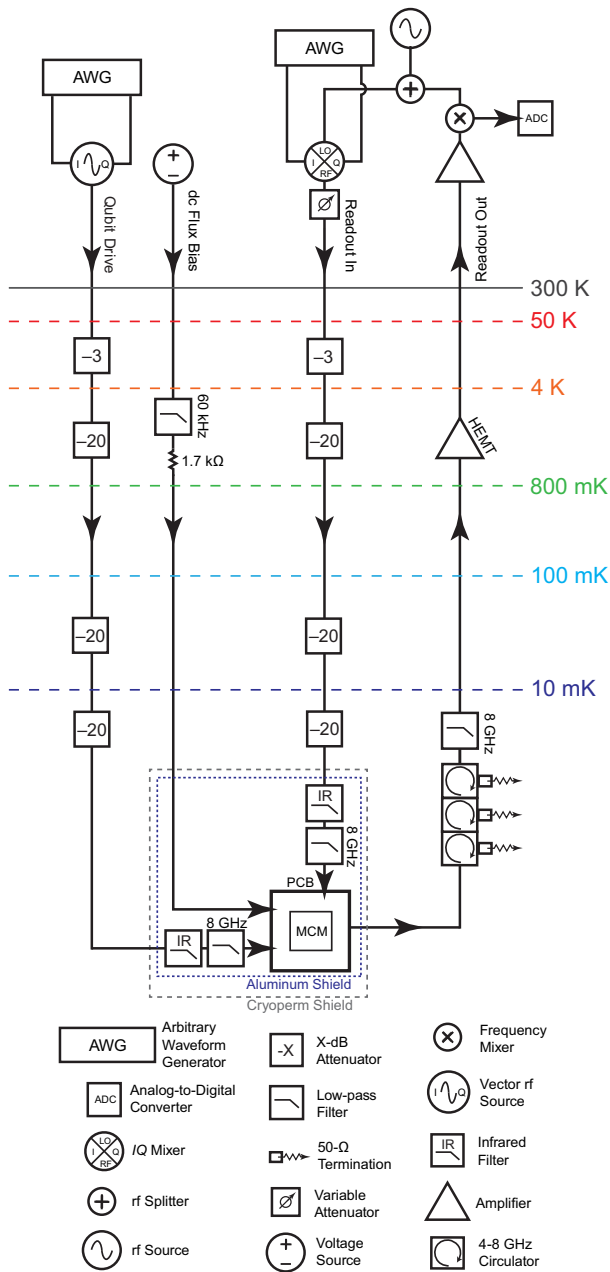


FIG. 9. Schematic of the wiring in the DR and room-temperature setup. The qubit drive and readout input lines are heavily attenuated and filtered using 63 dB of commercial attenuation (BlueFors cryogenic attenuators), along with K&L low-pass filters and infrared filters (manufactured by BlueFors). The dc flux bias line consists of a twisted pair, the positive terminal set by a voltage source and the negative terminal connected to the common ground plane of the chip. Each component in the figure is thermally anchored to the stage directly above it.

10–20 mK. The driving and readout lines were attenuated and filtered as depicted in Fig. 9. The MCM was mounted and wire bonded to a printed circuit board (PCB), which in turn was housed in a copper package. This package was bolted to a cold finger extending from the 10-mK stage of

the DR. The device package was encased in a superconducting (aluminum) shield as well as a cryoperm shield. Additionally, we used a magnetic shield inside the outer vacuum can of the refrigerator.

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