Layer-dependent switching and photodetection in two-dimensional InSe transistors

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The two-dimensional layered material-based multifunctional transistors are expected to be core devices in the post-Moore era. However, the relationship between layer thickness and device performance remains unclear. Here, we design the layer InSe transistors integrating switching and photodetection functions, exhibiting the fast-switching time and high responsivity when choosing the layer numbers of 2 and 3. Additionally, the maximum photoresponsivity and external quantum efficiency reach up to 0.29 A/W and 136.4% at the wavelength of 310 nm, respectively. The layer-number changing also induces 2 orders of magnitude improvement in and delay time. The dependence between layer number and device performance can provide a basis for designing multifunctional devices.

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I. INTRODUCTION

Atomic thick two-dimensional (2D) layered materials have emerged as an attractive candidate for future electronic and optoelectronic devices with ultrahigh integration multifunction density [1–7]. The unique physical and chemical properties can be suitable to improve the performance of the devices, thus continuing Moore's law [8–13]. For example, Desai *et al*. demonstrate a transistor with a gate length of 1-nm MoS_2, and the device displays subthreshold swing of approximately 65 mV/dec and an ON:OFF current ratio of approximately 10^6 [14]. Using the side-wall MoS_2 as the gate, Ren *et al.* scales down the gate length of transistors to 0.34 nm [15].

With the maturity of single-function devices, except shrinking the characteristic size of the device, increasing the functionalities of one single device is also another effective method. Therefore, it is necessary to explore atomic thick 2D van der Waals (vdW) semiconductor-based multifunction device [16–19]. For example, Syed *et al*. introduced a type-II vdW heterojunction-based optomemristive neuron, realizing combine and broadcast both excitory and inhibitory signals using one device [20]. The $MoSe_2$-WSe_2 electrical diodes implement the functions of ON:OFF ratio and thermal conductivity up to 10^4 and approximately 30 W/(m K), respectively [21]. Pan *et al*. fabricated double-gate field-effect transistor (FET) device, which can realize three types of circuits by modulation of charge carrier in the 2D channel [22]. Of note, due to the quantum confinement in atomic scale and the presence of interlayer coupling in multilayer, the physical properties of 2D materials strongly depend on layer number [23–25]. For instance, the electronic band structures, dielectric constant, and the refractive index of transition-metal dichalcogenides in the 2H phase present strong thickness dependence [26,27]. Moreover, modulating the layer number of 2D materials can affect the performance of the device. The Schottky-barrier heights for WS_2 contact with Au/Cr are reduced from 0.37 eV for a monolayer to 0.17 eV for 28 layers [28]. The result displays that it is necessary to consider the quantum confinement in 2D materials when constructing the multifunctional devices. However, the relationship of the layer number and device performance is unclear. Due to the high mobility and photoresponsivity, as well as the band gap regulated by the quantum confinement effect, we select InSe as an example for designing transistors and exploring transport properties.

Here, we systematically explore the dependent relationship of layer number and performance of multifunction transistors. The results reveal that the proper layer number can present excellent electronic and optoelectronic performance. For the photodetector, photocurrent density becomes larger and photocurrent spectra widen gradually

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by modulating the layer number. Meanwhile, the transconductance and subthreshold swing are also strongly layer dependent. The ON-state current (I_{on}) for monolayer devices with single and double gate satisfy the International Technology Roadmap for Semiconductors (ITRS) HP standard requirement. These results display the potential for layer-dependent electronic and optical of InSe transistors, opening the door for constructing multifunctional devices with the electronic properties of 2D materials.

II. METHODS AND COMPUTATIONAL DETAILS

The Vienna *ab initio* simulation package based on density-functional theory (DFT) carries out the electronic band structures [29,30]. The exchange-correlation functional is treated within the generalized gradient approximation and parameterized using the Perdew-Burke-Ernzerhof formula. The plane-wave cutoff and energy convergence tolerances are set to 500 and 10^{-5} eV, respectively [31]. Furthermore, a $13 \times 13 \times 1$ k-point mesh is used to sample the Brillouin zone. We choose a vacuum spacing of at least 20 Å to eliminate the interaction caused by periodic repetition [32]. In additional, we calculate the frequency-dependent dielectric function [$\varepsilon(\omega)$] to investigate the optical absorption properties. The optical absorption coefficient $\alpha(\omega)$ uses the formula

$$\alpha(\omega) = \sqrt{2\omega}\left[\sqrt{\varepsilon_1^2(\omega) + \varepsilon_2^2(\omega)} - \varepsilon_1(\omega)\right]^{1/2},$$

where $\varepsilon_1(\omega)$ and $\varepsilon_2(\omega)$ are the real part and imaginary part of the complex dielectric function, respectively.

The transport properties are calculated via DFT with nonequilibrium Green's function method at the generalized gradient approximation level using the Quantum ATK 2021 package [33,34]. The basis set of norm-conserving Pseudo Dojo pseudopotentials is used [35]. The k-point meshes of $1 \times 31 \times 151$ and cutoff energy of 110 hartree are set [36]. Figure S1 (see the Supplemental Material [37]) presents the k-point convergence test results.

The electrical current is calculated through the Landauer-Büttiker formula [38],

$$I(V_{DS}, V_G) = \frac{e}{h}\int_{-\infty}^{+\infty}\{T(E, V_{DS}, V_G)[f_D(E-\mu_D) - f_S(E-\mu_S)]\}\mathrm{d}E,$$

where T (E, V_{DS}, V_G) is the transmission coefficient at a given gate voltage V_G and bias voltage V_{DS}, f_{S-D} are the Fermi-Dirac distribution functions of the source-drain electrodes, μ_{S-D} are the electrochemical potentials of the source-drain electrodes.

And, the photocurrent spectrum is described by [39]

$$I_\alpha = \frac{e}{h}\int_{-\infty}^{+\infty}\sum_{\beta=D,S}[1-f_\alpha(E)]f_\beta(E-\hbar\omega)T^-_{\alpha,\beta}(E) - f_\alpha(E)[1-f_\beta(E+\hbar\omega)]T^+_{\alpha,\beta}(E)\mathrm{d}E,$$

$$T^-_{\alpha,\beta}(E) = NTr\{M^\dagger\tilde{A}_\alpha(E)MA_\beta(E-\hbar\omega)\},$$
$$T^+_{\alpha,\beta}(E) = NTr\{M\tilde{A}_\alpha(E)M^\dagger A_\beta(E+\hbar\omega)\},$$

where N is the number of photons, E is electron energy, h is Planck constant, $\hbar$ is reduced Planck constant, α and β labels the source and drain, A_α is the spectral function of lead α, $\tilde{A}_\alpha$ is the time-reversed spectral function of lead, M is the electron-photon coupling matrix, and ω is photon frequency.

$$M_{ml} = \frac{\mathbf{e}}{m_0}\left(\frac{\hbar\sqrt{\tilde{\mu}_r\tilde{\varepsilon}_r}}{2N\omega\tilde{\varepsilon}c}\right)^{1/2}\mathbf{e}\cdot\mathbf{P}_{ml}.$$

The total photocurrent is then calculated as $I_{ph}=I_S-I_D$. The retarded G and advanced $G^\dagger$ Green's functions, the spectral broadening of the leads Γ_α, and the momentum operator $\mathbf{P}$ are calculated self-consistently from DFT NEGF simulations of the device.

The key parameters for the detector are responsivity (R_{ph}) and external quantum efficiency (EQE). R_{ph} characterizes the efficiency of energy conversion and EQE is the ratio of extracted free electrons per incident photon outflowing the device, which define as

$$R_{ph} = \frac{I_{ph}}{PA} = \frac{I_{ph}}{eF_{ph}},$$
$$E = R_{ph}\frac{hc}{e\lambda} = R_{ph}\frac{E_{ph}}{e},$$

where P is the incident light power density, A is the effective area, e is the electron charge, λ is the wavelength of light, c is the speed of light, h is Planck constant, E_{ph} is the photon energy, and F_{ph} is the flux describing the number of incident photons per unit area and unit time.

The key parameters for FET are the subthreshold swing (SS) and transconductance (g_m), which is indicated the gate control capability of subthreshold region and superthreshold region, respectively, and defined as

$$S_S = \frac{\partial V_{GS}}{\partial\log(I_{DS})} = \left(1+\frac{C_{ch}}{C_{ox}}\right)\ln\frac{kT}{q},$$
$$g_m = \frac{\mathrm{d}I_{GS}}{\mathrm{d}V_{GS}},$$

where V_{GS} is the gate voltage, k is Boltzmann constant, T is absolute temperature, q is electron charge.

Moreover, delay time (τ) describes the upper limit of the switching speed, power dissipation (PDP) is the power consumption in one switching operation and the energy-delay product (EDP) represents energy efficiency of the devices, calculated by

$$\tau = (Q_{on} - Q_{off})/I_{on},$$
$$P = V_{DS} I_{on} \tau = V_{DS}(Q_{on} - Q_{off}),$$
$$E = \tau \times P$$

where Q_{on} and Q_{off} are the charges in the channel region in the ON and OFF state.

III. NUMERICAL RESULTS AND DISCUSSION

Figure 1(a) presents the geometric structures of monolayer InSe, which belongs to the hexagonal lattice. The optimized lattice constant is 4.094 Å and the bond length of In—Se is 2.69 Å, which agrees with previous reports [40,41]. As known from Fig. S2 (see the Supplemental Material [37]), the monolayer InSe has an indirect band structure and its gap is calculated to be 1.402 eV. The valence-band maximum (VBM) lies between K and Γ points and is contributed by a slight majority of Se, as well as the conduction-band minimum (CBM) resides at the Γ point and is composed of slight majority of In. Additionally, the band alignment for InSe with different layers is shown in Fig. 1(b). As the layer number increases from 1 to 5, the band gap decreases from 1.402 to 0.631 eV [42]. This result indicates that the layer number can modify the band gap due to the quantum confinement effect. Moreover, we calculate the absorption spectra of different layer numbers InSe, as shown in Fig. 1(c). The energy of the absorption spectra initial edge is approximately equal to the band-gap value. When the layer number gradually increases, the absorption spectra gradually improved. Particularly, for the layer number of 5, the maximum absorption spectra reach up to 49.9%. Additionally, the absorption spectra are slightly redshifted, which originates from the decrease of the energy band gap. Therefore, the results indicate that electronic and optical properties of InSe can be affected by the layer-number modulation.

In order to analyze the optical absorption, Fig. S3(a) (see the Supplemental Material [37]) presents the transition dipole moment for monolayer InSe because the optical absorption is closely related to the electrons' transition between the ground state and excited state. The transition dipole moment (bottom panel) has a maximum value at the Γ point, indicating that the transition is easily excited. Moreover, to further analyze the excitonic effects on optical absorption, Figs. S3(c) and S3(d) (see the Supplemental

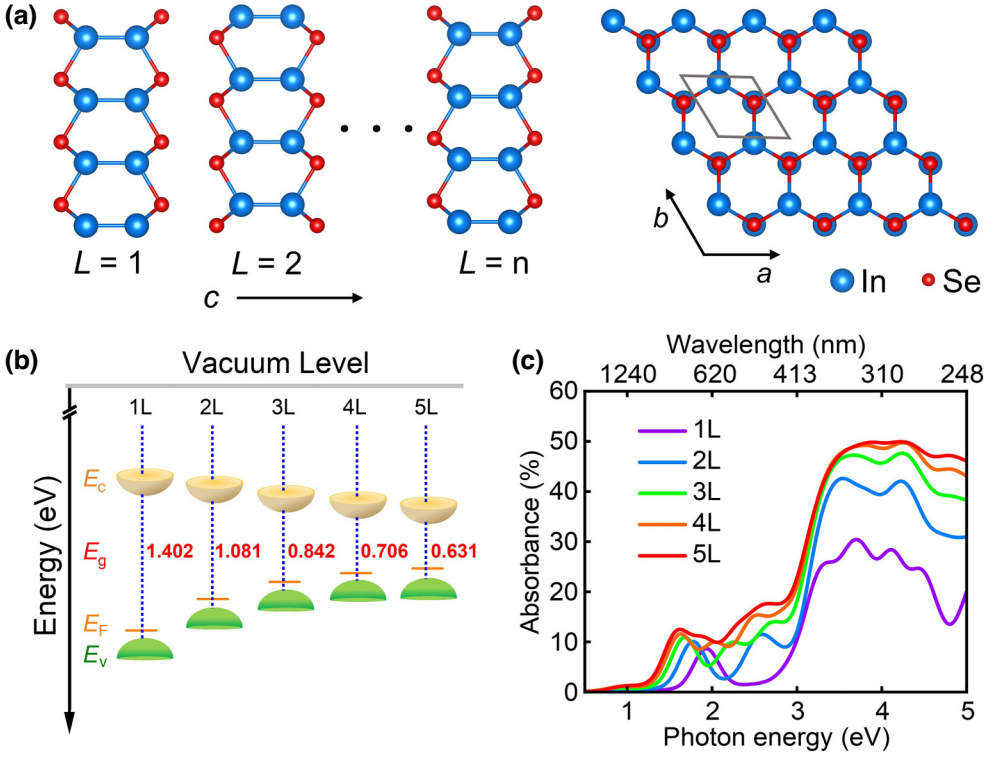

FIG. 1. (a) Side and top view of the lattice structure of monolayer InSe. (b) Band alignments and (c) absorption spectra of InSe with different layers. E_c, E_v, E_F, and E_g represent conduction band edge, valence band edge, Fermi level and band gap of multilayer InSe, respectively. L is the layer number.

Material [37]) plots the optical spectra of monolayer InSe. Without the electron-hole interaction, the optical absorption edge is located at 2.63 eV for the out-of-plane polarized light. Considering the electron-hole interaction, due to the ultrathin thickness of monolayer InSe, the optical spectra intensity is weak, and the peak is at 2.04 eV. Additionally, the transitions between the deeper valence bands and conduction bands are permitted for in-plane polarization. Including the electron-hole interaction, the peak A of optical spectrum is located at 2.59 eV, which happens in the transition from second and third valence to the first conduction band. The real-space wave functions for peak A bound exciton obtain by fixing the position of the hole in the center of supercell, as shown in Fig. S3(b) (see the Supplemental Material [37]). It displays that the electron wave function is evenly distributed, and it is a bright exciton, which is conducive to producing high optical absorption. Additionally, Fig. S3(e) (see the Supplemental Material [37]) presents wave functions at Γ point corresponding to states of bottom of the conduction band (Γ_3), top of the valence band (Γ_2) and top of the second highest valence band (Γ_1). It reflects their main In s, Se p_z and Se p_x–p_y orbital character, respectively. The second and third valence can occur a stronger mixing of states between them, which is beneficial to generation of optical transitions in InSe. These results indicate that the InSe monolayer has good optical absorption.

In order to explore the photocurrent property using InSe as photoresponsivity material under linearly polarized light, the side view of the two-probe model photodetector is depicted schematically, as shown in Fig. 2(a). The system is divided into three parts, including left and right lead structures, and scattering region. The left and right electrodes are semi-infinite in length along the transport direction of z axis, and the entire system extends periodically into the y-z plane. A small bias voltage of 0.5 V is applied between the source and drain to generate a stable continuous photoinduced current, along the direction of the z axis. In addition, considering the linearly polarized light incident vertically along the x axis, we use the angle θ in the y-z plane as the polarization angle of incident light, as shown in Fig. 2(a).

The photocurrent is displayed in Fig. 2(b) to further evaluate the optoelectronic properties of the monolayer InSe photodetector. Under illumination by linearly polarized light, the photocurrent density (I_{ph}) is essentially zero until the photon energy reaches at least 1.6 eV. Then, the I_{ph} increases significantly, the first peak appears at the photon energy of 2.2 eV and reaches the maximum when the photon energy is 4.0 eV. The insert of Fig. 2(b) exhibits the photocurrent varies as a function of cos (2θ) at photon energies of 3.1, 3.6, and 4.2 eV as examples. It displays the angle-dependent photocurrent under linear-polarized light. I_{ph} drops 75% as the polarized angle increase from 0 to 90°. Therefore, it can gain the maximum at the polarized angle θ of the light equal to 0°. Due to the excellent optoelectronic properties, we choose a polarized light along z direction to investigate the dependence of photocurrent on the number of layers. Figure 2(c) presents the all the I_{ph} of the devices have similar profiles and a wide response range from 1 to 4 eV. For the layer number increasing from 1 to 5, the photon energy of minimum photocurrent becomes larger and photocurrent spectra widen gradually, which is because of the quantum confinement effect. Moreover, the peak I_{ph} of the devices increases from 42.7 nA/m in one layer to 131.1 nA/m in five layer and significantly enlarged 3 times approximately. These results indicate that the layer number can improve the performance of InSe-based nanoscale optoelectronic devices.

To gain a deep study of the InSe-based detector, in Figs. 3(a) and 3(b), we further analyzed R_{ph} and EQE [43]. The R_{ph} presents in Fig. 3(a) for exploring the ability of the device to convert incident light energy to electrical energy at different wavelengths. The device has an

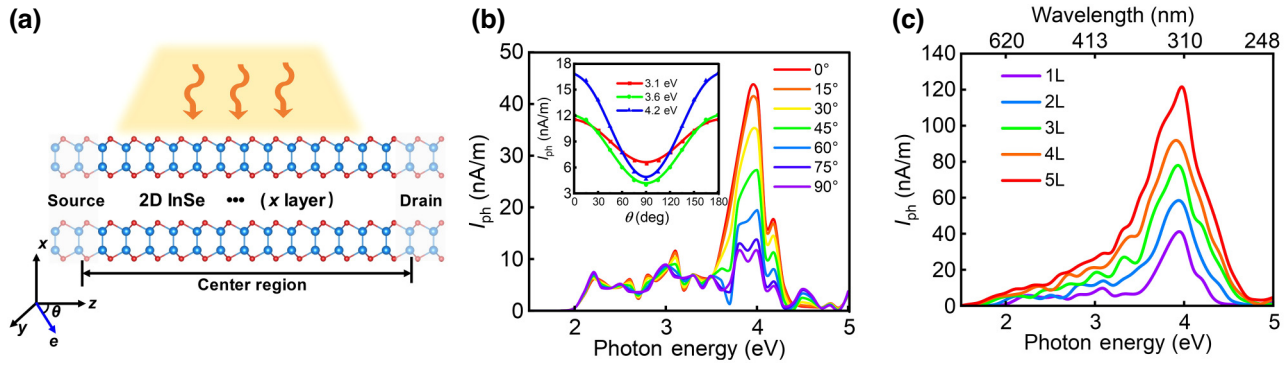

FIG. 2. (a) Device structure of few layer InSe phototransistor, and linearly polarized light irradiate vertically to the y-z plane at a polarization angle of θ. (b) The photocurrent of monolayer InSe as functions of the various photon energies under linearly polarized light with polarization angle of θ. The inset shows the functional relationship between the photocurrent and the polarization angle for photon energies of 3.1, 3.6, and 4.2 eV, respectively. (c) The photocurrent of phototransistors with various layers.

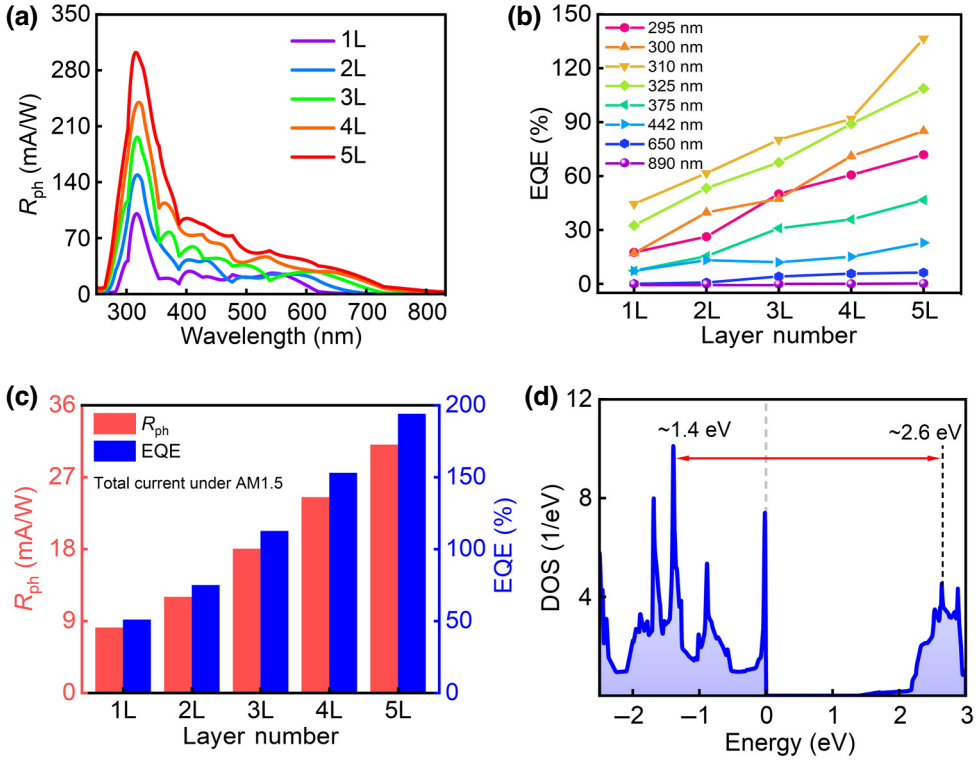

FIG. 3. Relationship between (a) responsivity versus wavelength and (b) EQE versus incident light wavelength of InSe devices with different layer thickness. (c) Responsivity and EQE under standard AM1.5 sunlight radiation for InSe with different layers. (d) Density of states of monolayer InSe.

obvious optical response in the range of 263–387 nm. In comparison, the photocurrent spectra of the five-layer InSe device are high due to the strong optical absorption. Particularly for the wavelength of 317 nm, the R_{ph} increases to 0.29 A/W with the increase of layer number. Moreover, EQE is vital to the photoelectric detector, we plot the EQE as a function of layer number as demonstrated in Figs. 3(b) and S4 (see the Supplemental Material [37]). Under the illumination of optical wavelength commonly used in experiments, the results show that EQE increases gradually with the increase of the number of layers. Take a wavelength of 310 nm as an example, the EQE increases from 44.5 (one layer) to 136.4% (five layer) with increasing the layer number of InSe material. Additionally, in Table SI (see the Supplemental Material [37]), we compare the R_{ph} and EQE of InSe photodetectors with different layers [44–47]. The results indicate that the R_{ph} of the recently reported devices improve with the layer number increasing, which reflects the regulate effect of layer thickness on the optical response of the devices. To comprehensively evaluate the photoelectric performance of the device, we further plot the R_{ph} and EQE of InSe devices under standard AM1.5 sunlight radiation in Fig 3(c) [48–50]. For one-layer to five-layer devices, the values of R_{ph} increases from 8.1 to 31.0 mA/W and EQE improves from 50.9 to 193.9%. These results indicate that the performance of the InSe-based detector is improved as the layer numbers increase, such as photocurrent, responsiveness, and EQE.

To better understand the mechanism of the layer-dependent optoelectronic properties, the density of states (DOS) of monolayer InSe is calculated, in Fig. 3(d). There are many peaks for DOS location at around −0.88, −1.39, and −1.68 eV in the valence bands, as well as +2.54, +2.63, and +2.88 eV in the conduction bands, respectively. According to Fermi's golden rule, the transition probability of electrons is proportional to the DOS. The electron transmission between photon energies of −1.39 and 2.63 eV is photoexcited via the absorption of the photon of approximately 4.0 eV, which has a large optical absorption. Therefore, the transition can generate a large probability due to the two large and sharp DOS peaks, inducing strong photocurrent. The multilayer InSe-based devices, they will have great potential for application in optoelectronic sensors.

To clarify the quantum size and gate regulation of electrical properties in the 2D semiconductor devices, we systematically investigated the transfer characteristic, subthreshold swing, and transconductance of one- to five-layer InSe-based FET. Figure 4(a) presents the structure of single-gate (SG) and double-gate (DG) devices with the gate length (L_G) of 5 nm, considering InSe as channel material. The electron doping concentration is

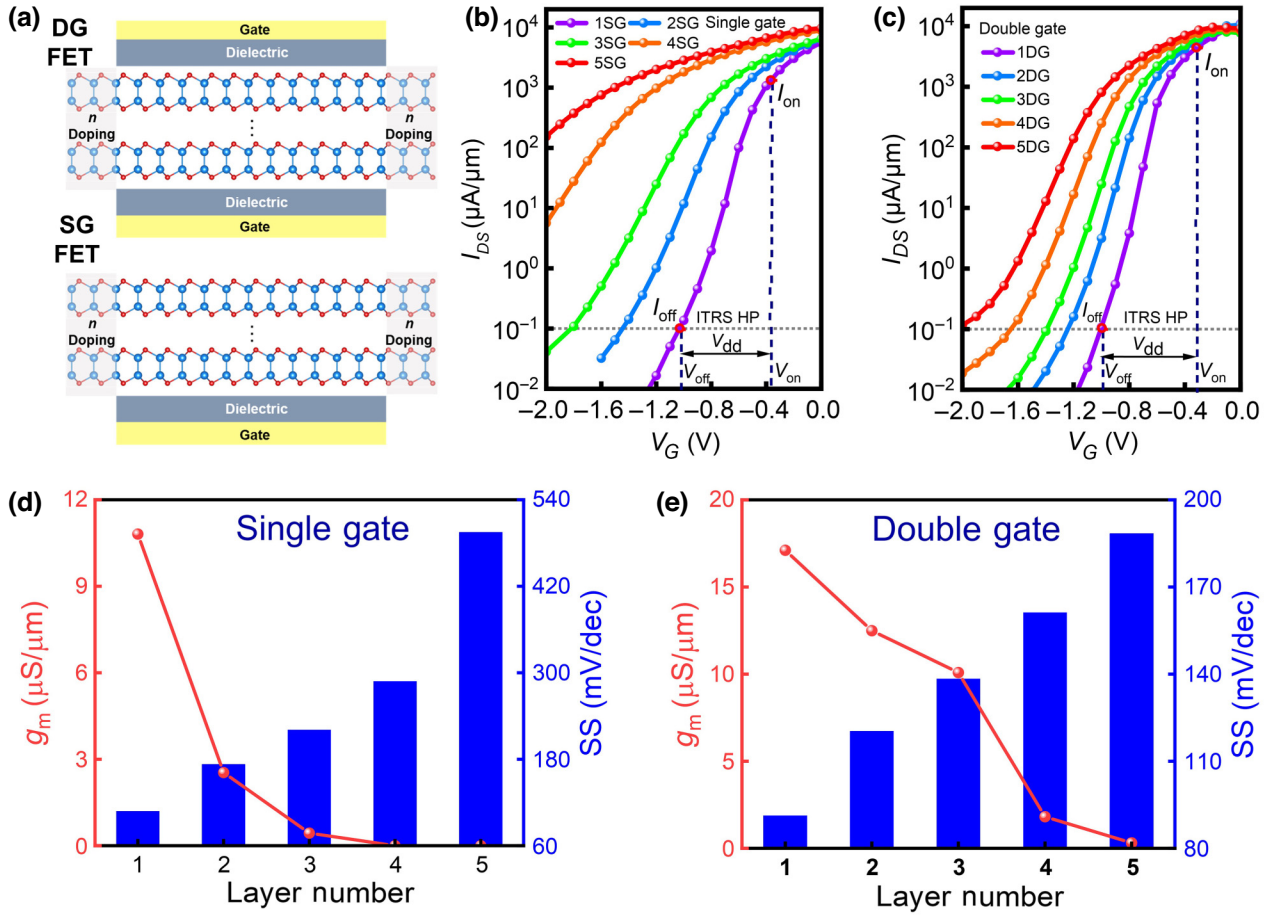

FIG. 4. (a) Device structure of InSe FET with single- and double-gate geometry, respectively. (b),(c) Transfer characteristics and (d),(e) g_m and SS of single- and double-gate 5-nm InSe FETs. The black dashed line represents the ITRS HP standard.

5×10^{13} cm^{-2} for both source and drain. According to the standards of ITRS for 5-nm devices, the equivalent oxide thickness (EOT) is set at 0.41 nm, supply voltage (V_{dd}) is set at 0.64 V, and OFF-state current (I_{off}) is fixed at 0.1 μA/μm [51,52].

Figures 4(b)–4(c) display the transfer characteristic curves of InSe SG and DG FETs with different layer numbers, respectively. The leakage currents decrease when the layer number decreases, and hence the monolayer devices have minimum leakage current. Compared to the SG devices, the DG devices have larger I_{DS}, as shown in Fig. S5 (see the Supplemental Material [37]). Under the modulation of 0.64-V gate voltage, the DG devices can quickly reach the current of 0.1 μA/μm, that is the OFF-state current of ITRS HP standard. Thus, the SG FET for four and five layers is hard to meet the standard. In addition, for the logic device, I_{on} is a key parameter for evaluating the transition speed. The I_{on} is determined by the $V_{GS,ON} - V_{GS,OFF} = V_{dd}$, in which $V_{GS,on-off}$ is the gate voltage at ON and OFF state. For SG and DG monolayer devices, the I_{on} can satisfy the ITRS HP standard requirement (900 μA/μm), reaching 1180 and 3432 μA/μm, respectively. The high I_{on} is advantageous for a fast-switching speed server. However, as the layer number increases to five for DG and three for SG devices, the I_{on} decreases to only 19 and 32 μA/μm, respectively, and the switching characteristics are degraded severely.

To further evaluate the layer-number influence on the performance of the multilayer InSe FETs, the SS and g_m are extracted from the transfer characteristics, as displayed in Figs. 4(d) and 4(e). The lowest limit of SS is 60 mV/dec according to the "Boltzmann tyranny" [53]. The results show that when layer number decreases from five to one, the SS of SG (DG) InSe FETs gradually decreases from 494 to 108 (188 to 91) mV/dec. Despite the thicker FETs having high electron mobility, the increasing mobility does not compensate for the increasing SS. Therefore, the I_{on} and SS of the five-layer device are worse than the monolayer one. Moreover, compared to the SG structures, the DG InSe FETs have a steeper SS and higher I_{on}. The SS for thermionic current is proportional to $1 + C_{ch}/C_{ox}$, where C_{ch} is quantum capacitance and C_{ox} is oxide capacitance. For DG configuration, the oxide capacitance is double of SG case, hence DG devices present lower SS than that

of SG devices. Furthermore, the g_m of both SG and DG InSe FETs monotonically decreases with the increasing layer number. The maximum value reaches up to 10 and 17 μS/μm for the SG and DG constructs, respectively. Therefore, the DG devices ensure higher g_m and carrier concentration, inducing higher I_{on}. These results indicate that the transport properties can be effectively modulated by layer number and gate structures, and monolayer DG devices present excellent electrical properties.

In Figs. 5(a) and 5(b), the electronic transmission coefficients of SG and DG InSe FETs under the gate voltage of −1.5 V regulate by changes in layer number. Due to the integral of the electronic transmission coefficient within the bias window equal to the current, the one-layer device has the minimum leakage current. This is because the energy barrier of the electrode and channel is controlled by the gate voltages. Under the same gate voltage, the monolayer device has strong gate control abilities and makes the electron become extremely difficult to inject into the channel region from the *n*-type electrode. Therefore, the channel region has lower electron concentration and results in little leakage current. Moreover, we further compare the device transmission coefficient of SG and DG InSe devices, the transmission coefficients of the DG structures are significantly 2 orders of magnitude lower than that of the SG case. This indicates the DG monolayer device has a lower current in the subthreshold region.

To further explain the difference of I_{DS} for the FET in the superthreshold region, Figs. 6 and S6 (see the Supplemental Material [37]) display the transmission eigenstates from one- to five-layer InSe FET at ON-state gate voltages. The transmission eigenstate is a three-dimensional wave function indicating the electronic transmit ability, which can be obtained by propagating the linear combination of the Bloch states. They are declared by a contour surface with isovalue presented by the size and the phase of the eigenstate. Figure 6 presents the incoming electron wave function of the one- and five-layer SG and DG InSe FET devices can propagate through the whole channel reaching the drain region. The conductive transmission channels are open, resulting in a high current at the ON state. As shown in Figs. 6(a) and 6(b), comparing the transmission eigenstates of monolayer InSe devices, the spatially resolved size have similar distribution patterns. The spatially resolved phase of the DG and SG devices have little phase of π, which means that most of the carriers can be easily transmitted to the drain. Therefore, the ON-state current and SS of the devices reach approximately 10^3 μA/μm and approximately 10^2 mV/dec, respectively, indicating that the gate control ability of the SG device is

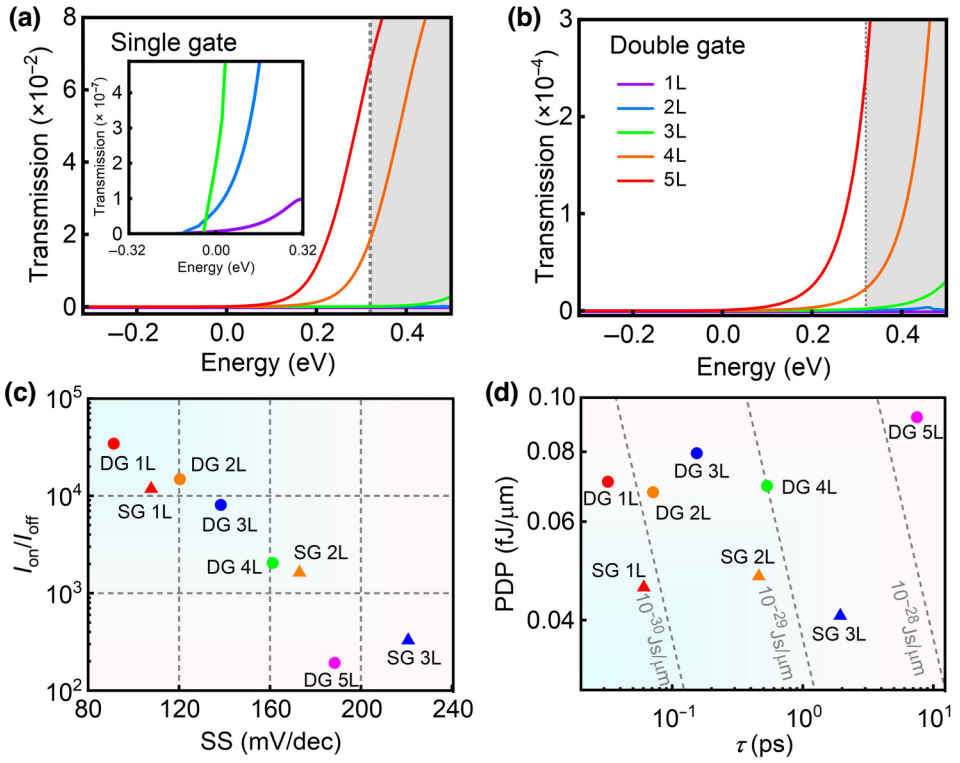

FIG. 5. (a),(b) Transmission spectra for the gate voltage of −1.5 V, the relationships between (c) SS and I_{on} and I_{off}, and (d) τ and PDP of the InSe devices with different layers. The inset of (a) shows the transmission spectra for the three-, four-, and five-layer device. The gray region indicates the exterior of the bias window. The blue corner represents the perfect performance region in the upper left corner and lower left corner for (c),(d), respectively.

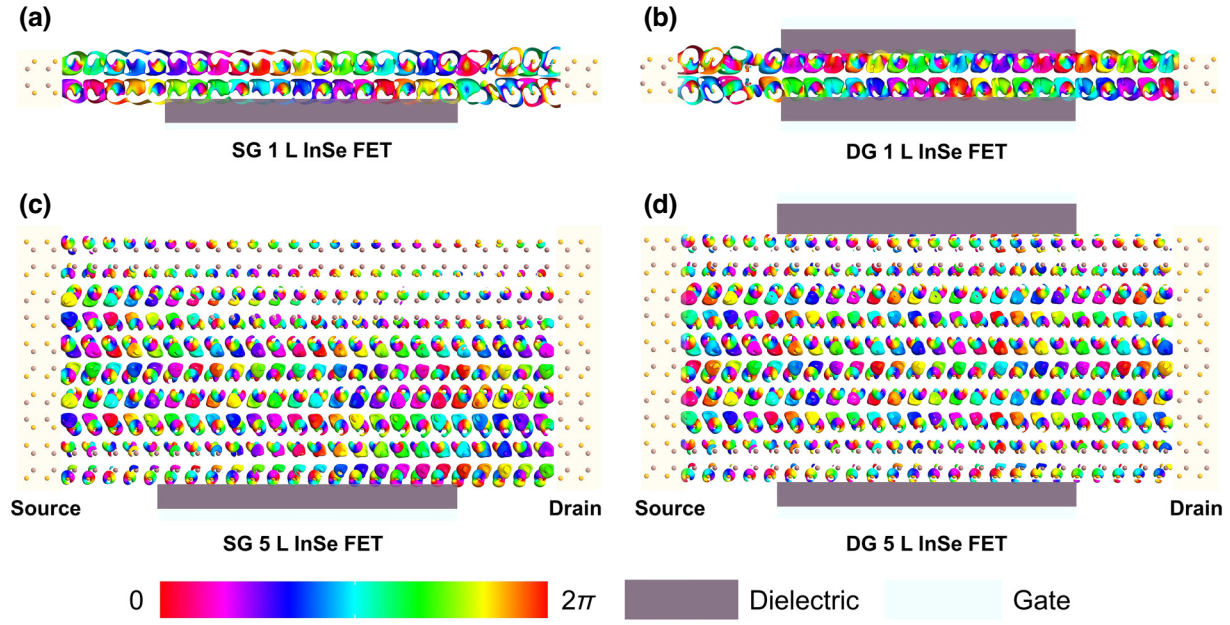

FIG. 6. Transmission eigenstates for SG and DG InSe-based FETs at the ON states with layer numbers of one and five, respectively. The color bar indicates the phase of the eigenstate.

equivalent to the DG case. However, in contrast to the SG five-layer device, the electrons of the DG five-layer device are affected by the electrostatic potential of the symmetrical gate, and form a symmetrical distribution of spatially resolved transmission eigenstates, leading to the higher ON-state current. Figs. S6(a) and S6(d) (see the Supplemental Material [37]) show that the same situation also appears in the case of the two- and three-layer devices, but the size of the eigenstate is reduced. Thus, the ON-state current is decreased. Additionally, Figs. 6(c) and S6(e) (see the Supplemental Material [37]) show that the size of transmission eigenstates at the top layer far from the gate is smaller than the bottom case. This indicates that in SG devices the eigenstate of the top layer far from the gate is significantly localized, and part of the incoming electron wave function passes through the whole channel, which leads to the low ON-state current. These further illustrate that the gate control ability of DG devices is more effective at controlling channel carriers than that of the SG cases, and introduces high g_m and I_{on}. As well as, the single-layer devices are more easily controlled SG, which facilitates the preparation and integration of devices.

In order to evaluate the device performance comprehensively, Fig. 5(c) presents the relationship between I_{on}/I_{off} and SS of InSe FETs with different layers according to HP requirements of ITRS 2013 in the 2028 horizon. Since the I_{off} of SG devices with the four- or five-layer channel cannot meet the HTRS HP standard (900 μA/μm), they are not covered in the subsequent discussion. The device reveals that the performance enhances with the decreasing layer numbers. For the monolayer device with double gate, the I_{on}/I_{off} and SS reach approximately 3.4×10^4 and 91 mV/dec, which display excellent performance and locate at the perfect region. The degrees of freedom for I_{on} and layer number enable them to apply in various conditions. Compared to layer number from one to five, the I_{on}/I_{off} and SS of DG devices are superior to the SG constructs. Therefore, the DG devices with the one- or two-layer channel and the SG devices with the one-layer channel satisfy the I_{on} and I_{on}/I_{off} requirements of the ITRS HP standard (900 μA/μm and 9000).

Additionally, as displayed in Fig. 5(d), we further compare gate τ and PDP, which are another two key indicators for transistors. With the decreasing layer number, the τ of the SG(DG) InSe FET decreases rapidly and the value of monolayer devices is lower to reach 0.060 and 0.032 ps, which is smaller than the HP standards (0.423 ps). Moreover, the PDP of monolayer SG(DG) InSe device has a lower power consumption of 0.045(0.070 fJ/μm) compared to the HP standards (0.24 fJ/μm). As well as, the value of DG device is larger than that of the SG cases, due to two gate constructs. However, PDP is no significant change by modulating the layer number, this reveals the power consumption is mainly dependent on the type of the gate structure. To comprehensively compare the performance of the device with different layer numbers, in Table SII (see the Supplemental Material [37]), we compare the performance of *n*-type InSe FETs against the ITRS roadmaps for HP devices, the main parameters, including I_{on}, τ, and PDP. It can be clearly seen that the performance of DG 1L devices are superior to others in terms of key parameters.

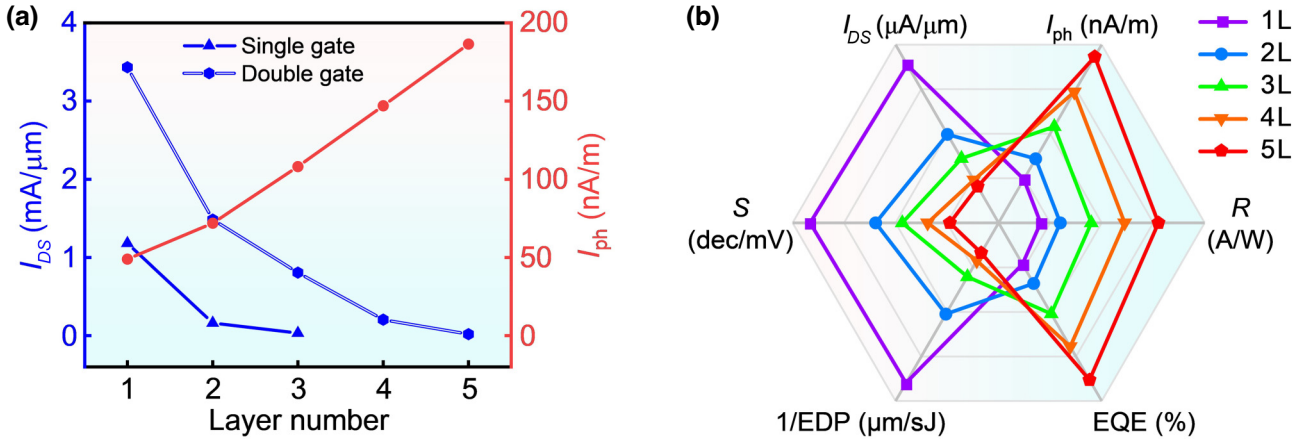

FIG. 7. Comparison of (a) I_{DS} (blue bars) and I_{ph} (red bars) and (b) I_{DS}, S, EDP, I_{ph}, R, and EQE of InSe-based devices with different layers.

Moreover, for Fig. 5(d), the EDP is represented by straight dotted lines. The value of all the devices is smaller than the minimum ITRS requirements (4.18×10^{-28} J s/μm) and comes in well below the ITRS requirements for the 2028 horizon (1.02×10^{-28} J s/μm) except the DG five-layer device. Remarkably, both the SG and DG monolayer InSe FETs (red dots) have almost the lowest EDPs among all of these considered devices for the HP applications, indicating an extremely high operation speed and low-energy consumption. The short intrinsic delay time and low power consumption thus further reveal the promising potential DG monolayer InSe devices for applications in digital circuits.

In order to comprehensively consider the electronic and optical properties of the device, the I_{DS} and I_{ph} of InSe-based devices with a different number of layers are also explored as shown in Fig. 7(a). The I_{DS} of SG and DG devices have the same tendency. As the layer number decreases, the device has a large ON-state current. However, electronic properties deteriorate with the layer number increase. This displays that the DG monolayer InSe gains the maximum I_{DS} reach 3432.84 μA/μm and presents outstanding electronic performance. Moreover, the I_{ph} monotonously increases when the layer number increases, and the device with a five-layer InSe channel reveals high R_{ph} and EQE. To further study the performance of dual-gate devices with layers one–five InSe channels, we plot Fig. 7(b) using six parameters to characterize the electrical and optical properties of the device. The parameter points connect to form the shape of a hexagon. Among them, S is the subthreshold slope ($S = 1/SS$), and EDP is expressed in reciprocal form. Therefore, the larger the enclosed area, the more excellent electrical and optical properties performance of the devices. Figure 7(b) for the one-layer device presents the I_{DS}, S, and EDP are superior to other devices, so the one-layer device has excellent electronic properties. On the other hand, the I_{ph}, R, and EQE for the five-layer devices are larger than the others, which indicates this device has excellent optical properties. However, multiple function devices are now receiving more attention. Accordingly, weighing the electrical and optical properties, the six parameters of two- and three-layer devices are all in the medium level, so it can have excellent electronic and optical properties at the same time. Further comparison of the devices, it is interesting that the layer number of the channel material has a significant effect on the electronic and optoelectronic properties of the device. This result reveals that it is still essential to optimize the InSe layer number to function with electronic and optical properties in the future.

IV. CONCLUSIONS

In summary, we design the InSe transistor integrating electronic and optical performance to systematically explorer the modulation of the layer number and gate engineering. Due to the quantum confinement effect, the band gap of InSe can be modified by layer number. As the photodetector, the maximum I_{ph} of the five-layer devices reaches 131.1 nA/m, which is three times that of the monolayer cases. The R_{ph} and EQE improve with the layer number increasing. Moreover, for SG and DG monolayer devices, the I_{on} reaches 1180 and 3432 μA/μm, respectively. The key parameters of monolayer FET outperform the ITRS HP standard requirement. In addition, the device can show excellent electronic and optical properties by choosing the proper number of layers. The results of relationship of layer number and performance guide the applications of 2D InSe in multifunction electronics and optoelectronics devices.

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