Cryogenic hyperabrupt strontium titanate varactors for sensitive reflectometry of quantum dots

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Radio-frequency reflectometry techniques enable high-bandwidth readout of semiconductor quantum dots. Careful impedance matching of the resonant circuit is required to achieve high sensitivity, which, however, proves challenging at cryogenic temperatures. Gallium arsenide–based voltage-tunable capacitors, so-called varactor diodes, can be used for *in situ* tuning of the circuit impedance but deteriorate and fail at temperatures below 10 K and in magnetic fields. Here, we investigate a varactor based on strontium titanate with a hyperabrupt capacitance-voltage characteristic, i.e., a capacitance tunability similar to the best gallium arsenide–based devices. The varactor design introduced here is compact, scalable, and easy to wire bond, with an accessible capacitance range from 45 pF to 3.2 pF. We tune a resonant inductor-capacitor circuit to perfect impedance matching and observe robust temperature- and field-independent matching down to 11 mK and up to 2 T in-plane field. Finally, we perform gate-dispersive charge sensing on a germanium-silicon core-shell nanowire hole double quantum dot, paving the way toward gate-based single-shot spin readout. Our results bring small magnetic field–resilient highly tunable varactors to mK temperatures, expanding the toolbox of cryo-radio-frequency applications.

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I. INTRODUCTION

Recent years have seen rapid progress in the realization of spin qubits in semiconductors [1–4]. Hole spins in germanium (Ge) and silicon (Si) nanostructures are of particular interest due to the availability of all-electrical spin control [2,5–9], short gate times [10–12], high-temperature qubit operation [13–15], an intrinsically low concentration of spinful nuclei and reduced hyperfine interaction due to the p-type hole wave function [16], and the presence of noise sweet spots [17–19].

Fast readout of charge and spin states in semiconductor qubit devices is typically achieved using high-frequency reflectometry methods such as radio-frequency (rf) single-electron transistors [20–23], single-lead sensor dots [24,25], or gate-dispersive charge sensing [26–30]. The latter constitutes the smallest-footprint charge sensing setup: the same gate that electrostatically defines a quantum dot is used to sense nearby dots. This makes gate reflectometry the obvious choice to use with nanowire qubits, since external charge sensors are difficult to implement [31–35].

High device impedances, typically on the order of the resistance quantum $Z \geq 25.8\,\mathrm{k\Omega}$ up to $Z \sim \mathrm{G\Omega}$ for gate sensors, make it necessary to down-convert toward $Z_0 = 50\,\Omega$ to maximize the signal and bandwidth. Down-conversion is implemented using inductor-capacitor (LC) resonators, so-called tank circuits, consisting of surface-mounted inductors and parasitic circuit or device capacitances [29]. Careful circuit design ensures optimal signal-to-noise ratios (SNRs) and high sensitivities [27,36]. The rf characteristics of the circuits are frequently affected by the cryogenic temperatures and magnetic fields required for qubit operations. Thus, *in situ* tuning of the impedance matching and thereby the coupling of the rf source circuitry and the LC resonator is needed. This can be achieved using varactors [16,24,37–39].

Commercial varactors with a high tuning range and steep capacitance-voltage (C-V) curves, classified as hyperabrupt varactors, are typically doped gallium arsenide (GaAs) diodes. The width of the p-n junction depletion region of the diode can be tuned by applying a reverse bias voltage, effectively changing the capacitor thickness and thus the series capacitance of the diode. Doped varactors are suitable for quantum applications only to a limited extent, requiring multiple diodes

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[38,39]. This is due to freezing-out effects [39] and strong dependencies on applied magnetic fields. In particular, perfect impedance matching using GaAs varactors has so far only been demonstrated down to $T \sim 200\,\mathrm{mK}$, using two varactors [39].

To resolve these issues, quantum paraelectric materials such as strontium titanate (STO) are under consideration as alternative cryogenic varactors [40,41]. Below 10 K, the dielectric constant of STO ranges from $\epsilon_r = 10\,000$ to $\epsilon_r = 24\,000$, depending on the crystal orientation and has been shown to be tunable with electric fields, reaching dielectric constants that are more than a factor of 10 lower [42–45]. This strong electric field tunability makes STO a prime candidate for the design of tunable cryogenic rf components, such as varactors or resonators [40,41,46]. The relatively small target capacitance range, $C_{\mathrm{var}} < 50\,\mathrm{pF}$ [38], required for impedance matching makes STO-varactor engineering challenging. Given the high ϵ_r, a plate capacitor formed by electrodes on opposite faces of STO crystals encounters conflicting constraints when required to reach such low C_{var}: (i) either the capacitor plate size is too small for wire bonding or (ii) the plate-to-plate distance is too large to form uniformly high fields, reducing the tunability [41]. Furthermore, contacting the electrodes on opposing faces of the crystal is inconvenient and limits scalability.

Here, we present a surface-patterned ring varactor design on STO that achieves hyperabrupt C-V characteristics and a tuning range exceeding that of typical GaAs varactors [24,38,39] while operating down to millikelvin temperatures and independent of magnetic fields. We fabricate varactors of various dimensions and characterize them first at 4 K, optimizing for tunability and capacitance range.

Next, we integrate such a varactor in a tank circuit for gate-dispersive readout. The selected design has a 300-µm footprint, smaller than STO plate-capacitor layouts and packaged commercial varactor diodes. Critical coupling is reached over a broad range of temperatures from $T \approx 4\,\mathrm{K}$ to 11 mK and in magnetic fields up to 2 T without retuning of the varactor. We use the matched circuit to dispersively measure charge transitions in a hole double quantum dot (DQD) formed in a Ge-Si core-shell nanowire (NW) [47–50]. Similar NWs have been used to demonstrate all-electrical ultrafast spin-qubit operation with a high degree of tunability [6–8,10]. To directly probe the significance of impedance matching for gate-dispersive charge sensing, we measure SNRs for variable matching conditions and at different charge transitions. Our implementation of gate-dispersive charge sensing paves the way for high-fidelity gate-dispersive single-shot spin readout with gated quantum dots (QDs). The realization of a highly tunable capacitor at cryogenic temperatures enables more sophisticated circuit architectures in various applications beyond charge sensing in semiconductors.

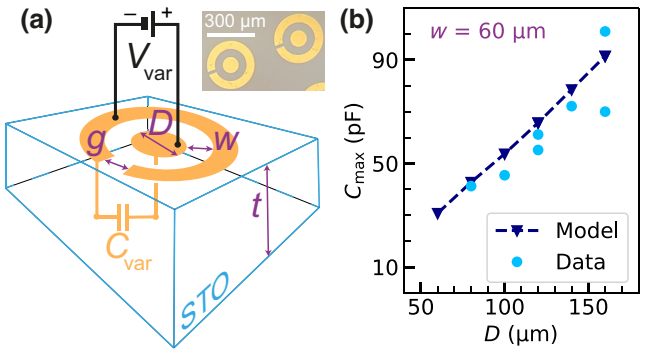

FIG. 1. The geometry of STO-ring varactors. (a) A schematic diagram of the STO-varactor design. Two gold electrodes, a circle with diameter D and a concentric ring with a spacing to the circle of w and a gap of $g = 20\,\mu\mathrm{m}$, form the capacitor. The application of a dc voltage V_{var} induces an electric field within the STO crystal, which is highly localized due to the compact geometry. The inset shows an optical micrograph of finished varactors. (b) The zero-field capacitance C_{max} as a function of D for $w = 60\,\mu\mathrm{m}$, simulated in COMSOL (triangles) and measured (circles).

II. VARACTOR CHARACTERIZATION AT 4 K

A. Geometry

The varactor ring design is presented in Fig. 1(a). It features two electrodes, a central circle with diameter D and a concentric ring, 50 µm wide and separated from the circle by a distance w. A $g = 20\,\mu\mathrm{m}$ wide gap in the outer ring facilitates lift-off. The electrodes were patterned on the polished side of a commercially available (001) STO chiplet with thickness $t = 0.5\,\mathrm{mm}$ (see Appendix A 1). This geometry provides several key features for optimal varactor performance: electric fields in the crystal are localized and large close to the electrodes. This allows for high tunability of ϵ_r while keeping the peak capacitance C_{max} in the desired range. The small varactor footprint of approximately 300 µm and the single-sided metallization allows tight integration with other circuit components and provides scalability. In particular, we are able to fit nine independent ring varactors on a chiplet the size of commercial surface-mounted GaAs varactors used in comparable experiments (MACOM MA46-series) [24,38,39].

All measurements presented in this section were performed at 4 K using standard lock-in techniques at 1 kHz. No frequency dependence of tunability and ϵ_r from 1 kHz to 50 MHz has been reported previously, predicting constant ϵ_r up to 100 GHz [44]. We thus expect our low-frequency results to apply at typical reflectometry frequencies as well. We estimate the zero-field capacitance C_{max} of our design using COMSOL to find the optimal device dimensions. For simplicity, we assume an isotropic dielectric constant $\epsilon_r = 24\,000$, approximately the experimental value for field lines parallel to the (001) direction at 4 K [44]. In our simulation, we primarily focus on D and

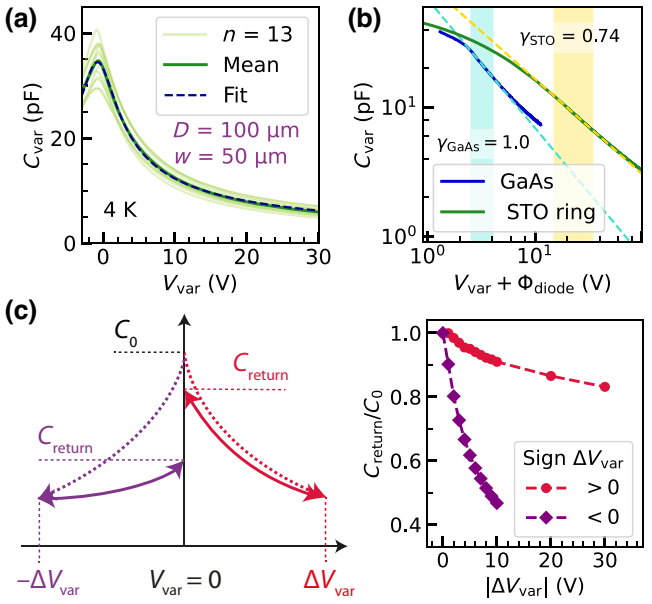

FIG. 2. The C-V characteristic of STO varactors. (a) The varactor capacitance C_{var} as a function of the applied dc voltage measured on 13 nominally identical devices (light green), the mean value (dark green), and the fit of the mean to Eq. (1) (dark blue). Fitting all 13 traces yields $C_0 = 34 \pm 3\mathrm{pF}$, $V_{\mathrm{offset}} = -0.8 \pm 0.1\mathrm{V}$, and $V_0 = 2.4 \pm 0.3\mathrm{V}$. (b) A comparison of the capacitance tunability of a commercial GaAs varactor with one exemplary STO ring at 4 K. The yellow (turquoise) dashed lines are fits of Eq. (2) to the steepest regime of the STO (GaAs) C-V traces, indicated by the shaded areas. (c) A schematic image (left panel) and a quantitative analysis (right panel) of the varactor peak-capacitance reduction. The application of a negative V_{var} (purple diamonds) causes a significant degradation of $C_{\mathrm{var}}(V_{\mathrm{var}} = 0\,\mathrm{V})$, which is less severe for positive V_{var} (red circles).

w, finding that neither g nor the width of the outer ring have a strong influence on C_{max}. We vary D from 60 µm to 160 µm and w from 10 µm to 80 µm and fabricate an array of 36 different combinations, excluding $w > 60$ µm due to decreased tunability. Not all combinations were measured because too small w and D frequently resulted in shorts between the two electrodes from wire bonding (for details, see Appendix C 1).

In Fig. 1(b), we compare the zero-field capacitance C_{max} estimated from finite-element simulations and measurements for $w = 60$ µm and variable D. We find good agreement, noting that some small capacitance over-estimations by the model could be explained by the anisotropy of ϵ_r, which was neglected in the simulation. Furthermore, the partial loss of tunability caused by the application of negative varactor voltages V_{var} described in Sec. II B and Fig. 2(c) may also explain some of the measured C_{max} lying below the model, as some of these values were taken from voltage sweeps starting at a varactor voltage $V_{\mathrm{var}} = -2\,\mathrm{V}$.

B. Voltage tunability

The capacitance tunability of STO varactors relies on an incipient ferroelectric phase transition at low temperatures that is never reached due to quantum fluctuations [40,41,46,51]. Below about 10 K, the low-temperature limit is reached and ϵ has no further temperature dependence, thus rendering STO varactors highly reliable and repeatable below 10 K. Johnson's relation describes the resulting highly nonlinear dependence of ϵ_r on dc electric fields to first order and neglecting anisotropies and can be used to express the voltage tunability of C_{var} as [40,41,51]:

$$C_{\mathrm{var}}(V_{\mathrm{var}}) = \frac{C_0}{\left(1 + \frac{(V_{\mathrm{var}} - V_{\mathrm{offset}})^2}{V_0^2}\right)^{1/3}}. \tag{1}$$

Here, C_0 is the zero-field capacitance, V_{var} the applied varactor voltage, and V_{offset} accounts for an experimentally observed deviation of the peak capacitance from $V_{\mathrm{var}} = 0\,\mathrm{V}$. The voltage V_0 parametrizes the strength of the tunability of ϵ_r and is geometry dependent [46].

From now on, we focus on devices with $D = 100\,\mu\mathrm{m}$ and $w = 50\,\mu\mathrm{m}$, as these varactors covered the desired capacitance range and could be easily bonded. The C-V characteristics of 13 nominally identical devices are shown in Fig. 2(a) together with their average trace, indicating that all devices have capacitances within 10% of the average. All curves show the characteristic maximum capacitance around zero V_{var} and the suppression at larger voltages. Fitting all 13 traces to Eq. (1) reveals that the model agrees very well with the data over almost the entire range. Further, the three fit parameters are very similar for all devices, exhibiting a variability of only about 10%.

For comparison with other varactors, we use the standard diode-varactor theory, which uses a power-law exponent γ as a benchmark for varactor performance, where a larger γ indicates higher tunability. Abrupt varactors have $\gamma \leq 0.5$ and if $\gamma > 0.5$, the varactor is considered hyperabrupt, indicating the highest tunability [52]. As a standard for comparison, a typical GaAs varactor used in similar experiments has $\gamma = 1$ [Fig. 2(b)]. The C-V characteristic of a diode varactor near its peak tunability regime can be expressed as

$$C_{\mathrm{var}}(V_{\mathrm{var}}) = \frac{K}{(V_{\mathrm{var}} + \Phi_{\mathrm{diode}})^{\gamma}}, \tag{2}$$

where K is the capacitance constant, V_{var} is the applied varactor voltage, and Φ_{diode} is the built-in potential of the varactor [52]. For GaAs varactors, $\Phi_{GaAs} = 1.3\,\mathrm{V}$ holds [53].

Fitting the peak tunability regime of the C-V traces of all 13 devices to Eq. (2), we find hyperabrupt behavior over a large voltage range with mean $\overline{\gamma}_{\mathrm{STO}} = 0.72 \pm 0.05$, as shown in Appendix C 3. This is slightly higher than

the $\gamma \approx 0.66$ expected from Eq. (1). We note that in this high-tunability regime [yellow shaded in Fig. 2(b)], the fit to Eq. (2) captures the measured capacitance slightly better than Eq. (1), as shown in Appendix C 2. In analogy to the built-in potential, V_{offset} is used as $\Phi_{\text{STO}} = 0.8\,\text{V}$ in the fits. To minimize the loss in tunability discussed in the following, we measure a single varactor from $V_{\text{var}} = 0\,\text{V}$ to $V_{\text{var}} = 100\,\text{V}$, as shown in Fig. 2(b). The accessible capacitance range of the STO varactor is $C_{\text{var}} = 45.0\,\text{pF}$ to 3.2 pF, exceeding the range of a commercial GaAs device used in comparable experiments (MACOM MA46H204-1056) [24,38,39] and of previous STO plate-capacitor implementations [41].

Interestingly, varactors with identical geometry but fabricated on (100) and (111) STO showed no significantly different C-V response as compared to the (001) devices. While (100) is equivalent to the (001) direction, the zero-field dielectric constant of (111) STO is $\epsilon_r = 12\,000$ [44], half the value of that for (001) STO. The approximately circular symmetry of the surface electrode evenly integrates over all field directions in the crystal plane, effectively averaging away the anisotropy in ϵ_r.

Sweeping from $V_{\text{var}} = 0\,\text{V}$ to a finite voltage ΔV_{var} and back to zero, we observe a reduction in $C_{\text{var}}(V_{\text{var}} = 0\,\text{V})$ from C_0 to C_{return} [Fig. 2(c)]. If V_{var} is subsequently kept within this same range, the C-V characteristic remains stable. The reduction is strongly dependent on the sign of ΔV_{var} as defined in Fig. 1(a). A negative ΔV_{var} causes significantly bigger losses than a positive ΔV_{var}. This effect is quantified in the right panel of Fig. 2(c), where C_{return}/C_0 is measured by sweeping to increasingly large $|\Delta V_{\text{var}}|$ and back to zero. The lost tunability range is fully recovered upon thermal cycling to 295 K. Similar effects have previously been discussed with several paraelectric materials and can be explained by the polarization of microclusters in the crystal, such as O vacancies in STO [46,51]. This voltage polarity- and voltage-history-dependent C-V characteristic, while not related to ferroelectric hysteresis, has been referred to as hysteresis in the literature [41,46]. The residual degradation of tunability present even when only applying positive voltages can easily be circumvented by choosing appropriate varactor dimensions and limiting the range of voltages applied.

III. GATE-DISPERSIVE CHARGE SENSING WITH Ge-Si CORE-SHELL NANOWIRE DOUBLE QUANTUM DOTS

A. Impedance matching

In a next step, we implement gate-dispersive charge sensing with a Ge-Si core-shell NW hole DQD, using an STO varactor to optimize impedance matching (for the NW device-fabrication details, see Appendix A 2). Quantum dots hosted in these NWs have been measured in dc measurements [48,49,54–57], using additional quantum dots as charge sensors [31,32] and with an on-chip superconducting resonator [35,58]. A strong electrically tunable direct Rashba spin-orbit interaction is present in Ge-Si core-shell NWs [6–8,49], enabling all-electrical spin control. Recent spin-qubit experiments in this system have shown Rabi frequencies of several hundreds of megahertz [10].

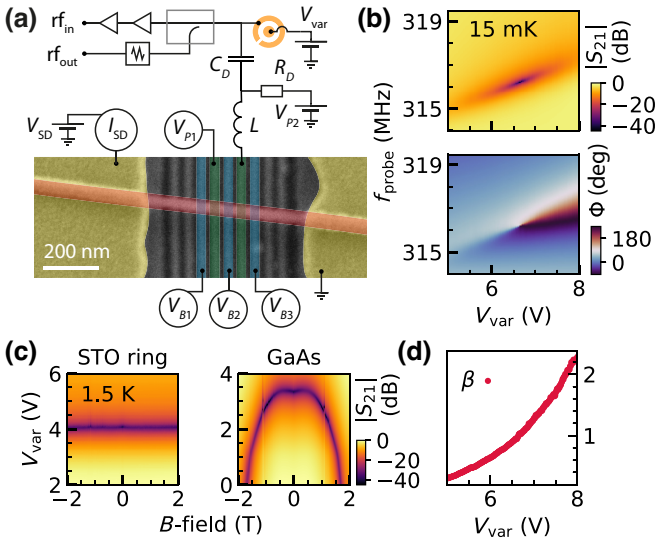

FIG. 3. The reflectometry setup and impedance matching. (a) The gate-reflectometry circuit with STO matching-varactor. The false-colored SEM image shows an NW device with nine gates, five of which were used to form a DQD with two plungers (green) and three barrier gates (blue). The NW (red) is contacted on either side, enabling dc transport measurements through the wire. (b) Impedance matching at probe temperature $T_{\text{probe}} \approx 15\,\text{mK}$. At perfect matching, the reflected amplitude is minimal and the phase response indicates a sudden shift from undercoupled ($V_{\text{var}} < 6.625\,\text{V}$) to overcoupled ($V_{\text{var}} > 6.625\,\text{V}$). (c) The magnetic field–dependent impedance matching at $T \approx 1.5\,\text{K}$ without an NW device. The tank with a STO-ring varactor is unaffected by magnetic fields up to 2 T. Using a GaAs varactor, the matching voltage shifts strongly, complicating the qubit measurements. (d) The coupling coefficient β as a function of V_{var}.

The reflectometry setup used to integrate an STO-ring varactor with the NW device shown in Fig. 3(a) is described in more detail in Appendix B. The tank resonance frequency at $f_{\text{res}} = 316.20 \pm 0.05\,\text{MHz}$ allows us to extract the parasitic capacitance, $C_p = 1.15 \pm 0.03\,\text{pF}$, of the circuit. Tuning the tank as shown in Fig. 3(b), we reach impedance matching at probe temperature $T_{\text{probe}} \approx 15\,\text{mK}$ in a Bluefors dilution refrigerator. We find the STO varactor to be highly temperature resilient (see Appendix C 4). The resonator coupling coefficient $\beta = Q_0/Q_{\text{ext}}$ depicted in Fig. 3(d) is a convenient measure to evaluate the matching of the resonator impedance Z_{res} to the external-source circuitry impedance Z_0 and can be extracted from the S_{21} response of the tank at resonance following Ibberson

et al. [39]. It is formally defined as the ratio of the unloaded (Q_0) and external (Q_{ext}) quality factors [39]. The transition from the under- ($\beta < 1$; $Z_{res} > Z_0$) to the overcoupled regime ($\beta > 1$; $Z_{res} < Z_0$) is marked by a narrow minimum in the reflected amplitude $|S_{21}|$ and a sudden flip by 180° in the phase of the reflected signal Φ where perfect matching ($\beta = 1$; $Z_{res} = Z_0$) is reached.

The impact of an in-plane magnetic field on the matching with STO-ring varactors and commercial GaAs varactors is compared in Fig. 3(c). Both scans were recorded at 1.5 K, because the GaAs varactor froze out at lower temperatures. No NW device was present for both scans. Fixing f_{probe} near resonance at zero field, B is subsequently swept against V_{var}. The GaAs varactor shows a strong dependence on B even for $B \leq 1$ T, the typical spin-qubit operation range [2,3,5,8,13]. The STO remains independent of the B field down to millikelvin temperatures (see Appendix C 5).

B. Charge sensing

Finally, we investigate charge transitions in a Ge-Si core-shell NW DQD using the impedance-matched tank circuit. Five bottom gates were used to define a DQD [Fig. 3(a)]. Bias triangles, the hallmark signature of a DQD, are shown in Fig. 4(a). Due to Coulomb blockade, the source-drain current I_{SD} can only flow through the DQD if at least one quantized energy level of each dot lies within the bias window. Estimating the plunger gate lever arms from the dc bias triangle yields $\alpha_{P1} \approx 0.3$ and $\alpha_{P2} \approx 0.24$ for the gates $P1$ and $P2$, respectively, in line with previous results on bottom-gated devices [48].

Gate reflectometry allows for the measurement of tunneling between the dots (interdot transition) as well as between the dot under the sensor gate and a neighboring reservoir (lead transition). Simultaneously measuring I_{SD} and changes of the reflected rf amplitude $\Delta|S_{21}|$ and phase $\Delta\Phi$ demonstrates the correspondence of the two signals. In the reflectometry signal, the two reservoir transitions (white in $\Delta\Phi$) and the interdot transition (dark purple in $\Delta\Phi$) are clearly visible, appearing similarly in both $\Delta|S_{21}|$ and $\Delta\Phi$ signals. Note that the phase jumps by more than $|\Delta\Phi| = 10°$ at the transitions due to the close-to-perfect matching. In addition, the excited state appears faintly between the reservoir lines in parallel to the interdot transition (orange arrows) and a weak ground-state transition of the lower triangle (purple arrows). The visibility of such features depends intricately on the balance of the tunnel barriers and the resulting tunnel rates in comparison to the resonator frequency. We note the remarkable stability of the quantum dots that can be formed in these NWs, manifesting in very sharp and highly repeatable transitions

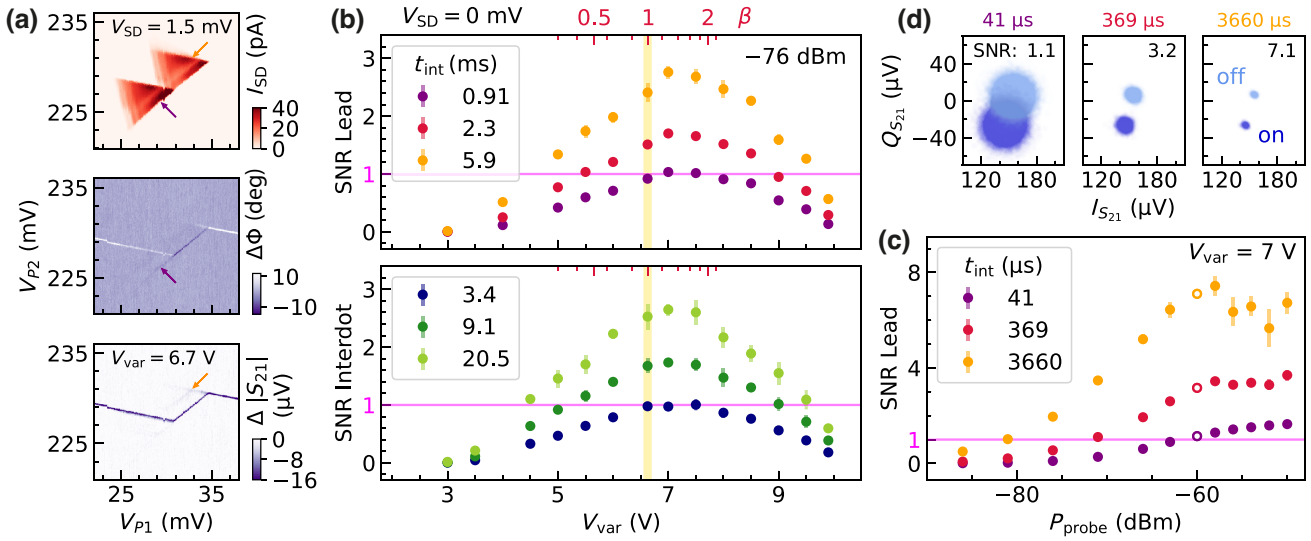

FIG. 4. The sensing of a Ge-Si NW DQD. (a) The charge-stability map of a DQD formed in the Ge-Si core-shell NW, showing a characteristic bias triangle in the dc transport measurement (top). The simultaneously acquired reflectometry data (middle and bottom) feature an interdot line coinciding with the triangle baseline and lead transitions of the right dot with its reservoir. The orange arrows indicate the faintly visible excited-state transition parallel to the baseline and the purple arrows point to the baseline of the lower triangle. (b) Time-domain SNR measurements of similar transitions as in (a), as a function of V_{var} and the integration time t_{int}. Both transition SNRs behave similarly: the highest-SNR regime is shifted to higher V_{var} from the perfect matching (yellow-shaded region). Investigating the interdot line, longer integration times are required to cross the SNR = 1 threshold (pink). Five independent SNR measurements were taken for each V_{var}. The error bars represent one standard deviation. (c) The SNR can be increased by applying higher powers up to approximately $P_{probe} = -58$ dBm, where the signal saturates. (d) Demodulated data measured on (dark blue) and off (light blue) the lead transition at $P_{probe} = -60$ dBm, corresponding to the empty circles in (c).

(see also Appendix D), only sporadically interrupted by a random charge switcher. A large-scale charge-stability map is presented in Appendix D, alongside investigations into the tunability of interdot tunneling using the barrier gate *B*2.

For the following analysis of line shapes and SNRs, we measure at zero source-drain bias to reduce random charge switchers and maximize dispersive signal. We select a lead transition that shows up primarily in the reflected phase and a bright interdot transition near the triangle depicted in Fig. 4(a). The lead-transition line shape can either be dominated by the reservoir hole temperature T_H, exhibiting a $\cosh^{-2}$ dependence on the gate voltage, or by tunnel broadening, which results in a Lorentzian line shape with a tunnel rate γ_L [59]. Fitting the particular transition depicted in Appendix E 1, we find slightly better agreement of the tail region with a $\cosh^{-2}$ relation, hinting toward the temperature-broadened regime, i.e., that $k_B T_H > \hbar\gamma_L$, where k_B is Boltzmann's constant and $\hbar$ is the reduced Planck's constant. We can thus extract $T_H \approx 520 \pm 20$ mK. This temperature is far above the refrigerator temperature, presumably due to microwave irradiation from the cryogenic amplifier. The interdot tunnel coupling, $t_c \approx 22 \pm 5$ μeV, can be extracted fitting the interdot transition shown in Appendix E 2 (for estimates of the quantum capacitances associated with these transitions [59], see Appendix E). Power broadening sets in above $P_{\text{probe}} \approx -60$ dBm for both transitions mentioned, resulting in a reduced signal amplitude and a larger width.

We investigate the impact of impedance matching through time-domain SNR measurements [28] at the two transitions mentioned above. Note that a random charge switcher occurred before we started the SNR measurements, resulting in a lower signal for the interdot transition than in the line-shape investigation. We record time traces of the demodulated reflectometry signal on and off a given charge transition for 2 s with a lock-in time constant TC = 4 μs. The in-phase ($I_{S_{21}}$) and quadrature ($Q_{S_{21}}$) components are then binned for a variable integration time t_{int}. Figure 4(d) depicts the two signals on the I-Q plane for different t_{int}. Comparing the distance of the two signals with the spread of the points estimates the SNR [28].

Figure 4(b) shows the SNRs measured as a function of V_{var}. The need for longer integration at the interdot transition may be due to different tunnel rates. Both transitions exhibit the same qualitative dependence of the SNR on V_{var}. The best SNR is in the slightly overcoupled regime at $V_{\text{var}} \approx 7$ V, where $\beta = 1.28$. In the case of dispersive sensing of a reactive load, the reduction of C_{var} by increasing V_{var} may lead to a higher tank quality factor, thus shifting the optimal sensing configuration away from perfect impedance matching [39]. The observed shift of the tank resonance toward higher frequencies in Fig. 3(b) supports this hypothesis. Evidently, the ability to tune impedance matching is of major importance for SNR optimization. Detuning the varactor by $\Delta V_{\text{var}} = 2$ V from the best operation point, causing a capacitance change of $\Delta C_{\text{var}} = \pm 4$ pF, the SNR drops by up to a factor of approximately 2.

The power dependence of the SNR at the lead transition for $V_{\text{var}} = 7$ V is shown in Fig. 4(c). We find that $P_{\text{probe}} > -60$ dBm causes significant instability of the system, as seen from the higher errors and plateauing of SNR, consistent with the onset of power broadening of the charge transitions (see Appendix E). At $P_{\text{probe}} = -60$ dBm, $t_{\text{int}} = 41$ μs suffices to achieve SNR = 1.1 (for charge-stability maps at low TC, see Appendix D 3).

IV. CONCLUSIONS AND OUTLOOK

In conclusion, we have fabricated and characterized hyperabrupt STO varactors with a tuning range of more than one order of magnitude. These varactors are not affected by moderate magnetic fields and can operate down to low millikelvin temperatures. The small size allows tight integration with other PCB components and scaling in applications with multiple tunable capacitors such as multiplexed readout. We demonstrate the high-frequency functionality of these varactors for gate-dispersive sensing of a Ge-Si core-shell NW hole DQD. Other charge-sensing schemes such as rf single-electron transistors or single-lead sensor dots should equally benefit from optimized impedance matching.

These results open up the possibility for gate-dispersive single-shot readout of spins in Ge-Si core-shell NWs and spin-relaxation measurements. Increasing the sensor gate lever arm as well as the resonator quality factor are important steps to improve the signal further. Expanding the varactor design, more elaborate matching networks including two tunable capacitors in one device may allow for greater flexibility and voltage tunability of the tank resonance frequency. In particular, lowering C_{max} while keeping γ similar should enable impedance matching with high-Q superconducting inductors.

As a circuit element for the nascent field of cryogenic rf engineering, the hyperabrupt varactors can be used in a multitude of applications akin to their room-temperature diode counterparts. Such applications include voltage-controlled oscillators and frequency multipliers, essential components in scaled quantum computation architectures where cryogenic signal generation and manipulation will be necessary to overcome the wiring bottleneck [60]. More immediately, the STO varactors may be used in the ever-growing number of solid-state systems where rf reflectometry techniques at cryogenic temperatures and in magnetic fields are employed, such as hybrid devices featuring superconducting components, for fast thermometry, or in materials science [29].

The data supporting the plots of this paper are available at the Zenodo repository [61].

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R.S.E, T.P., and D.M.Z. conceived of the project and planned the experiments. R.S.E. and D.T. fabricated and measured the STO varactors, with inputs from T.P., while S.S. fabricated, tuned, and operated the NW device. M.J.C. and P.C.K. helped with the NW device fabrication. R.S.E and S.S. integrated the varactor with the NW device and implemented the charge-sensing experiments, with inputs from T.P. The data were analyzed by R.S.E, S.S., D.T., and T.P., with inputs from M.J.C., S.G., A.V.K. and D.M.Z. The NWs were grown by A.L., under the supervision of E.P.A.M.B. The manuscript was written by R.S.E., with inputs from all authors. D.M.Z. supervised the project.

The authors declare no competing interests.

APPENDIX A: DEVICE FABRICATION

1. Varactor fabrication

The STO-ring varactors were optically defined using a Heidelberg μPG laser writer to pattern the structures on a commercially available $SrTiO_3$ (001) wafer (refractive index $n = 2.39$) [41]. The STO chiplets used were 0.5 mm thick and single-side polished, with a TiO_2 termination on the back side, purchased from SurfaceNet. A bilayer of photoresist, consisting of LOR 3A and S1805, was used. The laser writer was operated in pneumatic focusing mode due to the optical transparency at the wavelength of 405 nm. The structures were metallized with 5 nm (65 nm) of Ti (Au). On one 10×10^2 chip, approximately 200 devices were cofabricated and cleaved into smaller segments with 5–15 varactors for wire bonding and PCB integration.

2. Nanowire device fabrication

The QD device featured a set of nine bottom gates with a width of 20 nm and a pitch of 50 nm. The gates were fabricated by electron-beam lithography (EBL) on an intrinsic Si (100) chip with 290 nm of thermal SiO_2. Upon cold development [62], the gates were metallized with 1 nm (9 nm) of Ti (Pd), respectively. In order to electrically insulate the gates from the NW, the gates were covered by an approximately 20-nm-thick layer of HfO_2 grown by atomic layer deposition. A single Ge-Si core-shell NW with a core radius of approximately 10 nm and a shell thickness of approximately 2.5 nm [47] was deterministically placed approximately perpendicular to the nine bottom gates. However, the exact in-plane angle is unknown. Finally, ohmic contacts were patterned by EBL and metallized with 0.3 nm (50 nm) of Ti (Pd) after a 10-s dip in buffered hydrofluoric acid to remove the native SiO_2. The scanning electron micrograph presented in Fig. 3 shows a cofabricated device.

APPENDIX B: REFLECTOMETRY SETUP

A STO varactor with $D = 100\,\mu$m and $w = 50\,\mu$m was integrated into a standard reflectometry setup shown in Fig. 3(a) on a printed circuit board (PCB). Attenuated coaxial cables were used to inject an rf tone at frequency f_{probe} via a directional coupler (Mini-Circuits ZX30-17-5-S+) on the mixing chamber stage into a bias tee on the PCB ($C_D = 87$ pF, with $R_D = 5\,$kΩ). The varactor was operated as a tunable shunt capacitor. A surface-mounted ceramic core inductor ($L = 220 \pm 6$ nH), in series with the parasitic capacitance of a bottom gate of the NW device, formed the tank circuit. From the resonance frequency $f_{\text{res}} = 316.20 \pm 0.05$ MHz, we find a parasitic capacitance $C_p = 1.15 \pm 0.03$ pF. Filtered dc lines were used to provide gate, source-drain bias, and varactor voltages. The reflected signal was amplified at the 4-K stage (Low Noise Factory LNC0.2-3A) and at room temperature (B&Z BZY-00100700). A Zurich Instruments UHFLI lock-in amplifier was used for signal generation and demodulation at room temperature. The dc voltages were provided by a Basel Precision Instruments SP927 digital-to-analog converter and I_{SD} was amplified by a Basel Precision Instruments SP983c current-to-voltage converter and recorded using an Agilent 34410A digital multimeter.

APPENDIX C: VARACTOR PROPERTIES

1. Geometry

The results of COMSOL simulations of the C_{var} dependence on D and w are shown in Table I.

Corresponding measurements at $T = 4$ K are shown in Table II. Note that only devices with $w \leq 60\,\mu$m were fabricated and for small w and D, measurements were often impossible because wire bonding created shorts between the two electrodes. Typical room-temperature capacitances were $\leq$1 pF to 1.5 pF. In a few cases, the room-temperature capacitance was exceeding 10 pF, likely originating from

TABLE I. The simulated C_{var} at $V_{var} = 0$ V, in picofarads.

	w (μm)							
D (μm)	10	20	30	40	50	60	70	80
60	43	36	34	32	31	31	30	30
80	62	52	48	45	43	42	42	40
100	79	68	61	58	56	54	53	52
120	97	86	75	72	68	66	65	63
140	117	102	91	85	81	79	77	75
160	135	120	106	99	94	92	89	86

the dc wiring. These offsets were subtracted from the measured 4-K data presented here. Note that two such cases were excluded from the variability analysis in the main text. The devices used for the variability analysis were fabricated only after the results presented in Tables II and III were analyzed. In order to remove the potential for systematic variations of the varactor geometry due to small variations in the fabrication parameters, the C-V traces recorded for Tables II and III were excluded from the variability analysis. The instances where two nominally identical devices show widely different capacitances at $V_{var} = 0$ V may be due to device damage from lift-off or wire bonding. To assess the tunability range, we present the measured values of C_{var} at $V_{var} = 30$ V in Table III.

The limitations with regard to wire bonding should be easily overcome by adapting the electrode design to include remote designated bond pads. This would make the smaller capacitance values listed in Table III accessible without severe reduction of tunability. Furthermore, $C_{var} \sim 1$ pF at $V_{var} = 0$ V may be reached if the dimensions of the ring are further reduced, which would allow for different tank topologies [36] and tuning of the impedance matching with superconducting inductors.

2. Fitting of the high-tunability range

The two functions in Eqs. (1) and (2) can be used to fit the experimental C-V trace. As shown in Fig. 5, the agreement in the high-tunability regime is better for the power law given in Eq. (2).

TABLE II. The measured C_{var} at $V_{var} = 0$ V, in picofarads.

	w (μm)					
D (μm)	10	20	30	40	50	60
80	···	···	···	···	36	41
100	···	79, 43	52	···	43	46
120	45	···	···	···	···	55, 61
140	···	···	69	···	78	74
160	···	88, 83	80	46	74, 27	73, 97

TABLE III. The measured C_{var} at $V_{var} = 30$ V, in picofarads.

	w (μm)					
D (μm)	10	20	30	40	50	60
80	···	···	···	···	13	12
100	···	24, 18	19	···	14	15
120	20	···	···	···	···	21, 21
140	···	···	25	···	23	25
160	···	26, 72	28	15	18, 13	29, 26

3. Variability of hyperabrupticity

All 13 devices depicted in Fig. 2(a) show hyperabrupt C-V characteristics, as demonstrated in the fits shown in Fig. 6. We find the mean power-law exponent to be $\overline{\gamma} = 0.72 \pm 0.05$.

4. Temperature dependence of matching

Figure 7 shows the tank resonance recorded in the Bluefors setup for a fixed V_{var} using an STO varactor and, for comparison, using a GaAs varactor diode (MACOM MA46H204-1056) [36,38]. The STO varactor has almost no temperature dependence below 4.3 K down to 11 mK. We have verified this robustness to temperature in multiple subsequent thermal cycles. No difference in varactor behavior was observed when tuning the varactor in the kelvin temperature regime and subsequently cooling the refrigerator to the millikelvin regime versus keeping the varactor grounded while cooling to base temperature and tuning it later. In contrast, the GaAs varactor shows a strong dependence on the temperature, which sets in around 53 K, making perfect matching impossible in the millikelvin regime.

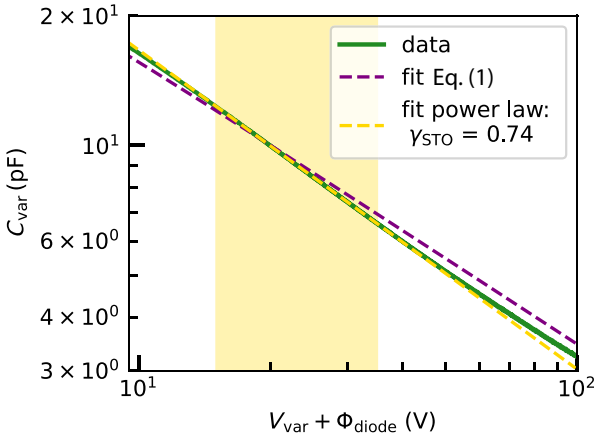

FIG. 5. Fitting the high-tunability regime: both fit functions show good agreement with the experimental data but the power law from Eq. (1) with $\gamma = 0.74$ captures the relevant slope slightly better than Johnson's relation in Eq. (2).

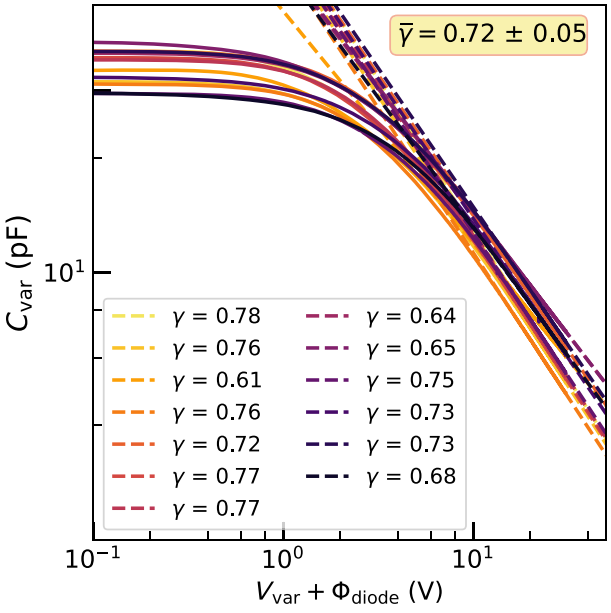

FIG. 6. Fits of C-V traces for all 13 devices from Fig. 2(a).

5. Zero-field anomaly

In the Bluefors LD setup, we observe a shift of the optimal matching condition within a range of $B \approx \pm 50$ mT from $B = 0$ T, as shown in Fig. 8.

The origin of this shift remains elusive. Scans where V_{var} is ramped rather than f_{probe} show a stronger effect. The measurements presented in Fig. 3 show only a minor feature at $B = 0$ T. There are three apparent reasons for this discrepancy:

(1) It is possible that the STO-varactor tunability or the dielectric constant is affected in a different manner

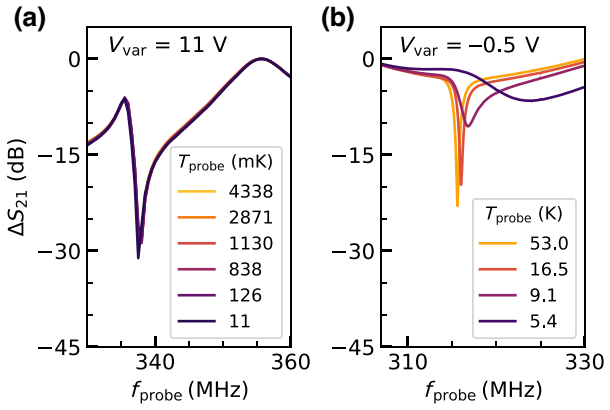

FIG. 7. The temperature dependence of the tank resonance: two subsequent cool downs of the sample PCB without an NW device in the Bluefors setup with (a) an STO-ring varactor and (b) a commercial GaAs varactor used to tune impedance matching.

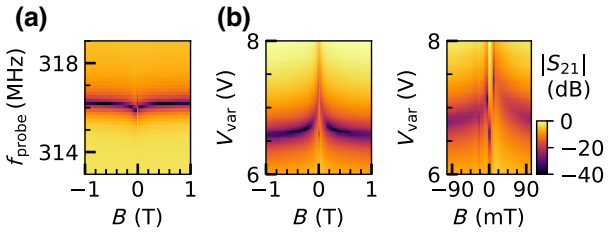

FIG. 8. The zero-field anomaly. (a) The shift of the tank resonance near zero field while V_{var} is kept constant. (b) The effect is much more prominent in a scan at constant f_{probe}, sweeping V_{var}. The right panel is an enlargement of the low-field regime. Note the apparent discontinuities at $B < 10$ mT.

at $T \approx 15$ mK as compared to $T \approx 1.5$ K. Since no such dependence has been mentioned in previous work [41], this appears to be a less likely explanation.

(2) The cryogenic amplifiers used in the two setups were different, namely, a Cosmic Microwave CLTF2 was used in the measurements at 1.5 K (similar to the CLTF1 used in Ref. [41]), but the setup at 15 mK featured a Low Noise Factory LNC0.2-3A amplifier.

(3) The wire bonds used to bond the varactor are made of aluminum, the normal-superconducting transition of which might show up around these fields.

Further experiments are needed to finally exclude or confirm either hypothesis.

APPENDIX D: CHARGE SENSING

1. Charge-stability maps

In Fig. 9, we present a larger scale charge-stability map of the Ge-Si core-shell nanowire DQD. We note that these data were taken at the same barrier gate voltages as the bias triangles presented in the main text. The dc transport signal shown in Fig. 9(a) exhibits multiple bias triangles, corresponding to transport in a DQD. Toward the upper-right quadrant of the graph, there is a region with signatures typical of a triple quantum dot (TQD) system, where the electrochemical potential of the center quantum dot is aligned with that of one of its adjacent outer quantum dots [63]. The presence of both types of transport signatures in this configuration is an indicator of cotunneling involving the center quantum dot, as has previously been observed in similar Ge-Si core-shell nanowire devices [48].

To make the lead and interdot transition lines more visible in the reflected signal, we increase the rf power to $P_{probe} = -35$ dBm, which significantly broadens the transitions in the scan. In this specific charge-stability diagram, we observe strong lead transitions at the regions where the dc transport signatures are those of a DQD, whereas the interdot transitions are more pronounced in the TQD region, indicating a change in the sensed quantum dot tunnel rates.

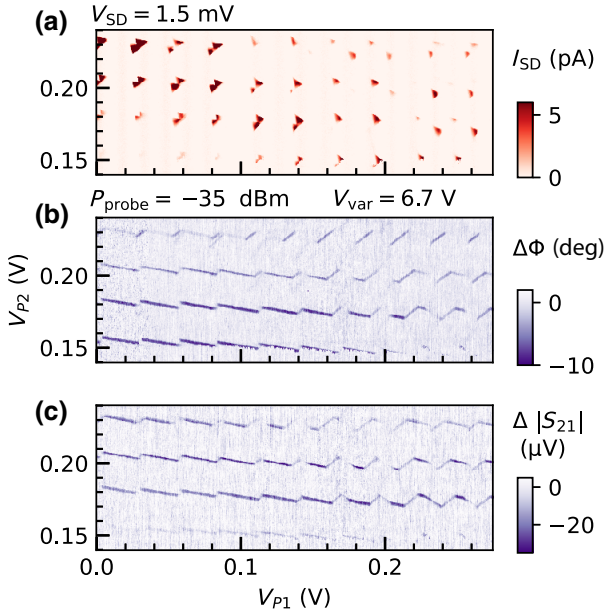

FIG. 9. Dispersive charge sensing over an extended plunger gate-voltage range. (a) The dc transport measurement of the charge-stability diagram in the investigated Ge-Si core-shell nanowire device. (b) The reflected phase $\Delta\Phi$ and (c) the rf amplitude $\Delta|S_{21}|$ measured along with the dc data in (a). Here, we have used a comparably large rf power $P_{\text{probe}} = -35$ dBm, leading to significant power broadening of the lead and interdot transitions and reducing the scan resolution requirements.

2. Tuning the interdot tunnel rate

The strength of the charge-sensing signal is dependent on the tunnel rates of the sensed charge transition. To illustrate this, we show a series of charge-stability maps in Fig. 10, tracking a particular interdot transition at $V_{SD} = 0$ mV for different center-barrier gate voltages V_{B2}. As the voltage applied to the center gate is reduced, the measured interdot transition becomes more faint, until it vanishes fully at $V_{B2} = 1.79$ V. The reduction in barrier voltage exponentially lowers the tunnel barrier, increasing the tunnel rate out of the sensitivity window of our sensor [26].

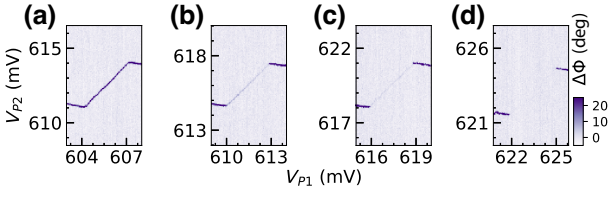

FIG. 10. The dependence on the center-barrier gate voltage V_{B2} = (a) 1.82 V, (b) 1.81 V, (c) 1.8 V, and (d) 1.79 V. The strength of the reflected-phase response $\Delta\Phi$ at the interdot line changes strongly within tens of millivolts being applied to V_{B2}.

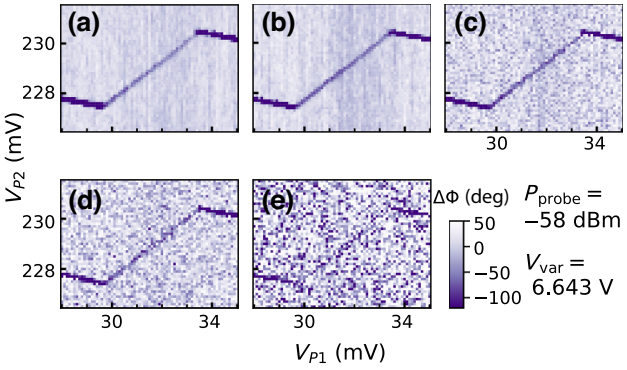

FIG. 11. The dependence on the integration time. The interdot and lead transitions of a selected bias triangle, shown for TC = (a) 80.0 ms, (b) 40.33 ms, (c) 1.33 ms, (d) 13.3 μs, and (e) 1.33 μs. The signal can be recognized down to TC = 1.33 μs.

3. Reducing the lock-in TC

In Fig. 4, we have determined the SNR for the lead and interdot transition of a selected bias triangle as a function of the integration time t_{int}. We plot an enlargement of an interdot transition and adjacent lead transitions at varying TC in Fig. 11 to illustrate the possible measurement speed-up. As TC is decreased, the background noise increases, such that at TC = 1.33 μs the transitions are barely visible.

APPENDIX E: CHARGE-TRANSITION LINE SHAPE

Investigating the line shape and line width of the charge transitions, we can extract several quantum dot parameters. In the case of primarily dispersive signals, i.e., when the transition manifests predominantly as a phase shift $\Delta\Phi$, we can model the signal as a capacitive correction to C_p, the quantum capacitance C_q. The dispersive shift $\Delta\Phi$ is translated to a change in circuit capacitance using the known slope $\delta\Phi/\delta f$ of $\Phi(f_{\text{probe}})$ at resonance for a given V_{var} and the well-known frequency relation for a resonant tank circuit [59]:

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{LC}}, \tag{E1}$$

where f_{res} is the tank resonance frequency, L is the inductance, and C is the capacitance of the resonator. The capacitive correction C_q is then

$$C_q = \left(2\pi\sqrt{L}\Delta\Phi \cdot \frac{\delta\Phi}{\delta f} + \frac{1}{\sqrt{C}}\right)^{-2} - C. \tag{E2}$$

In the following, we present the results of line-shape investigations of the lead transition and the interdot transition also used for the SNR analysis in the main text.

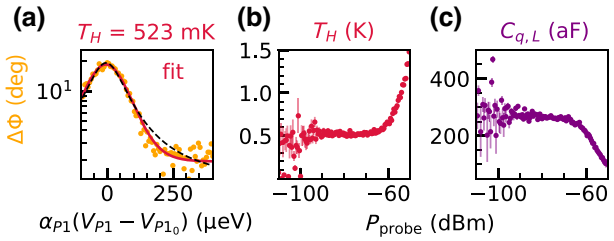

FIG. 12. Fitting the lead-transition line shape. (a) An example line cut (orange) of the lead transition recorded at $P_{probe} = -78$ dBm. The $\cosh^{-2}$ fit (red) captures well the flank of the peak where a Lorentzian model (dashed black) fails. Note the logarithmic y-axis scale and the enlargement on the right flank of the transition to highlight the discrepancy between the two models. (b) The fitted hole temperatures T_H as a function of the probe power. (c) The quantum capacitance of the lead transition $C_{q,L}$, calculated from the maximum phase shift at the charge transition. Power broadening causes a rise in the line width and a reduced resonance height, as observed for $P_{probe} > -60$ dBm.

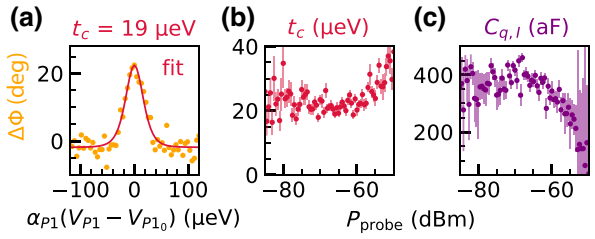

FIG. 13. Fitting the interdot transition line shape. (a) An example line cut (orange) and fit (red) of the lead transition recorded at $P_{probe} = -66$ dBm. (b) The fitted tunnel coupling t_c as a function of the probe power. (c) The quantum capacitance of the interdot transition $C_{q,I}$, calculated from the maximum phase shift at the charge transition. The signal is generally more unstable as compared to the lead transition, causing higher uncertainties.

1. Lead transition

Fitting the lead-transition line shape recorded at $V_{var} = 7$ V, we find temperature broadening to be dominant, $k_B T_H > \hbar\gamma_L$, where k_B denotes Boltzmann's constant, T_H is the hole temperature of the lead, $\hbar$ s the reduced Planck's constant, and γ_L is the lead-dot tunnel rate [59]. We fit the phase signal to

$$\Delta\Phi = \Delta\Phi_{max} \cdot \cosh^{-2}\left(\frac{\alpha_{P1}(V_{P1} - V_{P1_0})}{2k_B T_H}\right). \quad \text{(E3)}$$

Here, $\Delta\Phi_{max}$ is the amplitude of the phase response and V_{P1_0} is the center of the peak along the V_{P1} axis [59].

The dependence of T_H and $\Delta\Phi_{max}$ on the applied rf power P_{probe} shown in Fig. 12 indicates power broadening to set in above $P_{probe} = -60$ dBm. In the regime of flat T_H, we find $T_H \approx 520 \pm 20$ mK and $C_{q,L} = 266 \pm 8$ aF.

2. Interdot transition

The dispersive signal at the interdot transition can be evaluated according to

$$\Delta\Phi = \Phi_0 \cdot t_c^2 \left(\left(\frac{\alpha_{P1}(V_{P1} - V_{P1_0})}{2\sqrt{2}}\right)^2 + t_c^2\right)^{-3/2}, \quad \text{(E4)}$$

where the constant prefactor Φ_0 relates the term for the interdot quantum capacitance $C_{q,I}$ to the dispersive shift and t_c is the interdot tunnel coupling [59]. Note the additional factor $\sqrt{2}$ compared to Ref. [59], translating the quantum dot detuning axis into the plunger gate-voltage axis.

The results of fitting an interdot transition-line cut as a function of P_{probe} are depicted in Fig. 13. In the regime around $P_{probe} = -70$ dBm, $t_c \approx 22 \pm 5$ μeV and $C_{q,I} \approx 380 \pm 70$ aF are plateauing. Lower powers result in too low a signal for reliable fitting, while higher powers cause power broadening, similarly to the case of the lead transition.

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