Superconducting-Semiconducting Voltage-Tunable Qubits in the Third Dimension

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(Received 23 March 2022; revised 21 April 2023; accepted 24 August 2023; published 25 September 2023)

We propose superconducting-semiconducting (super-semi) qubit and coupler designs based on high-quality compact through-silicon vias (TSVs) to overcome challenges introduced by materials and processing required to fabricate high-quality super-semi Josephson junctions. In our designs, an interposer "probe" wafer containing TSVs is used to contact a sample wafer with, e.g., a superconductor-proximitized epitaxially grown germanium quantum well. By utilizing the capacitance of the probe-wafer TSVs, the majority of the electric field in the qubits is pulled away from lossy regions in the semiconducting wafer, such as the graded buffer layers sometimes required for epitaxial growth. Through simulations, we find that the probe wafer can reduce the electric field participation of the qubit in the sample wafer by an order of magnitude for thin substrates and remains small even when the epitaxial-layer thickness approaches 100 μm. We also show how the qubit-coherence improvements achieved via this scheme are extensible to multiqubit systems that have tunable qubit-qubit couplings without magnetic fields. This approach additionally shrinks the on-chip footprint of voltage-tunable superconducting qubits while homogenizing critical wiring structures independent of semiconducting materials, which could aid in accelerating the understanding of super-semi heterostructures in a variety of systems.

DOI: 10.1103/PhysRevApplied.20.034056

I. INTRODUCTION

Solid-state quantum devices based on superconducting Josephson junctions (JJs) have formed the basis for a variety of new quantum information technologies. Circuit quantum electrodynamics (QED) [1], for example, has inspired the development of both qubits and associated control circuitry, such as readout resonators and parametric amplifiers [2–4]. More recently, these techniques and technologies have been increasingly incorporated into semiconductor-based qubits for control, readout, and long-range coupling [5–8]. In parallel, devices with voltage-tunable superconducting-semiconducting (super-semi) junctions [9–12], known as gatemons, have emerged as an interesting avenue both for developing new kinds of devices and for exploring the fundamental physics associated with highly transmissive channels [13,14].

One of the important challenges in this area is to identify and reduce the sources of microwave loss in these new hybrid super-semi devices. An extensive body of research has focused on characterizing and improving dielectric loss at surfaces and in bulk substrates for superconducting qubits [15–21]. Similar work in semiconductor quantum-dot qubits focuses on materials improvements to reduce charge noise [22–25]. The fabrication of gatemon qubits containing super-semi JJs, similar to dot-resonator experiments [26–28], typically involves additional design and process steps to prepare and position the semiconducting element relative to the superconducting components. In particular, maintaining a sufficient quality of the superconducting elements while maintaining the voltage tunability of the super-semi JJ requires the removal of excess lossy material in the case of gatemon devices based on a two-dimensional (2D) electron-hole gas (2DEG-2DHG) [29–32]. These complications can lengthen the iterative process between device fabrication and measurement and may also impede progress toward multiqubit demonstrations.

Flip-chip technology, in which the active components of both a probe wafer and sample wafer are placed facing each other with a small (or zero) separation between wafers, increases the options for materials choices and signal routing while reducing fabrication demands [33,34]. Through-silicon-via (TSV) technology allows for an additional layer of connectivity and signal routing [35] and has recently been integrated into active components used in superconducting control lines and readout [36], as well as qubits [37]. In this work, we propose the use of this

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technology for gatemon qubit and coupler designs with active components on two different wafers. Our proposed architecture can serve to improve the coherence of existing super-semi qubit circuits by reducing electric-field participation in lossy dielectrics intrinsic to epitaxial semiconductor growth. Furthermore, our "probe-wafer" approach positions the majority of wiring structures on a separate chip from the super-semi JJs, facilitating reuse of the same wiring layer to investigate different semiconductor-heterostructure JJs in an otherwise identical microwave environment.

II. DEVICE DESCRIPTION

A schematic diagram of the device, which consists of "probe" and "sample" wafers in a flip-chip configuration, is shown in Fig. 1. The silicon probe wafer incorporates superconducting TSVs, which connect device components on its front and back surfaces. Separation between the two wafers is defined by etched silicon spacers on the edges of the probe wafer and has been demonstrated to have a separation accuracy of < 100 nm, which enables reproducible gate placement over sample wafer and range of chip separations from 500 nm up to 10 μm [38]. The sample and probe wafers are connected via superconducting indium bump bonds, which have been previously demonstrated to have sub-$\mu\Omega$ resistance and to be compatible for use in superconducting qubits [39]. A crucial element of this scheme is that the majority of the qubit electric field energy is confined to the bulk of the (high-quality) probe wafer and away from both the device wafer and the lossy metal-air interfaces. This distinguishes the present proposal from a recent work [40] that made use of flip-chip technology, in which the pads of a transmon qubit were bump bonded across two wafers.

For a concrete example of the advantages of this scheme, we consider the sample wafer to be an epitaxially grown Si-Ge heterostructure on the surface of a high-resistivity silicon substrate [41,42]. An epitaxially grown Al capping layer is assumed to provide a low-transparency connection between the Si-Ge layers and the Cooper pairs in the aluminum, which proximitizes the germanium quantum well at low temperatures [43]. Additionally, a thin layer of TiN can be deposited on top of the aluminum [omitted from the schematic in Fig. 1 (a) for clarity] to prevent lossy intermetallic alloys from forming between the indium superconducting bumps and the proximitization layer [39]. Electron-beam and photolithography steps are used to pattern and etch the TiN and aluminum layers as well as define the gap, which will be used to form the voltage-tunable JJ. The tuning-gate electrode is patterned on the backside of the probe wafer and aligned over the gap in the sample-wafer aluminum, depicted in a top-down schematic in Fig. 1. Although the aluminum gap will be approximately 100 nm in length (the short-junction limit

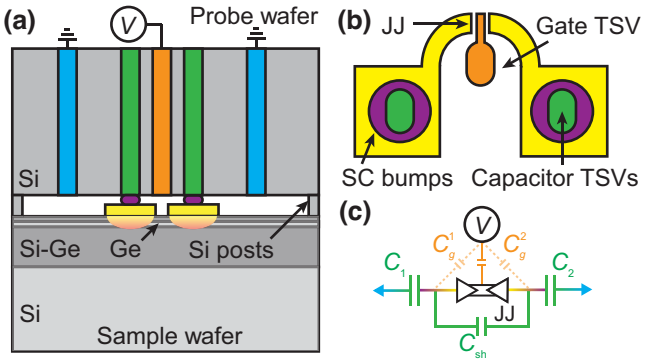

FIG. 1. The probe-wafer gatemon qubit: a schematic diagram of the TSV probe wafer bonded to the sample wafer via superconducting bump bonds (purple). The sample wafer consists of epitaxially grown aluminum (yellow), capped with a TiN layer (same area as the bumps) that is etched to leave a small gap of a proximitized germanium quantum well between the capacitor pads. The probe wafer contains ground TSVs (blue) for shielding and capacitors formed with two additional TSVs (green). (b) A top-down diagram of the qubit metal on the sample wafer (yellow), where the middle TSV (orange) is positioned above the etched gap in the aluminum and used to tune the transmission through the gate-biased JJ. (c) A circuit diagram for the three-dimensional (3D) gatemon device, where the colored wires and capacitors correspond to the schematic shown in (a), with the voltage-tunable JJ shown in black.

[44]), the tuning-gate electrode can be several microns wide to accommodate a small misalignment between the sample and probe wafers. The total capacitance of the qubit comes from a combination of the sample-wafer contact pads and the probe-wafer–TSV capacitors, which sets the charging energy, $E_C = e^2/2C_\Sigma$, where $C_\Sigma = C_{\rm sh} + (1/(C_1 + C_g^1) + 1/(C_2 + C_g^2))^{-1}$, in which $C_{\rm sh}$ is the capacitance between the TSVs. To bias the junction, the capacitance between the tuning-gate and capacitor TSVs must be much less than the TSV capacitance to ground, i.e., $C_g^1, C_g^2 \ll C_1, C_2$. The electrode used to tune the Josephson energy E_J (via the chemical potential of the quantum well) is a TSV in the probe wafer centered directly above the aluminum gap on the sample wafer [Fig. 1(b)]. When the gatemon is in the transmon regime, $E_J/E_C \gg 1$, the qubit frequency is approximated as $\omega/2\pi \approx \sqrt{8E_JE_C} - E_C$ and is adjustable *in situ* via changes to the gate electrode. The symmetry of the tuning-gate electrode between the capacitor pads suppresses its coupling to the (differential) qubit degree of freedom, thereby minimizing its contribution to qubit relaxation, a worked example with further detail is provided in Appendix A. We note that the present choice of Si-Ge for the sample wafer is only made for concreteness, and the corresponding analysis can easily be done for other proximitized 2D materials such as InGaAs [45].

An additional benefit of the three-dimensional (3D) TSV setup is a substantial reduction of the planar footprint of

the qubit, since the majority of the qubit shunt capacitance, C_{sh}, is associated with the vertically oriented TSVs contained in the probe wafer. In the device design presented here, the footprint of the gatemon is reduced by over an order of magnitude, from 0.18 mm^2 to 0.014 mm^2, while maintaining a high quality factor (Q). In addition, the vertically oriented capacitor in the probe wafer can be much more effectively shielded electrostatically (using TSV-based via structures) than a planar design, allowing adjacent qubits to be placed in closer proximity without increasing parasitic couplings.

III. DIELECTRIC LOSS

Dielectric loss plays a dominant role in limiting the quality factors and lifetimes of superconducting resonators and qubits. The excited-state lifetime, T_1, of a transmon qubit [46] with frequency ω can be approximated as

$$\frac{1}{T_1} = \frac{\omega}{Q} = \omega \sum_i \frac{P_i}{Q_i} + \Gamma_0, \tag{1}$$

where the decay rate has been broken into a sum of terms associated with dielectric losses in different materials and interfaces (each with a fractional participation of P_i and quality factor Q_i) and a term Γ_0 that captures the decay rate due to all other mechanisms (such as quasiparticle tunneling across the JJ [47] and damping due to coupling to the measurement circuitry [48,49]). Each P_i can be calculated via finite-element simulation, by defining voltages on the qubit electrodes, solving for the dc electric field across the device, and integrating the field in each of different dielectric volumes,

$$P_i = \int_{V_i} \varepsilon_i |E_i|^2 / U_{\text{tot}}, \tag{2}$$

where ε_i is the dielectric constant of a region and U_{tot} is the total energy stored in the system. We simulate the electric field distribution over four volumes: the two Si substrates, the Si-Ge epitaxial layers, a 5-nm-thick oxide layer on top of the qubit and ground plane, and the vacuum between the two wafers (here assumed to be separated by 4 μm). Additional details regarding the simulations are provided in Appendix B. For comparison, we also simulate a traditional planar gatemon design. We approximate the multilayer epitaxial quantum well heterostructure as a uniform block of $Si_{0.8}Ge_{0.2}$ with a dielectric constant of $\varepsilon_r = 12.6$ and calculate the $P_{\text{Si-Ge}}$ as a function of the Si-Ge–layer thickness (Fig. 2). To verify that the dc electric field accurately captures the field participation for the planar and 3D geometries, we add a lumped-element inductor between the qubit capacitors, find the eigenmodes of the system, and calculate $P_{\text{Si-Ge}}$ near the qubit frequency of 4–5 GHz. The data from the eigenmode solver (green and red stars in Fig. 2) are in good agreement with the dc field solutions, indicating that for these qubit geometries, use of the simpler electrostatic solver is sufficient to accurately model the field participation. For Si-Ge layers < 10 μm, $P_{\text{Si-Ge}}$ is an order of magnitude smaller for the 3D TSV-based devices compared to the planar gatemons and for Si-Ge thicknesses above 10 μm, $P_{\text{Si-Ge}}$ saturates at around 5%.

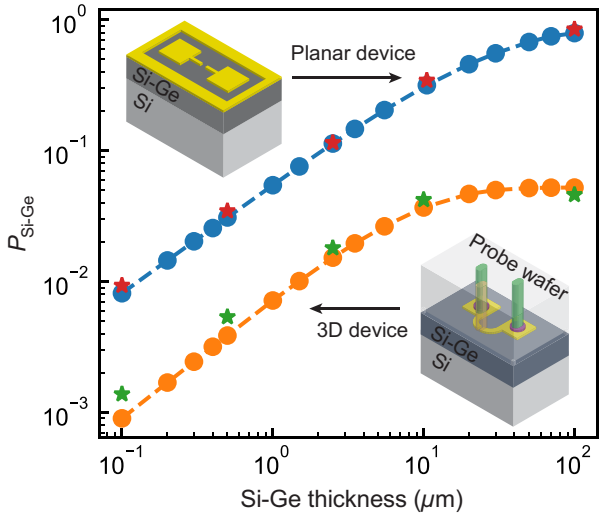

FIG. 2. The field distribution and size improvements in the probe wafer. The energy participation in the Si-Ge layer as a function of the Si-Ge–layer thickness for an existing planar gatemon device (upper-left schematic) and for the proposed 3D TSV based device (lower-right schematic). The planar gatemon capacitor pads are 300 μm square with 50-μm spacing between the pads and ground (inset schematics not to scale). The TSV gatemon planar extent can be reduced in size by a factor of 10, to 30 μm square, while maintaining the same shunt capacitance of the planar device of $C_{sh} = 75$ fF. The star icons are the $P_{\text{Si-Ge}}$ values obtained via an eigenmode solver at the qubit frequency (see main text).

A reduction in $P_{\text{Si-Ge}}$ is particularly advantageous when the microwave loss in the Si-Ge epitaxial layers, expressed as the loss tangent $\tan\delta_{\text{Si-Ge}} \equiv 1/Q_{\text{Si-Ge}}$, is large compared to that of bulk Si, where $\tan\delta_{\text{Si}} \approx 2 \times 10^{-7}$ [20]. The loss in bulk Si-Ge is believed to arise from threading dislocations originating at the interface between the buffer layer and the epitaxial heterostructure grown on the surface; however, its exact origin is a matter of ongoing study [45]. Using the relationship of the participation-weighted Q values described in Eq. (1), the calculated participation factors for Si-Ge from Fig. 2, and a recently reported value of $\tan\delta_{\text{Si-Ge}} = 1.6 \times 10^{-5}$ [50], we can compare the total Q values for a planar device to a 3D integrated device. As the specific details of the geometry, metallization, and fabrication processes of TSVs are device specific and might not be known *a priori*, we will approximate Q for the 3D TSV design (Q_{TSV}) as the participation-weighted sum of all the

surface and bulk losses intrinsic to the TSV structure and treat the weighted Q_{TSV} as a variable. A recent demonstration of a transmon qubit containing a TSV capacitor has measured $Q_{\mathrm{TSV}} = 750 \times 10^3$ [37], which can be used to inform the comparison with the fully planar device constructed entirely on the sample wafer. For losses related to the superconducting bump bonds, we note that recent measurements have demonstrated a connection between two wafers using indium bumps with $R < 2\ \mu\Omega$ [39]. Modeling this connection as a resistor in series with an $L = 15$ nH Josephson inductance, both placed in parallel with a qubit capacitance of $C_\Sigma = 75$ fF, we calculate $Q > 10$ M, which can be omitted from the overall loss calculation, as it is an order of magnitude larger than the substrate loss.

Figure 3 shows the estimated T_1 times of the 3D TSV device, with $\omega/2\pi = 4.75$ GHz, as a function of Q_{TSV}. Here, a simplifying assumption has been made that the loss in the Si-Ge layers is uniform for all thicknesses of Si-Ge. In future experimental work, measurements of the loss in these devices will elucidate the degree to which this assumption is valid. For thick Si-Ge layers, the 3D design can yield an already significant improvement at the currently achievable Q_{TSV}, with the T_1 values improved by 30% for a 2.5-μm-thick Si-Ge layer and by over a factor of 4 for 30-μm-thick Si-Ge (comparison shown at the black line in Fig. 3). It is worth noting that for very thin epitaxial layers of Si-Ge, the T_1 of a fully planar device (blue dashed line) is improved by the addition of the probe wafer only when $Q_{\mathrm{TSV}} > 2$M. This can be understood as follows. In planar devices with very thin Si-Ge epitaxial layers, $P_{\mathrm{Si\text{-}Ge}}$ is limited to a few percent (blue and red points near to the left-hand side of Fig. 2) and the majority of the electric field is in the Si below the Si-Ge, with $\tan\delta_{\mathrm{Si}} \approx 2 \times 10^{-7}$. In the 3D design, although $P_{\mathrm{Si\text{-}Ge}}$ has been reduced by an order of magnitude compared to the planar equivalent, if it is the case that Q_{TSV} is lower than the sum of the loss from the Si-Ge layer and Si substrate in the sample wafers, then the planar design will have a greater T_1 than the 3D design, as would be the case for very thin and/or low-loss Si-Ge layers and very low Q_{TSV}. Although the use of very thin epitaxial layers could in principle improve T_1, devices that require thick quantum wells or buffer layers, or need to be constructed from particularly low-Q semiconductors such as InP [51], would necessarily be in the lossy "bulk" regime.

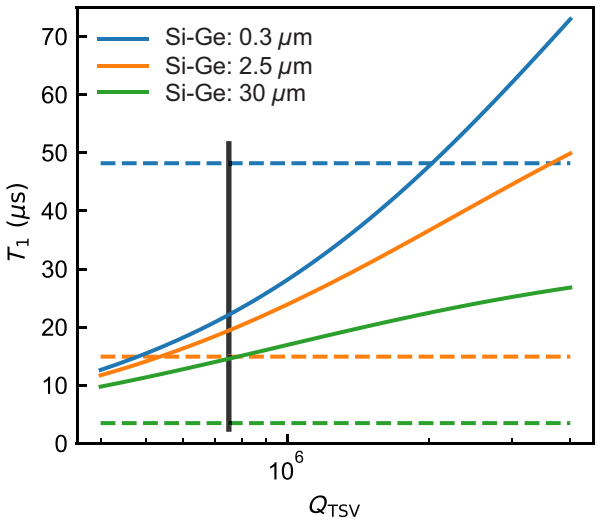

FIG. 3. The projected gatemon T_1 in the probe-wafer geometry. The calculated T_1 as a function of Q_{TSV}, for three values of the Si-Ge thickness corresponding to thin, intermediate, and thick layers, all assumed to have a uniform $\tan\delta_{\mathrm{Si\text{-}Ge}} = 1.6 \times 10^{-5}$. The dashed lines indicate the estimated T_1 values of a fully planar device constructed on a substrate for each of the three different Si-Ge thicknesses. The increasing T_1 for planar devices with decreasing Si-Ge thickness is a reflection of the reduction in $P_{\mathrm{Si\text{-}Ge}}$. The 30-$\mu$m-thick layer (green) is in the "bulk" regime, where the change in $P_{\mathrm{Si\text{-}Ge}}$ is small and is decreasing as the Si-Ge thickness is increased (the right-hand side of Fig. 2). The bulk regime is where the most significant improvement is expected over existing planar designs. The 2.5-μm- (orange) and 0.3-μm- (blue) thick Si-Ge layers are similar to those that have been used in other 2DEG gatemon devices [45]. The solid-black vertical line is the reported value of Q_{TSV} from Ref. [37].

IV. MULTIQUBIT DEVICES

While we have so far motivated our 3D TSV design because of its potential for reducing loss and minimizing processing of the sample wafer containing the semiconductor heterostructure, the design also supports a two-qubit coupling scheme based on voltage-controlled tunable couplers. Tunable coupling between qubits has the potential for higher on-off ratios of interaction between qubits compared to systems based on fixed two-qubit coupling and microwave-drive-activated gates [52]. This kind of quasistatic controllable coupling between superconducting qubits is typically achieved by modulating the magnetic flux bias applied to a nonlinear coupler circuit [such as a superconducting quantum interference device (SQUID)], thereby changing the effective coupling strength between qubits [53,54]. To minimize the resulting additional susceptibility to flux noise via the coupler circuits, they are typically designed so that a relatively large difference in coupler flux bias separates their on and off states. However, as the circuit size and the number of qubits and couplers increases, it becomes increasingly challenging to independently control these large flux-bias signals, due to the nonlinearity and nonlocality of Meissner screening of these signals by surrounding superconducting circuit elements. Static power dissipation from flux control lines also poses a considerable challenge as the qubit count on a chip increases. One recent study found that up to 50% of the total power dissipated, about 0.1 μW per line, on the mixing chamber of a dilution refrigerator results from the dc currents used to set flux idling points for qubits

[55]. As no current flows on the gate-voltage control when idle, using a voltage control immediately gives a factor-of-2 improvement in power dissipation in the experimental setup.

These difficulties could, in principle, be avoided if it was possible to use *voltage-sensitive* coupler circuits, since electrostatic shielding for reduction of parasitic capacitive coupling is much better controlled and is extensible. In fact, proposals for electrostatically tunable couplers exist back to the early days of Cooper-pair box qubits [56]. However, these kinds of circuits were quickly found to be impractical experimentally due to the ubiquitous presence of nonstationary low-frequency electric noise, in the form of slowly drifting offset charges and quasiparticle-tunneling events [57–59]. Gatemon qubits present a new opportunity to revisit these schemes, since their voltage tunability is of an entirely different semiconducting character, and could be dominated by less severe noise processes. The proposed TSV-based 3D design presented here gives a natural platform for realizing such schemes.

We propose constructing the coupler and qubits out of the TSV-based gatemons in the transmon regime. This multiqubit system can be described by the following Hamiltonian [53,60,61]:

$$H/h = \sum_{i=1,2,c} \left(\omega_i a_i^\dagger a_i + \frac{\alpha_i}{2} a_i^\dagger a_i^\dagger a_i a_i\right) + \sum_{i<j} g_{ij}\,(a_i - a_i^\dagger)(a_j - a_j^\dagger), \tag{3}$$

where ω_i and α_i are the qubit and coupler frequencies and anharmonicities, respectively, g_{ij} is the coupling strength between the qubits and the coupler, and $a_i^\dagger$ (a_i) are the creation (annihilation) operators for each qubit and coupler. A schematic of the multiqubit system is shown in Fig. 4. Although this device layout can be used with most types of coupling schemes, we highlight the system similar to Ref. [60] in which two differential transmons have been coupled via a tunable coupler with a frequency lower than those of the two qubits. We note that an in-depth theoretical treatment of coupling strengths and fidelities for several transmon-gatemon systems has been previously reported [62] and that here, we explore the particular transmon qubit-gatemon coupler system to understand the coherence impact on the transmons from the reduced gatemon coherence. The qubit-qubit interaction is of the form ZZ, with an interaction strength $\zeta = \omega_{11} - \omega_{10} - \omega_{01} + \omega_{00}$, where ω_{ij} are the frequencies of each qubit in the coupled system. The Hamiltonian in Eq. (3) is numerically diagonalized to find the qubit and coupler frequencies as well as the magnitude of ζ. In this treatment, the coupler is assumed to remain in its ground state.

A short voltage pulse on the gate TSV adjusts the tunable-coupler frequency ω_c and changes the magnitude of ζ to perform a controlled-Z gate between the two qubits. As the coupler frequency is adjusted by the change in junction transparency, a local effect on the scale of the junction dimensions, crosstalk from adjacent coupler pulses is expected to be substantially reduced compared to flux-based control schemes, which typically have crosstalk on the order of approximately 10% [63]. Figure 5 shows ζ versus ω_c for three different sets of couplings chosen to have similar idle frequencies.

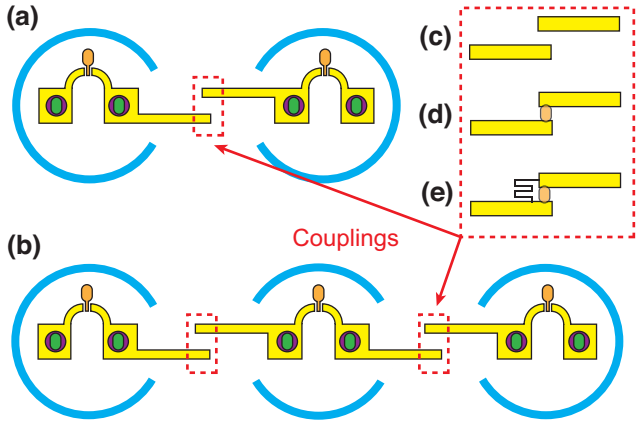

FIG. 4. An extension to a multiqubit system. (a),(b) Schematics for multiqubit systems directly coupled (a) or coupled via an intermediate coupler (b). (c)–(e) Both schemes are compatible with (c) capacitive, (d) inductive, or (e) tunable inductive coupling. As in the single-qubit case, neighboring qubits are shielded with a fence of TSVs (blue rings) to reduce parasitic capacitance between non-nearest-neighbor qubits.

One potential area of concern of this coupling scheme is the deleterious effects of gate noise, which changes ω_c and will shift the dressed-qubit frequencies ω_{qi}, causing a reduction in their T_2, similar to what has been noted in flux-based tunable-coupling schemes [64]. In a hybrid system where the coupler is fabricated with a gatemon and the qubits are transmons with Al/AlO_x JJs, we can quantify the impact of this gate-voltage coupler noise on qubit coherence by observing the dressed-qubit frequencies as a function of the strength of the gate noise. For each of the parameter sets shown in Fig. 5, ω_c is set such that $\zeta = 0$, with an additional offset from the idle point, ϵ. For simplicity, we assume that the noise on ω_c is quasistatic (constant during the approximately 100 ns of a gate pulse but variable over many experimental runs) and we choose ϵ from a zero-mean Gaussian distribution with a width of $\sigma_{\omega c}$. We solve Eq. (3) for 1000 different values of ϵ for a fixed value of $\sigma_{\omega c}$ [Fig. 5(c)] to obtain the variation in dressed-qubit frequencies. As the magnitude of the gate-voltage noise is not something that is known *a priori*, we repeat this simulation for different $\sigma_{\omega c}$ [Fig. 5(d)]. For a gatemon coupler coherence less than 1 μs, corresponding to $\sigma_{\omega c} \simeq 0.3$ MHz, the coherence limit via this dephasing mechanism for the qubits is still above 100 μs. This is

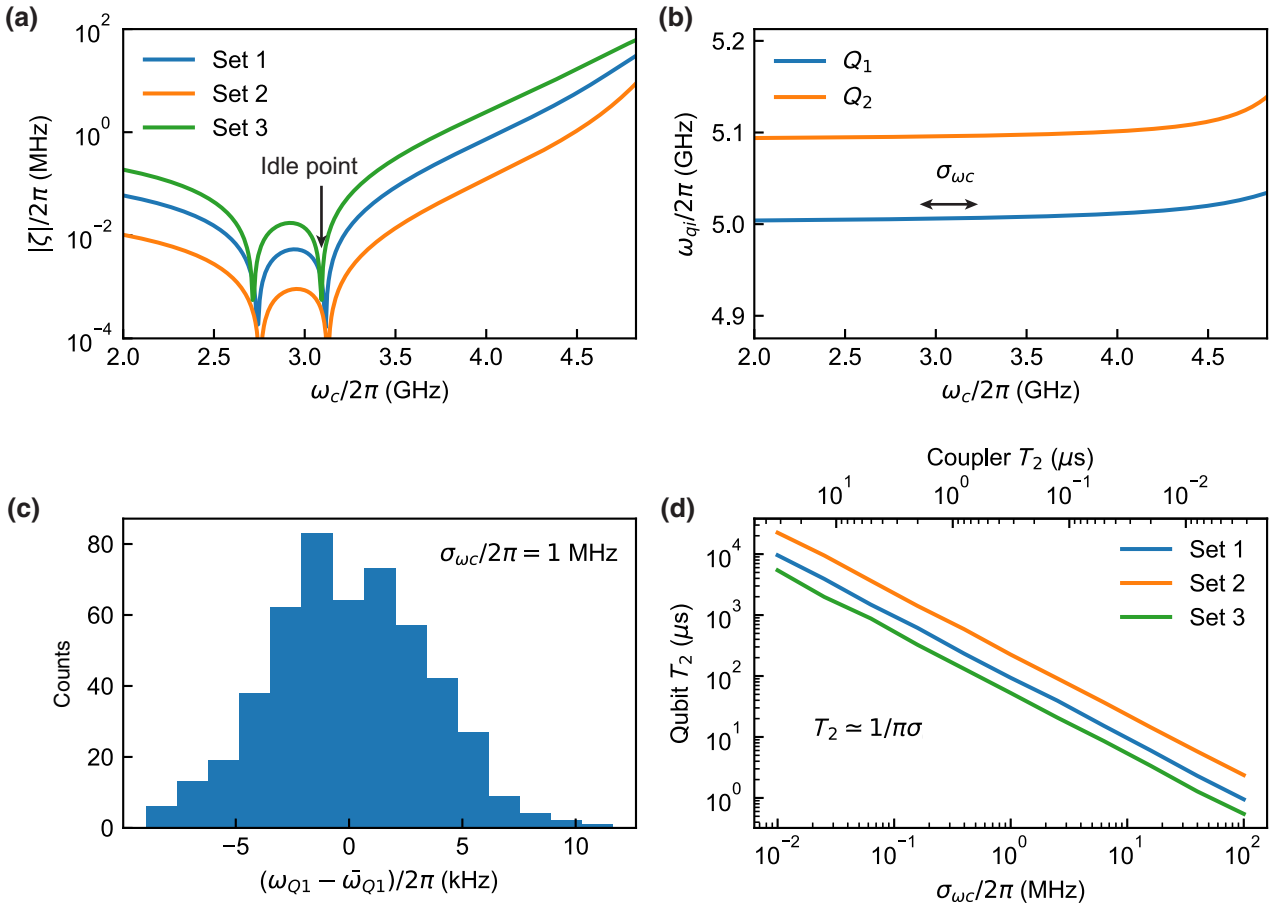

FIG. 5. The gatemon-tunable-coupler compatibility in multiqubit systems: the simulation of two qubits coupled via a tunable coupler. (a) The effective ZZ coupling strength between the qubits as a function of the coupler frequency for three parameter sets, $g_{1c}/2\pi = g_{2c}/2\pi = 110$ MHz, $g_{12}/2\pi = -6$ MHz (set 1), $g_{1c}/2\pi = g_{2c}/2\pi = 70$ MHz, $g_{12}/2\pi = -2.5$ MHz (set 2), and $g_{1c}/2\pi = g_{2c}/2\pi = 150$ MHz, $g_{12}/2\pi = -11$ MHz (set 3), with $\alpha_{1,2,c}/2\pi = -260$ MHz in all cases. These parameters are chosen such that the coupler idle frequency is similar for the three parameter sets. (b) The dressed-qubit frequencies for the two qubits versus the coupler frequency. The finite derivative of $d\omega_q/d\omega_c$ implies that changes to the coupler frequency, $\sigma_{\omega c}$, though charge noise or gate-voltage fluctuations move the qubit frequencies. (c) A histogram of the difference between the noise-free and noisy dressed-qubit frequencies for 1000 different values of ϵ for a $\sigma_{\omega c}/2\pi = 1$ MHz. (d) This can then be converted to a T_2 for the qubits based on the strength of the noise in the coupler.

encouraging, as coherence times much greater than 1 μs have already been demonstrated in gatemon devices [10], indicating that this scheme is compatible with existing devices. We note that as the strength of coupling between the qubits and resonators is increased, there is a reduction in the qubit T_2, which implies that a balance will have to be achieved between strong coupling for fast two-qubit gates, but not so strong as to significantly impact the qubit-coherence times.

V. CONCLUSIONS

We have proposed a type of super-semi qubit device formed across two wafers. This design allows for minimal processing of the sample wafer as well as an improvement to the qubit coherence for very thick and lossy sample substrates. This scheme is also compatible with a high-coherence magnetic field-free multiqubit coupling architecture. Although we have considered a particular use case of the TSV probe wafer for qubits, the modular nature of probe makes it compatible as a tool for studying other systems such as layered 2D materials [65], in which processing of the sample wafer could be drastically simplified.

ACKNOWLEDGMENTS

We would like to thank all members of the LPS Qubit Collaboratory, especially Christopher Richardson, Emily Toomey, Hugh Churchill, Ben Palmer, Kevin Osborn, Rusko Ruskov, and Utkan Güngördü for useful discussions. We would also like to thank William Oliver, David

Kim, Mollie Schwartz, Donna Yost, and Wayne Woods for valuable discussions related to TSV fabrication and design. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of the U.S. government. This research was funded in part by the Undersecretary of Defense for Research & Engineering under Air Force Contract No. FA8721-05-C-0002. This work was funded under the LPS Qubit Collaboratory.

APPENDIX A: EFFECTIVE CAPACITANCE OF A SYMMETRIC GATE

As mentioned in the main text, it is advantageous to have the gate electrode that tunes the Josephson energy of the gatemon be symmetric with respect to the two capacitor TSVs. When an asymmetry exists, the qubit mode couples to the gate electrode and can emit energy into the bias line via the Purcell effect, which in the limit of weak coupling strength to the gate is given by

$$T_1 \cong \frac{C_\Sigma}{\omega^2 Z_0 C_{\text{eff}}^2}, \tag{A1}$$

where C_Σ is the qubit capacitance, Z_0 is the impedance of the voltage bias line (taken here to be 50 Ω), ω is the qubit frequency, and C_{eff} is the effective capacitance to the bias line [49]. From the circuit diagram in Fig. 1(c), we can write the expression for C_{eff}:

$$C_{\text{eff}} = \frac{C_1 C_g^2 - C_2 C_g^1}{C_1 + C_2 + C_g^1 + C_g^2}. \tag{A2}$$

Using the capacitance values extracted from the loss simulations presented in the main text, of $C_1 = C_2 = 70$ fF, $C_g^1 = C_g^2 = 0.5$ fF $C_{\text{sh}} = 40$ fF, and $\omega/2\pi = 4.5$ GHz, we find that the Purcell-limited T_1 exceeds 1 ms for gate asymmetries of 20%, i.e., if $C_g^2 = 0.5 \pm 0.1$ fF. In terms of the physical misalignment, this corresponds to a (3–4)-μm displacement of the gate line away from the symmetry axis for a 60-μm spacing between the qubit capacitors.

APPENDIX B: SIMULATION DETAILS

The simulation data in the main text were generated using ANSYS ELECTRONICS DESKTOP MAXWELL (dc) and HFSS (high-frequency eigenmode solver). For the dc electric field simulations, voltages are applied to each metal conductor—i.e., ground, qubit capacitor pad 1, qubit capacitor pad 2, etc.—and the resulting electric fields are integrated over each dielectric volume in order to extract the participations. To ensure accurate simulations, the convergence criteria are set such that the change in the total energy of the system between successive iterations is less than 0.5%. We use a chip size of 1000 × 1000 μm, which is much larger than the active portion of the qubit, to limit the effects of the chip boundary or finite-size ground plane. For the eigenmode simulations, a lumped-element 15-nH inductor is added between the capacitor pads on the sample wafer to approximate the linear inductance of the JJ and solve for the system eigenmode iteratively until the frequency is changing by less than 0.5% per pass. The good agreement between the electrostatic and eigenmode solvers over several orders of magnitudes of $P_{\text{Si-Ge}}$ gives us reasonable confidence in the convergence of the solutions. As mentioned in the main text, a 5-nm layer of lossy AlO_x is included on top of the qubit to model loss from the metal-to-air interface. We verify that the eigenmode solver is accurately capturing the effects of this layer by comparing the Q of a device with a 5-nm oxide layer with a loss tangent of $\tan\delta_{MA} = 3.3 \times 10^{-3}$ [20] with a device where the layer is 50 nm thick with a loss tangent of $\tan\delta_{MA} = 3.3 \times 10^{-4}$ and find that the values of Q are indistinguishable. In the limit that this increased dielectric thickness is much smaller than the size of all the other gaps and substrate thicknesses, then this will be a small perturbation on the electric field profile.

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