Complementary Two-Dimensional Vertical Transistors through Lamination with a van der Waals Metal

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Vertical transistors, with the channel material sandwiched between graphene and metal electrodes, are promising for the development of next-generation electronic devices. However, realizing complementary transport in two-dimensional vertical transistors is challenging due to the significant disorder and severe Fermi-level pinning effects at the metal-semiconductor interface caused by conventional metallization. Here, we report complementary vertical transistors in graphene/WSe_2/van der Waals metal heterostructures. In this device, the van der Waals metal retains the pristine nature of atomically thin WSe_2, minimizing the Fermi-level-pinning effect at the metal-WSe_2 interface. Thus, the barrier height and the type of majority carrier can be simply controlled by the metal work function. Based on this approach, we achieve *n*- and *p*-type WSe_2 vertical transistors by laminating Ag and Pt as van der Waals contact metals, respectively. Moreover, with highly controllable device polarities, we demonstrate a complementary inverter by integrating two vertical transistors with different polarities. Our work not only enables complementary two-dimensional vertical transistors, but also provides a promising strategy for controlling the polarity of carriers in vertical heterostructures.

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I. INTRODUCTION

Intensive research into two-dimensional (2D) materials and van der Waals (vdW) heterostructures has facilitated the development of graphene-based vertical transistors, in which the channel material is sandwiched between graphene and metal electrodes [1–14]. Within this device geometry, the tunable Fermi energy of graphene enables efficient modulation of carrier injection and transport across the graphene-channel junction. More importantly, the channel length in vertical transistors is simply determined by the semiconductor thickness and can be scaled down to the sub-10-nm regime for high-performance devices [5,10,14] and further enable multiple vertical stacking for three-dimensional integration [13,15,16]. Following this device concept, vertical transistors with various semiconductors (such as 2D materials [3,5,10,14], bulk crystals [2,4,7,12], and thin-film organics [6,8,9]) have been fabricated. In particular, abundant 2D materials enrich vertical transistors with exceptional properties for low-power [4,8], high-speed [9,12], and flexible operation [3,7].

However, with nearly a decade of intensive efforts, 2D vertical transistors demonstrate only single-polarity transport (either *n* type or *p* type), and complementary electrical behavior has not been realized so far. The fundamental challenge for this is the ultrathin vertical structure (∼10 nm), where the contact interface is actually the whole device and controls the overall electrical behavior. In terms of the metal-2D contact, conventional metallization methods for vertical transistors (e.g., *e*-beam or thermal evaporation) are general "high-energy" processes involving hot-atom and cluster bombardment, resulting in interface damage, metal diffusion into the channel material, and surface states at the metal-semiconductor junction [17,18]. Such effects not only limit further scaling down the vertical channel length due to the direct leakage current within such a short length (sub-10 nm) [5,14,19], but also lead to severe Fermi-level-pinning effects at the vertical metal-2D interface [17,20–23]. Therefore, the Fermi level is fixed in the middle of the gap and only one type of majority carrier can be injected, depending on the height difference between the electron and hole barriers. Hence, complementary transport behavior has not yet been realized in 2D vertical transistors, greatly limiting the achievement of complementary logic functions and practical applications of 2D vertical transistors.

Here, we report the realization of complementary 2D vertical transistors in graphene/WSe_2/metal structures using the vdW-metal lamination process. The conventional fabrication-induced defects and surface states are

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largely minimized by mechanically laminating metal electrodes onto the surface of the 2D material, leading to a Fermi-level-pinning-free interface. Within this device, the contact barrier and the majority carrier type can be simply controlled by the metal work function. Based on this approach, we realize *n*- and *p*-type WSe_2 vertical transistors by laminating Ag and Pt as vdW contact metals, respectively. Furthermore, these complementary 2D vertical transistors can be connected, leading to a functional logic inverter using the same channel material. Our work not only enables complementary transport in 2D vertical transistors, but also provides a promising approach for controlling carrier polarity in vertical heterostructures.

II. RESULTS AND DISCUSSION

Figure 1(a) illustrates the schematic structure of our 2D vertical transistor. In this device, graphene and vdW metal with proper work functions act as bottom and top contacts, respectively, for the WSe_2 channels. As shown in the band diagram of Figs. 1(b) and 1(c), to achieve complementary transport in 2D vertical transistors, both the metal work function and graphene work function should be adjusted to match the energy bands of the channel material. Figure 1(d) shows the fabrication process of our complementary 2D vertical transistor. To fabricate this vertical transistor, doped graphene is first fabricated on a Si(p^{++}) substrate with 300-nm surface oxide (SiO_2). Next, a few-layer WSe_2 flake (0.6–5.2 nm) is mechanically exfoliated and dry transferred on top of graphene using dry-transfer techniques, resulting in vdW-graphene/WSe_2 heterostructures. Finally, metal electrodes with different work functions (Ag, 4.3 eV; Pt, 5.6 eV) are prefabricated on a sacrificial Si wafer and then mechanically released using a previously developed vdW-metal-integration process (see Sec IV for details) [14,17,19,22,23]. Here, vdW-metal contacts are essential for the realization of complementary 2D vertical transistors for two reasons. First, vdW-metal integration can protect the fragile WSe_2 channel from high-energy hot atoms that can damage the delicate 2D lattice during conventional metal deposition, leading to direct leakage vertical current paths and eventually short circuiting of ultrathin vertical transistors [5,14,19]. Second, vdW-metal integration enables an atomically clean and electronically sharp interface (as evidenced by the TEM images in previous reports [17,19,24]) in the metal-WSe_2 contacts, minimizing conventional Fermi-level-pinning effects [17]. Therefore, we can simply select metals (with different work functions) to match either the conduction band or valence band of WSe_2, enabling the injection of electrons or holes, depending on the metal work function used.

As mentioned above, the graphene work function should also be adjusted to match the energy bands of the channel material for achieving complementary transport in 2D vertical transistors. To achieve a highly tunable work function in graphene, two strategies are applied to dope pristine graphene (see Sec. IV for details): *n* doping of graphene via mechanically exfoliation onto the polyvinyl alcohol (PVA) coated substrate [25–27], and *p* doping of graphene through prefunctionalizing the SiO_2 substrate with O_2 plasma and postannealing [28–33]. For comparison, graphene directly exfoliated on SiO_2 substrate (termed as pristine graphene) is also prepared. The transfer characteristics of pristine, *n*-doped, and *p*-doped graphene are shown in Fig. S1(a) within the Supplemental Material [34]. For pristine graphene, the channel's current minimum (Dirac point) is located at a back-gate voltage of about 30 V due to slight *p* doping from the SiO_2 substrate, consistent with previous reports. In contrast, the charge-neutrality point of *n*-doped Gr is shifted to −20 V, due to electron transfer from the PVA substrate to graphene. At the same time, the substrate O_2-plasma functionalization [28–30] and postannealing [31–33] processes further enhance electron transfer from graphene to the SiO_2 substrate, leading to the *p* doping of graphene. Therefore, the charge-neutrality point of *p*-Gr is shifted well beyond 60 V, confirming the heavy-hole-doping effect in graphene.

In addition to electrical measurements, Raman spectroscopy is further carried out to confirm effective doping and the graphene work function. As shown in Fig. S1(b) within the Supplemental Material [34], the *G* and 2*D* peaks are redshifted for *n*-doped graphene and blueshifted for *p*-doped graphene, in agreement with previous reports [35–37]. Moreover, the doping concentration can be quantitatively estimated using the I_{2D}/I_G intensity ratio. $I_{2D}/I_G = 2.3$ (for *n*-doped graphene) corresponds to a doping concentration of 0.25×10^{13} cm^{-2}, while $I_{2D}/I_G = 1$ (for *p*-doped graphene) corresponds to a doping concentration of 1.6×10^{13} cm^{-2}, as reported in previous work [36]. Using these carrier concentrations, the estimated Fermi energies of our *n*-Gr and *p*-Gr are 4.4 and 5.1 eV, respectively (see Sec. IV for details), suggesting that our doping strategy can effectively tune the work function of graphene. Furthermore, the work functions of doped graphene are further verified by Kelvin probe force microscopy (KPFM) measurements, as shown in Fig. S1(c) within the Supplemental Material [34]. The calculated work functions of *n*-doped and *p*-doped graphene are 4.43 and 5.05 eV, respectively (see Sec. IV for details), which are consistent with the Raman results. It is noted that, from the surface-potential mapping [Figs. S1(d) and S1(e) within the Supplemental Material [34]], doping in the bottom graphene layer is highly uniform, which is critical for it to act as an efficient carrier source.

Next, to achieve *n*-type vertical transistors, we adopt *n*-doped graphene and vdW Ag (work function of 4.3 eV) as the bottom and top contacts of the WSe_2 channel, respectively. The optical image and cross section of the *n*-type 2D vertical transistors are illustrated in Figs. 2(a) and 2(b). To confirm the device polarity of the *n*-Gr/WSe_2/vdW-Ag

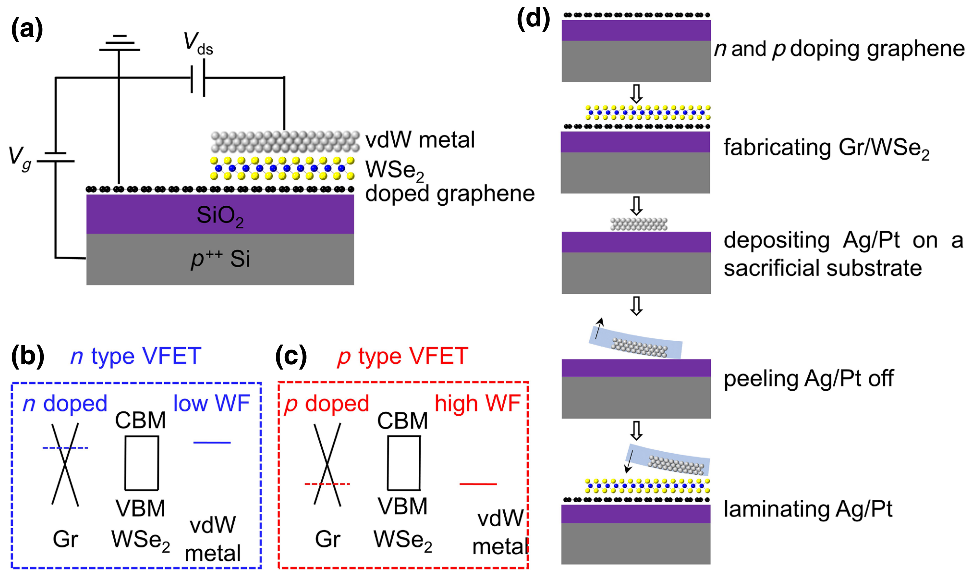

FIG. 1. (a) Schematic of the complementary WSe_2 vertical transistors, in which doped graphene and vdW metal with proper work functions are used as the bottom and top contacts of the WSe_2 channel, respectively. Proposals to realize *n*-type (b) and *p*-type (c) transport in 2D vertical transistors. WF, work function. CBM, conduction-band minimum. VBM, valence-band maximum. VFET, vertical field-effect transistor. (d) Schematic of the fabrication process for complementary WSe_2 vertical transistors.

vertical transistors, we perform I_{ds}-V_g transfer characteristic measurements on various devices with different channel thicknesses. For all device measurements, as illustrated in Fig. 1(a), the bottom graphene is grounded as the source, the top vdW metal is biased as the drain, and a back-gate voltage is applied to highly doped silicon. As shown in Figs. 2(c)–2(f) and Figs. S2(a)–S2(d) within the Supplemental Material [34], clear *n*-type transport behavior with an ON:OFF ratio of up to 10^4 is observed. We note that the ON:OFF ratio decays from 1.43×10^4 to 2 with reducing channel length (WSe_2 thickness) from 5.2 to 0.65 nm (see Fig. S3 within the Supplemental Material [34]), which is consistent with previous reports [5,7,14] and can probably be attributed to the increasingly enhanced tunneling effect in such an ultrashort-channel regime [5,7,14,38].

Figures 2(g) and 2(h) show the band diagrams of our *n*-type WSe_2 vertical transistor. In this device, the work functions of *n*-Gr and Ag are close to the CBM of WSe_2 [Fig. 2(g)], enabling electrons to be the majority carrier and dominate *n*-type transport behavior. As shown in Fig. 2(h), a negative gate voltage can shift the Fermi level of graphene far away from the CBM of WSe_2, leading to a larger Schottky barrier at the graphene-WSe_2 junction, and the device is at the OFF state. On the other hand, a positive gate voltage reduces the barrier between graphene and WSe_2, enhancing the carrier-transport efficiency, and the device is in the ON state. This working mechanism is consistent with previous MoS_2-based vertical transistors and is responsible for the observation of *n*-type transistor behavior [2,5].

Then, *p*-type WSe_2 vertical transistors [see Figs. 3(a)–3(f) and Figs. S2(e)–S2(h) within the Supplemental Material [34]] are fabricated using *p*-doped graphene and vdW Pt (work function of 5.6 eV) as bottom and top electrodes, respectively. In this device [Fig. 3(g)], the work functions of *p*-Gr and Pt are close to the VBM of WSe_2, leading to the *p*-type transistor behavior, as designed in Fig. 1(c). At this point, applying a negative gate voltage shifts the graphene Fermi level to the VBM of WSe_2, leading to a smaller Schottky barrier at the graphene-WSe_2 junction, and the device is in the ON state. On the contrary, a positive gate voltage enhances the barrier between graphene and WSe_2, reducing carrier-transport efficiency, and the device is in the OFF state [Fig. 3(h)]. This mechanism of operation is responsible for the observed behavior of *p*-type transistors. Similar to the *n*-type transistor, due to the inevitable enhanced tunneling effect, the ON:OFF ratio of the *p*-type transistor decays from 41 to 2 with decreasing channel length from 5.2 to 0.65 nm (Fig. S3 within the Supplemental Material [34]). We also note that the ON:OFF ratio of the *p*-type vertical transistor is smaller than that of the *n*-type vertical transistor; this can probably be attributed to the weak back-gating effect of heavy-hole-doped graphene (Fig. S1 within the Supplemental Material [34]). While reducing the hole-doping level in graphene may enhance the ON:OFF ratio of *p*-type transistors, achieving a controllably lower hole-doping level in graphene remains a challenge with our current doping strategy (Fig. S5 within the Supplemental Material [34]). In this regard, a more precise doping strategy that can finely adjust the work functions of graphene may enhance

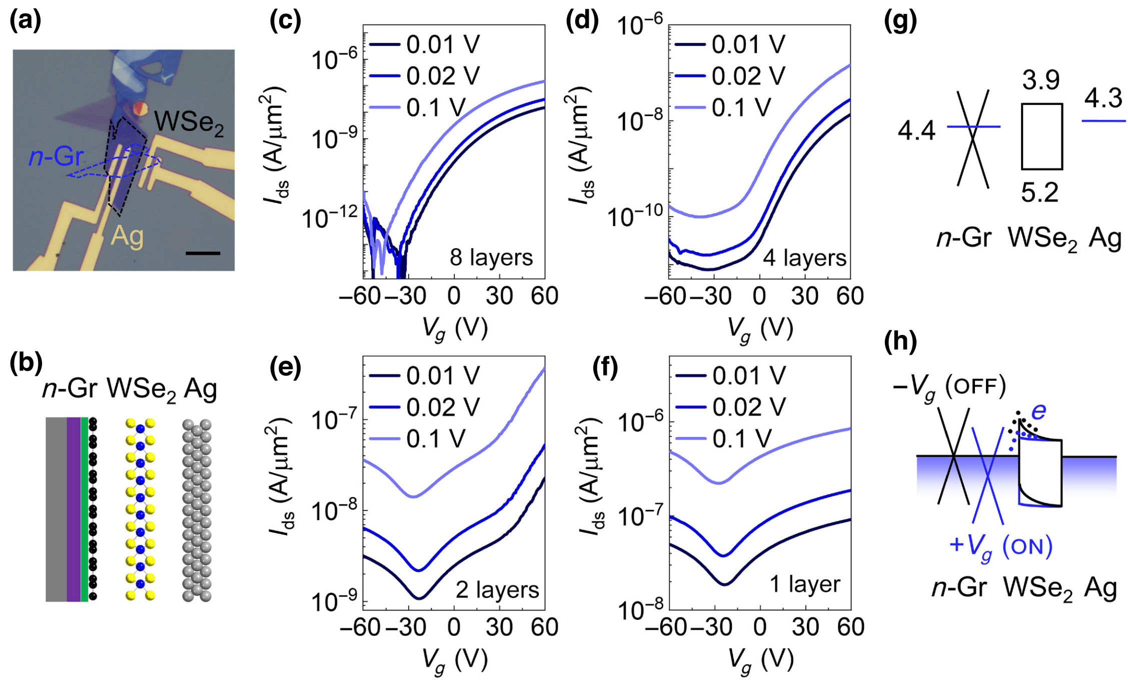

FIG. 2. Optical image (a) and cross section (b) of the n-type WSe_2 vertical transistors. In this transistor, n-Gr and vdW Ag are used as the bottom and top contacts for WSe_2, respectively. In (a), n-Gr and WSe_2 are highlighted by the blue and black dashed lines, respectively. Scale bar, 10 μm. (c)–(f) I_{ds}-V_g transfer characteristics of n-type transistors with 8-layer, 4-layer, 2-layer, and 1-layer WSe_2 as the channel material, respectively. Band diagrams of n-type vertical transistors before contact (g) and at work (h). Units in (g) are eV. In (h), working states at positive and negative gate voltages are represented by blue and black lines, respectively.

the switching performance of p-type transistors. Furthermore, it demonstrates that, when using doped graphene as an electrode for achieving complementary vertical transistors, it is important to find a balance between ON:OFF ratios and polarity control.

Furthermore, to verify the band diagram of our complementary vertical transistors, we use the Arrhenius plot [17,39–41] to extract the barrier height at each interface of both n-type and p-type transistors (Figs. S6 and S7 within the Supplemental Material [34]). The detailed extraction process is given in Sec. IV. For the n-type WSe_2 transistor, the barrier heights at the n-Gr/WSe_2 interface and the WSe_2/vdW-Ag interface at zero gate voltage are 160 and 100 meV, respectively. We note that the experimentally extracted values are much smaller than that based on ideal band parameters [shown in Fig. 2(g)]; this can be attributed to the inevitable aggressive tunneling effects [14] and/or the drain-induced-barrier-lowering effects [5,42,43] at such an ultrashort-channel regime. Even so, the barrier height on the graphene side is slightly larger than that on the vdW-Ag side, which is consistent with the relatively larger work function of n-doped graphene compared to that of Ag. Moreover, both values decrease monotonously with increasing gate voltage [Figs. S6(c) and S6(f) within the Supplemental Material [34]], indicating that carrier injection at both interfaces is dominated by an electron barrier. This result is consistent with the n-type transfer properties shown in Figs. 2(c)–2(f). Reasonable results are also obtained for the p-type WSe_2 transistors (see Fig. S7 within the Supplemental Material [34]). In particular, zero barrier height at the WSe_2/vdW-Pt interface is observed, as evidenced by the positive slope of the Arrhenius plot in Fig. S7(b) within the Supplemental Material [34], because the work function of Pt is much larger than the VBM of WSe_2. In the presence of a finite hole Schottky barrier at the p-Gr/WSe_2 interface, a pronounced rectification effect is reasonably observed in the p-type vertical devices, as shown in Fig. S2(e) within the Supplemental Material [34].

To further confirm the essential role of van der Waals metal integration in our complementary vertical transistors, we also fabricate WSe_2 vertical transistors using the conventional evaporation method. For the n-Gr/WSe_2/evaporated Ag device [Figs. S8(a) and S8(b) within the Supplemental Material [34]], although n-type transport behavior is observed, the performance is largely degraded due to the evaporation-induced leakage paths in the pristine 2D lattice [5,7,14]. As for p-Gr/WSe_2/evaporated Pt device [Figs. S8(c) and S8(d) within the Supplemental Material [34]], in strong contrast to the p-type behavior of p-Gr/WSe_2/vdW-Pt devices, n-type transport behavior is observed; this can be attributed to the strong Fermi-level-pinning effects at the semiconductor–evaporated-metal interface [17,20–22]. Thus, the damage- and pinning-free contacts provided by

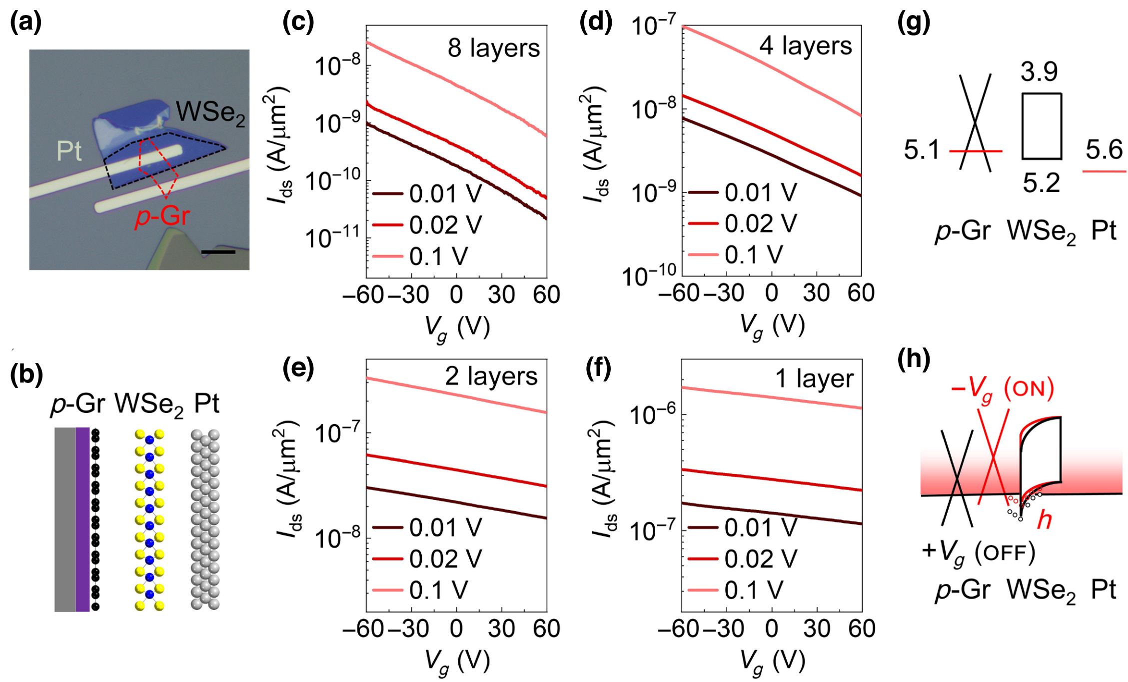

FIG. 3. Optical image (a) and cross-section (b) of the p-type WSe_2 vertical transistors. In this transistor, p-Gr and vdW Pt are used as the bottom and top contacts for WSe_2, respectively. In (a), p-Gr and WSe_2 are highlighted by the red and black dashed lines, respectively. Scale bar, 10 μm. (c)–(f) I_{ds}-V_g transfer characteristics of p-type transistors with 8-layer, 4-layer, 2-layer, and 1-layer WSe_2 as the channel material, respectively. Band diagrams of p-type vertical transistors before contact (g) and at work (h). Units in (g) are eV. In (h), working states at positive and negative gate voltages are represented by black and red lines, respectively.

van der Waals metal integration are a crucial prerequisite for achieving complementary behavior in our vertical transistors. Moreover, for comparison, we also fabricate two types of WSe_2 vertical transistors with pristine graphene as the bottom contact: Gr/WSe_2/vdW-Ag and Gr/WSe_2/vdW-Pt devices. As shown in Fig. S9 within the Supplemental Material [34], bipolar transport behavior is consistently observed in these devices because the Fermi level of pristine graphene is located in the middle of the WSe_2 gap. The above results strongly suggest that

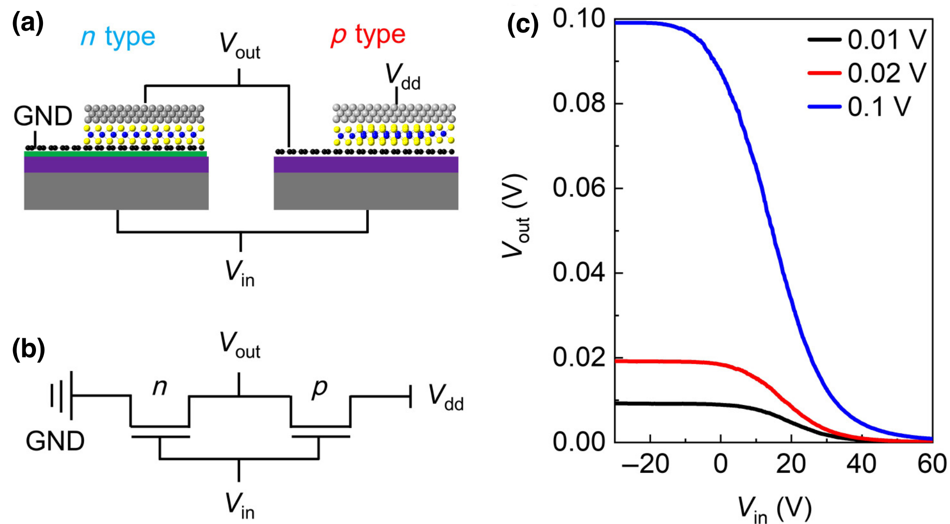

FIG. 4. Schematic of the complementary inverter constructed by connecting two vertical transistors with opposite device polarity, in which the n-type transistor is contacted with n-Gr and vdW Ag, whereas the p-type transistor is contacted with p-Gr and vdW Pt (a), and its corresponding circuit diagram (b). GND, ground. (c) Voltage-transfer characteristics, V_{out}-V_{in}, of the inverter with different V_{dd}.

both properly doped graphene and vdW metal are critical for realizing complementary behavior in WSe_2 vertical transistors.

Finally, with the ability to control the majority carrier through the work function of the vdW metal, complementary device functions can be realized by connecting different 2D vertical transistors. Here, as a proof-of-concept demonstration, we fabricate a complementary inverter by connecting a 4-layer p-type WSe_2 vertical transistor with a 4-layer n-type WSe_2 vertical transistor in series, as illustrated in Fig. 4(a). Its corresponding circuit diagram is presented in Fig. 4(b), in which the p-type transistor is turned ON and the p-type transistor is turned OFF when a small $V_{\rm in}$ is applied, resulting in a high $V_{\rm out}$ close to $V_{\rm dd}$. In contrast, applying a large $V_{\rm in}$ reduces $V_{\rm out}$ close to 0 V. Figure 4(c) shows the $V_{\rm out}$-$V_{\rm in}$ voltage-transfer characteristics of our inverter at various $V_{\rm dd}$, showing the desired switching behavior. Although the present inverter is comprised of transistors on separate chips due to limitations of the doping techniques employed in our work, following our complementary vertical-transistor approach, advancements in doping techniques for 2D materials, specifically in terms of precise selective doping, will facilitate the fabrication of inverters on a single chip.

III. CONCLUSIONS

Using the vdW-metal-integration method, we fabricate graphene/WSe_2/vdW-metal heterostructures and realize complementary transport in these 2D vertical transistors. In these devices, vdW metals retain the intrinsic properties of atomically thin WSe_2 and minimize Fermi-level pinning effects at the metal-WSe_2 interface. The Fermi-level-pinning-free metal-WSe_2 interface allows us to easily control the barrier at the metal-WSe_2 interface via the metal work function. Thus, with doped graphene as the bottom contact, we realize n-type and p-type 2D vertical transistors just by laminating Ag and Pt, respectively, as the vdW contacts for WSe_2. In the end, with the ability to control the majority carriers, we demonstrate a complementary inverter by integrating two vertical transistors with opposite polarities. Our work achieves not only complementary 2D vertical transistors but also provides a common strategy to control the carrier polarity in vertical heterostructures.

IV. EXPERIMENT DETAILS

A. Doping graphene

Pristine graphene is mechanically exfoliated onto the 300-nm SiO_2/p^{++}Si substrate with Scotch tape. To achieve electron-doped graphene, 0.1-g PVA (Alfa Aesar, 98–99% hydrolyzed, high molecular weight) is first dissolved in 10-ml deionized water and heated with magnetic stirring up to 90 °C for 3 h. Then, the solution is spin-coated on the surface of 300-nm SiO_2/p^{++}Si substrate at a speed of 8000 rpm for 30 s and baked at 70 °C for 1 min to remove the solvent. Finally, monolayer graphene is mechanically exfoliated onto the PVA-coated substrate. To obtain hole-doped graphene, the 300-nm SiO_2/p^{++}Si substrate is first prefunctionalized in a plasma cleaner (CIF, CPC-B). The functionalization process is conducted at 100 W for 5 min with O_2 plasma. Then, monolayer graphene is mechanically exfoliated with Scotch tape onto the prefunctionalized substrate. Finally, graphene is postannealed at 340 °C for 3 h under an N_2 atmosphere.

B. Device fabrication

To fabricate the vdW-metal-contact devices, multilayer WSe_2 is mechanically exfoliated and transferred onto as-fabricated n- and p-Gr or pristine Gr through a dry-transfer approach. Next, the Ag(30 nm)/Au(20 nm) and Pt(50 nm) electrodes are prefabricated on sacrificial silicon substrate by standard e-beam lithography and e-beam evaporation, followed by functionalization with a hexamethyldisilazane layer and then spin-coated with a poly(methylmethacrylate) (PMMA) layer. With functionalization, the PMMA layer and metal electrodes wrapped underneath have weak adhesion to the sacrificial substrate and can be mechanically released and physically laminated onto the n- or p-doped graphene-WSe_2 heterostructure using a polydimethylsiloxane stamp. Finally, all pads of the devices are exposed by e-beam lithography for subsequent electrical measurements.

To fabricate the evaporated-metal contacted devices, conventional e-beam lithography is used to define the metal contacts directly on the n- or p-Gr/WSe_2 heterostructure. Then Ag(30 nm)/Au(20 nm) or Pt(50 nm) is implemented by e-beam evaporation followed by a lift-off process with acetone.

C. Material characterization and electrical measurement

The Raman spectrum is measured using a confocal microscope (Renishaw invia-reflex) excited by a 488-nm laser. Surface potential is measured by a Kelvin probe force microscope (Bruker Dimension Icon). The electrical characteristic measurements are performed in a cryogenic probe station (Lakeshore PS-100) at 300 K under vacuum using an Agilent B1500A semiconductor parameter analyzer.

D. Work-function calculation with carrier concentrations

Based on carrier concentrations, the work function of graphene can be calculated by

$$E_{\rm F}(n) = \hbar|v_{\rm F}|\sqrt{\pi n}, \tag{1}$$

where $|v_F| = 1.1 \times 10^6$ ms^{-1} is the Fermi velocity and $\hbar$ is the reduced Planck constant. Substituting $n = 0.25 \times 10^{13}$ cm^{-2} (for n-doped graphene) and 1.6×10^{13} cm^{-2} (for p-doped graphene) into Eq. (1), the Fermi energies of our n-Gr and p-Gr are 4.4 and 5.1 eV, respectively,

E. Work-function calculation with KPFM measurements

The work function of doped graphene is calculated by

$$E_{\mathrm{F,\,graphene}} = E_{\mathrm{F,HOPG}} - (\varphi_{\mathrm{graphene}} - \varphi_{\mathrm{HOPG}}). \quad (2)$$

Substituting $\varphi_{n-\mathrm{graphene}} = 0.13$ eV, $\varphi_{p-\mathrm{graphene}} = -0.49$ eV, $\varphi_{\mathrm{HOPG}} = -0.04$ eV, and $E_{\mathrm{F,HOPG}} = 4.6$ eV into Eq. (2), the calculated work functions of n-doped graphene and p-doped graphene are 4.43 and 5.05 eV, respectively.

F. Schottky-barrier-height extraction

Our vertical transistor can be simplified as two Schottky diodes connected back to back. In this device geometry, the reverse-bias contact consumes most of the voltage drop and dominates the transistor behavior. The current injected through a reverse-bias Schottky barrier can be expressed as

$$I_{\mathrm{ds}} = A^* T^2 \exp\left(\frac{-q\phi_{\mathrm{b}}}{k_{\mathrm{B}} T}\right)\left[1 - \exp\left(-\frac{qV_{\mathrm{ds}}}{k_{\mathrm{B}} T}\right)\right], \quad (3)$$

where A^* is the effective Richardson constant, T is the temperature, q is the elementary charge, ϕ_{b} is the Schottky barrier height, k_{B} is the Boltzmann constant, and V_{ds} is the voltage across the diode. If $qV_{\mathrm{ds}} \gg k_{\mathrm{B}} T$, Eq. (3) can be simplified to

$$I_{\mathrm{ds}} = A^* T^2 \exp\left(\frac{-q\phi_{\mathrm{b}}}{k_{\mathrm{B}} T}\right). \quad (4)$$

Then, the Schottky barrier at a given gate voltage can be extracted from the slope in the Arrhenius plot using the following equation:

$$\ln\left(\frac{I_{\mathrm{ds}}}{T^2}\right) = -\frac{q\phi_{\mathrm{b}}}{k_{\mathrm{B}} T} + c, \quad (5)$$

where c is a constant.

For n-type vertical transistors, we use $V_{\mathrm{ds}} = 0.1$ and -0.1 V to extract the electron-barrier height at n-Gr/WSe_2 and WSe_2/vdW-Ag interfaces, respectively. For p-type vertical transistors, we use $V_{\mathrm{ds}} = 0.1$ and -0.1 V to extract the hole-barrier height at WSe_2/vdW-Pt and p-Gr/WSe_2 interfaces, respectively.

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