

Device Isolation in Hybrid Field-Effect Transistors by Semiconductor Micropatterning Using Picosecond Lasers

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A solid-state picosecond laser is used to ablate semiconductor thin films in spatially localized areas, providing an alternative to device isolation strategies based on chemical or ion etching techniques. Field-effect transistors (FETs) of emerging organic and inorganic materials often utilize a continuous semiconductor film and an array of top-contact electrodes. Electrically isolating individual FET components from other circuit elements is essential in order to reduce parasitic capacitances and unwanted current pathways, both to improve device performance and to enable the observation of new or enhanced physical phenomena. We pattern FET arrays with ultrafast-pulse-duration (1.5 ps) and low-fluence (0.09 J cm^{-2}) optical pulses using the fundamental wavelength (1030 nm) of an Yb-YAG laser. We investigate two representative semiconductor materials. First, zinc oxide (ZnO) is deposited onto Si/SiO₂ substrates by sol-gel methods and used to create *n*-channel FETs with aluminum top electrodes. Isolation of individual FETs enables the clear observation of photomodulation of the FET device parameters via photoinduced electron donation from an adsorbed chromophore. The second system comprises thin-film bilayers of tellurium and organic semiconductor molecules sequentially vapor-deposited onto Si/SiO₂ substrates, with gold electrodes deposited last. Charge carrier mobility is maintained for devices isolated by picosecond lasers, but leakage currents through the FET dielectric are drastically reduced.

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I. INTRODUCTION

Thin-film electronic technology based on organic and inorganic semiconductors has seen improvements in performance and processing during recent years, motivated by low-cost and large-area fabrication of chemical sensors, active-matrix displays, and transparent or flexible microelectronics [1–13]. However, leakage currents and bias effects remain as important challenges to the commercialization of such devices [14–28]. The electrical characterization of novel circuit components, i.e., utilizing field-effect transistor (FET) devices to evaluate new semiconductor materials, can also be confounded by gate leakage and bias stress. The effects can be detrimental, resulting in high off currents, low on/off ratios, and increased power consumption. Therefore, leakage-current reduction results in the greatest benefit to devices designed for low power and mobile applications, like radio-frequency identification tags and autonomous sensors.

The creation of well-defined stable interfaces between inorganic electronic materials and organic electronic systems provides a new range of functionalities. Photovoltaic charge separation can be promoted, transistor threshold voltages can be shifted, and memory effects can be obtained [29–32]. High carrier mobility and transparency in the inorganics can be combined with photosensitivity at desired wavelengths from the organics. The surface chemistry of oxide electronic materials and gate dielectric materials provides important functionality, including photoresponse, environmental sensitivity or protection, and local dipole moments that can dramatically shift electronic properties. For instance, molecules on the surface of *n*-channel FETs based on zinc-oxide (ZnO) and zinc-tin-oxide (ZTO) semiconductors can enhance mobility or induce photocurrent [32–36]. However, it is difficult to incorporate electronic materials in devices without destroying their bulk or surface electronic properties during processing. Limiting the leakage current through thin-gate dielectric layers and isolating adjacent devices are important goals when introducing new materials into devices and applications. In fundamental studies, the isolation of regions of active material improves

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the accuracy and reliability of fundamental measurements by reducing leakage current and parasitic bias stress from the semiconducting film surrounding the device [2,3,15,19–22].

Semiconductor thin films fabricated by using solution- or vapor-deposition techniques often produce a thin layer that uniformly covers the entire substrate comprising the gate electrode and gate dielectric layers [1–6,8–10,12,14,15]. Multiple devices are created on a single shared semiconductor film, typically by depositing metallic electrodes from vapor through a shadow mask. Such devices mimic conventional metal-oxide-semiconductor (MOS) device structures and typically utilize standard Si/SiO₂ substrates, which allow the distribution of gate voltages to arrays of FETs when the silicon is sufficiently doped, and silicon dioxide acts as the gate dielectric. The electrical continuity of the semiconducting layer increases parasitic currents between the source and drain electrodes of adjacent FETs and increases the effective area over which voltages can be equalized. In addition, imperfections of the gate oxide, i.e., pinholes or local defects, can result in orders-of-magnitude increases in leakage current. It is therefore highly desirable to reduce these effects by physically isolating each device.

A number of FET configurations and circuit components can display similar leakage problems, although a few methods have been implemented to mitigate leakage current and unwanted effects, such as engineering device interfaces and geometry [18–28] or implementing biasing and feedback circuits [15–17]. Several strategies exist to mitigate leakage currents via local chemical passivation [26–28], designed to restrict leakage current through the gate dielectric of thin-film transistors. For instance, self-assembled molecular monolayers (SAMs) provided an electrostatic barrier to leakage currents in *n*-channel organic semiconductor (OSC) FETs using a dielectric consisting of just 10 nm of silicon dioxide (SiO₂), which would otherwise have exhibited sufficiently high leakage to make FET operation impossible [26]. The molecular side chains of the SAM contributed to the capacitance of the gate dielectric and modify the differences in FET operation at millisecond versus 10-s gate application times. We recently reported the demonstration of OSC molecular segments contributing to the gate capacitance, although they suffer from apparently insufficient dielectric strength and result in considerable gate leakage [27]. The parameters of *p*-channel tellurium-based FETs are similarly modulated by using OSC films to shift internal potential differences among layers of the device, and the OSC substantially acts as a gate material in series with the oxide dielectric [28].

Similar effects can be expected with newer high-dielectric-constant (high-*k*) dielectrics [37–41]. Enhancing the physical properties of the dielectric may be the best way to mitigate current leaking vertically through the dielectric layer, but it will not necessarily reduce lateral currents. Significantly, a

change in dielectric, or a modification like SAMs, can affect devices electronically or chemically in potentially undesirable ways or may be ill suited for particular applications. High-*k* dielectrics are shown to reduce charge carrier mobility in OSCs due to a random dipole field present at the interface and local polarization effects leading to carrier delocalization [42]. Moreover, thinner dielectrics are more difficult to obtain by using large area processing due to uniformity issues and an increased risk of pinholes or defects [3]. Clearly, there are compromises involved with the choice of gate-insulator material and its thickness, which should be designed to achieve high capacitance density, low gate leakage, and desirable interfacial chemistry for compatibility with semiconductor materials. Regarding the modeling of FETs, reports that take leakage current into account do not consider isolation by also including active regions beyond the device stack [23–25]. It appears that leakage is not dependent on a particular electronic or chemical property of the dielectric (for voltage potentials below the dielectric breakdown) but, instead, is mainly dependent on the pinhole or defect density, dielectric thickness, and gate-to-source or gate-to-drain overlap.

Lithography using solution-processing [15,22] and high-resolution printing methods [39,43] is presently being developed. As opposed to silicon-based technology which requires high temperatures to fabricate large-area platforms (or handles) of rigid crystalline semiconductor material, devices based on flexible substrates utilize low-temperature processes that allow diverse configurations and complexities to be obtained, including multilayer gate stacks and individually patterned gate electrodes for the fabrication of integrated circuits [18–22]. Individually patterned gate electrodes reduce the risk of leakage current by localizing the applied electric field, which reduces the parasitic capacitances from large areas extending beyond the active device, and potentially reducing parasitic capacitance overlap within the device stack [2,3,14,19–22].

However, there are still drawbacks to these emerging methods, such as alignment issues and chemical requirements [19–22]. Rather than controlling the alignment of gate-to-contact overlap during processing, or depending on additive-only processes, patterning can be achieved by removing material from films after their fabrication using “dry-” or “wet-”etch techniques, thus isolating the semiconductor films to their individual device stack. Precise patterning without materials degradation is critically important in applications where several devices must be fabricated by using adjacent areas of a conductive film, i.e., when either active layer cannot be patterned *in situ* with sufficient quality or resolution (such as the active organic semiconductor, dielectric layer, or the Si handle). Lithographic processes are well developed for patterning a variety of inorganic and organic materials but often require multiple chemical steps and can have undesirable effects on electronic materials. For instance,

inorganic semiconductors such as ZnO are etched by developers used in photolithography, which can alter the surface chemistry and layer microstructure even when the active ZnO layer is not completely removed. Other materials, such as GaN, resist etching and cannot be patterned by chemical methods.

Together, these previous observations illustrate both the importance and the continuing challenge of controlling gate current leakage in semiconductor devices across a wide range of materials systems. Furthermore, other effective strategies for limiting gate leakage must do so without modifying the interface chemical state of the material. We present here a laser direct-write (LDW) processing method and demonstrate it in the isolation of solution-processable hybrid ZnO/organic and vapor-processable Te/OSC field-effect devices. LDW utilizes ultrafast pulse duration, particularly valuable for patterning devices while leaving the surface chemistry unchanged for the preservation of device performance and for the attachment of functional molecules. The physics allow the LDW method to be applied to semiconductor materials that require or benefit greatly from dry postprocessing methods, due to etching sensitivity or etch resistance. Moreover, microprocessing via laser allows us to fabricate semiconductor films under ideal conditions and then pattern a large area, which otherwise would require multiple invasive and complicated steps. Similar laser-based lithographic techniques have gained significant interest as an alternative approach to patterning metallic and dielectric materials with minimal contact [44–63].

Optical pulses with picosecond durations enable high peak powers on the order of 10 MW to be produced with only a few watts of average optical power. Focused radiation can have intensities reaching several TW cm⁻², which permits direct machining of temperature-sensitive, brittle, and soft materials with low total power and thus a small rise in the temperature of the substrate as a whole. In addition to materials that have fundamental optical band gaps with energies lower than the photon energies, materials that are transparent at the laser wavelength can be machined via nonlinear absorption. Previous applications of picosecond lasers in micromachining are in medical technology, anti-icing thin films, optical filters, and circuit components [44–51]. Engelhardt, Hildenhagen, and Dickmann, for example, investigated the fundamental processing properties of picosecond laser radiation on stainless steel, alumina, poly(methyl methacrylate), and quartz glass [52]. All the materials they investigated could be ablated efficiently provided that the laser fluence and peak powers were above the ablation threshold of the material while maintaining temperatures below those that would result in thermally driven compositional or microstructural changes.

We investigate two representative systems, including ZnO prepared as a standard transistor semiconductor and in a photomodulatable bilayer with a rhenium bipyridine (Re1c) chromophore, and thin-film bilayers of tellurium

(Te) above OSCs. The chemical structures for organic molecules are given in Supplemental Material (Fig. S1) [64]. The semiconductor thin films for this study are deposited on Si/SiO₂ substrates and subsequently source and drain contacts were deposited. Although flexible substrates with a variety of gate and dielectric systems have been developed for electronic applications, the Si/SiO₂ platform remains attractive for semiconductor device testing because of its flatness, relatively dense native surface oxide, and high earth abundance. Moreover, its standardization and the reputation of thermal SiO₂ as only a marginal-quality dielectric provides a platform on which the utility of certain methods for improving devices may be readily observed. The source and drain electrodes of FETs are isolated by optically patterning the semiconductor film using the fundamental wavelength (1030 nm) of a solid-state picosecond laser (Yb-YAG, Hamamatsu Photonics). Detailed experimental conditions for the optical patterning are given in the Methods section.

To determine effects of laser isolation on FET performance, we analyzed the steady-state electronic behavior (field-effect mobility, on/off current ratio, and gate currents) before and after the LDW process. An explicit lowering of the leakage current is demonstrated by isolation, particularly with the picosecond laser. The only factor that changes due to isolation is reduction in semiconductor area capacitively coupled to the gate for each device. Reducing the semiconductor area does not directly influence the effective performance parameters of the device but simply reduces the leakage vertically through the dielectric to the gate and laterally along the semiconductor. Conclusions drawn from this report will be applicable to ultrafast laser ablation of active semiconductor materials (organic and inorganic, with various mechanical, chemical, and optical properties), particularly for top-contact bottom-gate FETs but potentially for a wide range of device systems. Besides technical processing advantages, the laser isolation allows the confirmation of key scientific observations otherwise masked (or diminished) by leakage current, including the ZnO photomodulation and the effects of Te-OSC interfacial polarization examples discussed here.

II. EXPERIMENTAL METHODS

Heavily As-doped silicon wafers (SI-Tech, Process Solutions, $N_D \sim 10^{18}$ cm³) are cut into one-square-inch (6-cm²) pieces and then cleaned by sonication in deionized water, acetone, and 2-propanol for 10 min each and blown dry with N₂. Substrates are cleaned further by submerging in piranha solution (sulfuric acid to hydrogen peroxide 3 : 1; CAUTION: highly corrosive and dangerous to skin) for 30 min, followed by sonication in deionized water for 10 min, blown with N₂, and baked on a hotplate at 110 °C for 5 min. The insulator capacitance for 100 and 300 nm of

thermally grown silicon dioxide is consistent with previous reports: 35.6 and 11.5 nF/cm², respectively. 5,5'-bis(4-hexylphenyl)-2,2'-bithiophene (6PTTP6) is synthesized by using a well-established method [65]. Te powder (325-mesh, 99.99% metals basis, Alfa Aesar) is used as purchased. Hybrid bilayer FETs are fabricated by thermally evaporating OSC and Te powders by using an Edwards thermal evaporation system at pressures below 5×10^{-6} Torr, deposited 10 nm thick from alumina crucibles in succession during the same vacuum cycle, using the same deposition rate of 0.3 Å s⁻¹. Si substrates with 100 nm of SiO₂ are held at 55 °C during deposition. Gold or aluminum electrodes are deposited 50–100 nm thick at 0.5 Å s⁻¹ through a shadow mask. The channel width and length are about 8000 and 250 μm, respectively, for Te/OSC hybrids and 1000 and 100 μm, respectively, for ZnO devices. Deposition rates and thicknesses are monitored by quartz crystal microbalance. Substrate temperature is monitored by thermocouples placed on the substrate back side. Silicon gates for FETs are accessed by scratching through the oxide with a diamond scribe.

The ZnO precursor solution consists of 0.3 M zinc acetate dihydrate (Alfa Aesar) dissolved in absolute ethanol with 0.3 M of acetyl acetone added as a stabilizer (adapted from Ref. [8]). The precursor solution is stirred overnight at room temperature and filtered through a 0.2-μm polytetrafluoroethylene (PTFE) filter. As-prepared precursor solution is kept for 24 h to promote hydrolysis and filtered through a 0.45-μm PTFE filter. ZnO solutions are deposited onto 300 nm SiO₂ by spin coating at 5000 revolutions per minute for 30 s followed by heating to 75 °C for 10 min to evaporate residual solvent. The films are annealed in air at 500 °C for 1 h. The coating process is repeated in three consecutive cycles of spin coating and heat treatment. The heat treatment converts the zinc acetate precursor into ZnO and improves the crystallinity of the film. The ZnO layer exhibits a crystallographic texture in which the *c* axis is along the surface normal of the substrate. The surface of prefabricated ZnO FET samples is sensitized with the Re1c dye molecules by immersion in 5 ml of a 1 mM solution of Re1c dye in tetrahydrofuran (THF) at room temperature for 24 h. The vials containing the samples are covered in foil during immersion to block light. After immersion, the samples are rinsed with 5–10 ml of pure THF without allowing the dye solution to dry on the sample surface and then blown dry with a high-purity nitrogen jet.

Amplified Yb:YAG picosecond laser pulses (MOIL-ps, Hamamatsu Photonics), pulse duration ca. 1.5 ps, 1030-nm wavelength, and 40-kHz repetition rate are used to process the hybrid structures. For other samples, the wavelength can be selected to up to the fourth harmonic to achieve maximum absorption. The laser pulses are focused on the sample surface by using an achromatic lens with a focal length of 60 mm delivering a focused beam spot with a diameter of approximately 25 μm and a laser fluence of

TABLE I. Optical beam parameters.

Wavelength	1030 nm
Rep. rate, scan speed	20 kHz, 480 mm min ⁻¹
Spot size	25 μm
Pulse duration	1.5 ps
Fluence	0.09 ± 4 J cm ⁻²
Peak power	0.24 MW
Min spot size	1.5 μm

0.09 J cm⁻² for the hybrid material. The sample is located on an XYZ translation stage and scanned at 480 mm/min. Table I shows the beam parameters used for laser processing and the pertinent specifications of the Hamamatsu Photonics MOIL laser L11590. This laser has a tunable pulse duration capability (from 1.5 to 10 ps) and high energy per pulse (200 μJ). Typically, picosecond lasers achieve only low energy per pulse (approximately 10 μJ) and rely on high repetition rates to increase peak power.

FET measurements, taken before and after isolation, are employed by using an Agilent 4155C semiconductor parameter analyzer. Low-resistance probes from micro-manipulators are used to contact devices under ambient fluorescent lighting conditions, in air.

III. FET ISOLATION IMAGING

Trenches created by picosecond-laser patterning are imaged by using laser optical microscopy, scanning electron microscopy (SEM), and atomic force microscopy (AFM). The images and height profiles show that the laser patterning physically isolates transistors from the shared semiconductor film. The physical mechanism of the patterning varies for different semiconductor layers. The ZnO semiconductor layer and SiO₂ gate insulator of the ZnO FETs both have band gaps larger than the fundamental 1030-nm wavelength of the Nd:YAG picosecond laser. A large fraction of the incident optical power during patterning is thus transmitted to the Si substrate. In ZnO, the rapid ablation of the Si ruptures the SiO₂ and ZnO layers, creating the trenches shown in the SEM images in Fig. 1. The bottoms of the trenches in Si exhibit a pattern of ridges consistent with interface instabilities observed in rapid solidification of laser-melted Si [57,58].

The mechanism for laser patterning and subsequent isolation of a Te FET is different from that of the ZnO devices. Sufficient optical power is absorbed in Te to ablate the Te layer before damaging the underlying SiO₂ or Si. Figure 2 shows bright-field optical micrographs of the regions patterned by using the picosecond laser. Inspection of the ablated surface reveals that the Te and OSC layers are completely removed by the patterning. Atomic force microscopy confirms the removal of the approximately 10 nm Te as well as the 20 nm of 6PTTP6 underlying it, while the dielectric surface remains intact (Fig. S2) [64]. The trenches in Te-based devices are 10–30 nm deep,

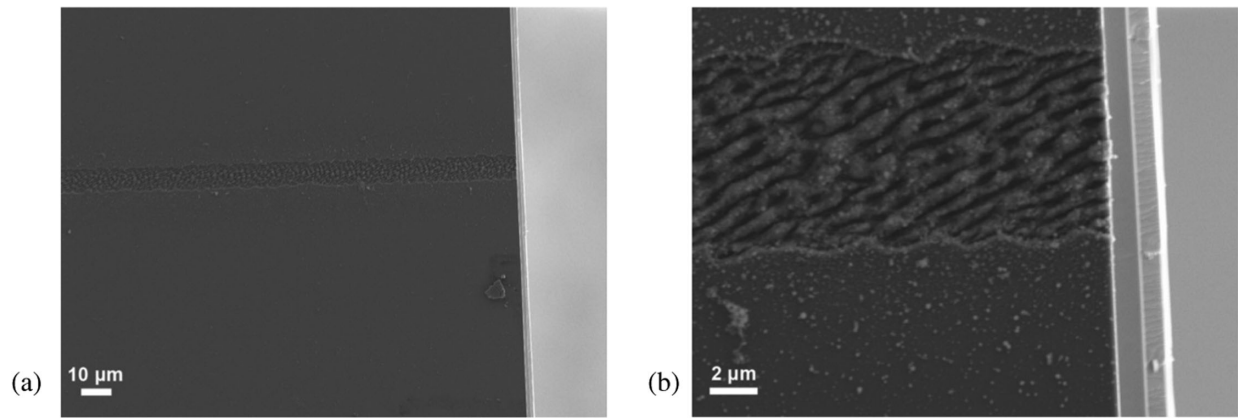


FIG. 1. Scanning electron micrographs of (a) a laser-isolated microchannel running up to the freshly cleaved edge of the Si/SiO₂/ZnO chip (scale bar 10 μm) and (b) magnification of the previous region near the edge (scale bar 2 μm).

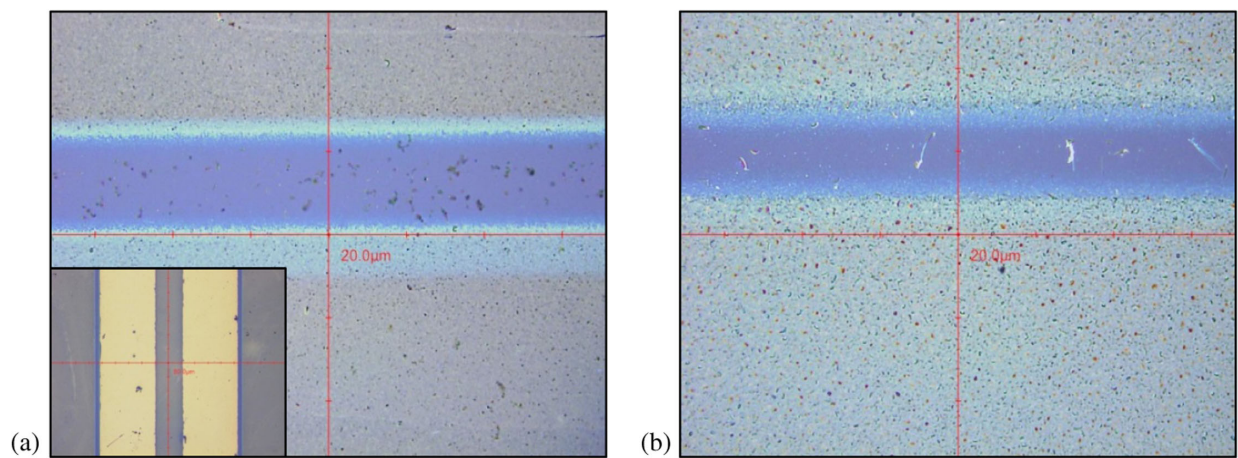


FIG. 2. Color optical microscope images show microchannels in (a) Te (the inset shows channels in Te alongside the gold electrode pair) and (b) Te/6PTTP6.

which is the approximate thickness of semiconductor stacks. The edge roughness is less than 1 μm, and burrs are not apparent on the Te surface. It is therefore relatively straightforward to remove Te films selectively at low ablation thresholds without damaging the SiO₂ dielectric.

The width of fabricated channels matches the diameter of the pulse beam in the case of Te-based devices, 25 μm, and is thinner for zinc-oxide-based devices, 10 μm. In both cases, some of the material removed from the trenches is deposited as submicron debris in the surrounding areas. Channel widths obtained by hand isolation, via scribing around devices with hard tools or using paint brushes carrying solvent, could not be reduced below 100 μm due to the width of the scribing tools.

IV. FET ANALYSIS AND DISCUSSION

FET device parameters such as field-effect mobility (μ), threshold voltage (V_{th}), gate current (I_G), and the ratio of on-to-off drain current (I_{on}/I_{off}) are measured as a function

of the applied gate voltage (V_G) and source-drain voltage (V_{SD}) before and after isolation. Tables SI and SII of the Supplemental Material [64] list the performance parameters of all FETs before and after the LDW method and after scribing for comparison. Identical control devices are stored for the same time interval but do not undergo isolation. The electronic effects of hand isolation are essentially reproduced by the LDW method. Isolation by either method reduces I_G while not altering the critical parameters, such as field-effect mobility μ and I_{on}/I_{off} . Figure 3(a) shows graphically that the critical FET parameters are essentially unchanged by the LDW method for zinc-oxide- and tellurium-based devices. I_G of FETs in both the on and off operation are shown separately in Fig. 3(b) for zinc-oxide- and tellurium-based devices.

We observe that all parameters (mobility, on/off ratio, and gate currents) depend on the semiconductor material and that isolation treatment affects the gate current only by reducing it to a minimal value. The final gate leakage currents depend on the parasitic source-gate and drain-gate

overlap and on the number of defects or pinholes in the dielectric that remain in the gate stack after isolation treatment.

A. Zinc-oxide-based FETs

ZnO forms *n*-channel accumulation mode transistors. After the LDW method, the measured I_G is reduced in the off mode by almost 2 orders of magnitude [Fig. 3(b)]. There is still relatively large leakage in ZnO devices at high gate voltages (50 V), which may be due to leakage at high fields in the regions directly beneath the source (*S*) and drain (*D*) electrodes or the FET channel.

Figure 4 shows the transfer curves and I_G for ZnO devices before and after isolation, with $V_{SD} = 5$ and 50 V. The drain current is enhanced by isolation due to fewer current losses by leakage, which accounts for the slight decrease in the on/off ratio [Fig. 3(a)]. Figure 4 also shows that dielectric breakdown occurs after applying a gate

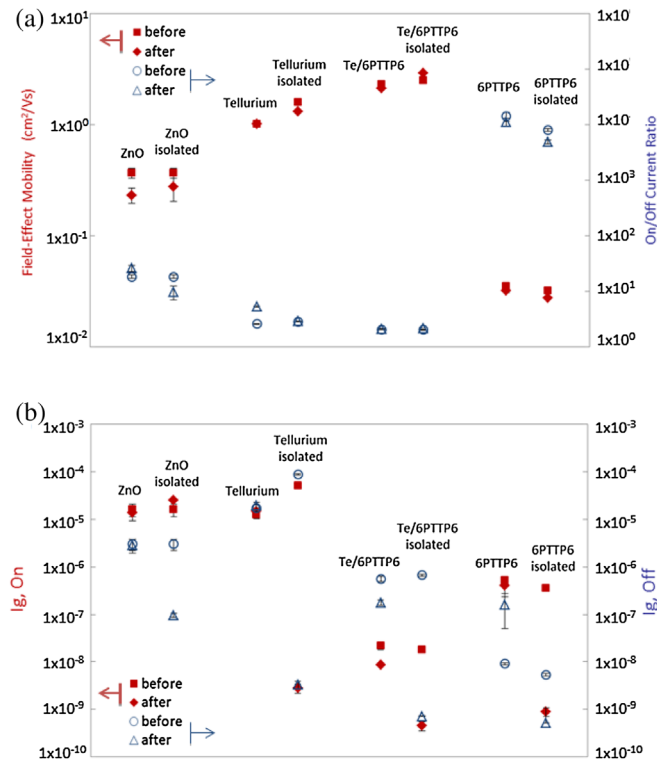


FIG. 3. Comparison chart for (a) field-effect mobility (left axis) and on/off current ratio (right axis) and (b) gate current in the on mode (left axis) and off mode (right axis) for zinc-oxide, tellurium-based, and organic semiconductor devices. Values for identical sample sets are shown in vertically aligned points; sample sets are labeled above from left to right; each point is an average of 12 devices. “Before” and “after” refer to measurements taken before and after laser isolation; values are given for both nonisolated and “isolated” sample sets. The lower value of red diamond and blue triangle values (compared to red square and blue circle values, respectively) for isolated systems indicates the beneficial effect of the isolation.

voltage of 40 V or higher but that isolation minimizes gate leakage over the rest of the gate voltage range. I_G for on-mode ZnO devices is greater after isolation according to Fig. 3(b) only because the value used is taken at $V_G = 50$ V, whereas the I_G due to isolation is actually much lower for applied gate voltages below the dielectric breakdown. This difference is understandable, because isolation does not reduce vertical leakage current from the gate drain and source overlap, which would increase drastically during dielectric breakdown as observed. The LDW method only reduces lateral currents due to an extended semiconductor film gate stack and vertical pathways beyond the gate stack.

Nonchemical isolation methods are particularly useful for ZnO devices, because chemical etching, usually with acid, can modify ZnO/molecular interfaces. The vapor transport of the etchant can result in interface modification within regions of the film separated from the etched regions up to distances of millimeters or more. The organometallic donor ReIc can be attached to ZnO and used to donate electrons to ZnO following optical excitation [36]. Here we illustrate the importance of nonchemical isolation by examining the photocurrent response for ReIc-functionalized ZnO FETs that are isolated by laser ablation and compare to control devices which are not isolated. The drain and gate currents are measured in the dark and then again after exposing the FET channel to light ($\lambda = 532$ nm) for 60 s. Prior to isolation, the leakage current is on the same order of magnitude as the drain current (greater than $5 \mu\text{A}$ at a gate voltage of 30 V), as expected because the relatively high mobility in the ZnO layer allows leakage current from a large area of the dielectric to contribute. The leakage I_G is greater than the photocurrent by a factor of 4 under this forward bias condition ($V_G = 30$ V). After the isolation via the LDW process, the magnitude of the I_G is reduced to less than 1% of the magnitude of the photocurrent. Figure 5 shows the ratio of I_G to photocurrent for devices that are not isolated and devices isolated by the LDW method. Figure 6 shows the transfer curves and I_G for ZnO/ReIc devices with and without isolation. The isolation procedure could greatly enhance the possibilities for use of organic-inorganic hybrids for photodetector applications.

As an alternative to the LDW method, FET devices can be isolated by locally etching the ZnO films with a mild acid, such as acetic acid. Chemical isolation using acetic acid and a paint brush is more effective than laser processing for eliminating gate leakage in zinc-oxide films (reduced more than 5 orders of magnitude; Fig. S3 [64]). This effectiveness could be due to the fact that the excess ZnO semiconductor material is removed from around and between FETs, while the underlying SiO₂ gate dielectric is undamaged by the comparatively mild acid etching. However, vapors from the acetic acid etching process can uncontrollably change the conductivity of the ZnO film remaining in the channel, as well as possibly affect

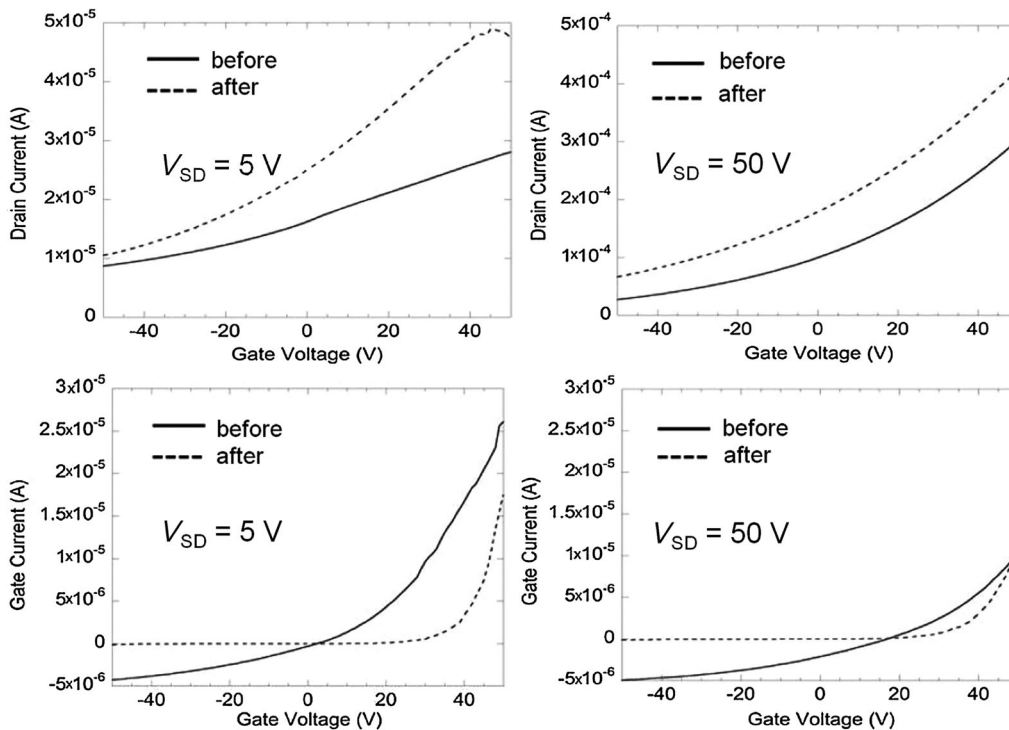


FIG. 4. Transfer curves and I_G for ZnO devices before and after isolation, with V_{SD} equal to (a) 5 and (b) 50 V.

attachment of donor molecules on the surface by blocking attachment sites for the carboxylic acid groups [33]. Additionally, this form of hand isolation for research devices is not scalable as a high-throughput isolation method for manufacturing arrays of many devices.

B. Tellurium and organic-based FETs

Elemental tellurium behaves as a p -channel depletion mode transistor, which means the FET is inherently on at zero V_G and requires positive V_G to turn the device off. The gate voltage required to turn off FETs is approximately 40–50 V for our 10 nm of Te deposited at a rate of 0.3 \AA s^{-1} onto SiO_2 substrates held at 60°C . 6PTTP6 is also p -channel and is deposited under the same conditions. 6PTTP6, however, operates in accumulation and requires only negative V_G . The drain voltage (V_D) for all 6PTTP6 and Te devices is swept from 0 to -20 V for measuring output curves and held at -20 V for transfer curves.

6PTTP6 devices that are not isolated show a slight increase in off-state I_G over time [Fig. 3(b)], while the on-state I_G is constant. Laser isolation reduces I_G significantly for both cases and does so more effectively than mechanical isolation (Table SII [64]), even though there is the possibility that laser processing may eject positive Si ions from the oxide and could cause a buildup of electrical charge [59,62]. In Te FETs, I_G is drastically reduced (4 orders of magnitude) by sandwiching an OSC layer between Te and the dielectric, and lateral field-effect mobility is enhanced

by the OSC, as we noticed previously [28]. The isolation of Te alone results in I_G less than Te/6PTTP6 not isolated (5 orders of magnitude reduction), but the Te/6PTTP6 bilayer after isolation, in the on state, had the lowest I_G of all. The transfer curves and I_G for representative Te and Te/6PTTP6 devices, before and after isolation, are shown in Supplemental Material (Fig. S4 [64]). Note the lower current scale for the I_G plot after isolation.

The data points in Fig. 3(b) show, counterintuitively, that the on-state leakage current for nonisolated Te/6PTTP6 is considerably lower than for 6PTTP6 alone, even though the Te could greatly expand the area over which leakage could occur because of its much higher conductivity than that of 6PTTP6. It is not clear from the data whether this effect is because of an attribute of the entire film area or of a few distributed defective points. The fact that the lower bilayer on-state leakage current is observed in a set of *isolated* devices as well is evidence for this difference being characteristic of the *entire film*, since the effect is observed at multiple arbitrary locations. This conclusion could not be reached without the isolation procedure.

Note that the off-state I_G is not lower for the bilayer. We attribute this contrast to a polarity resulting from hole transfer between Te and 6PTTP6 resulting in an interfacial dipole with the positive end at Te and the negative end at 6PTTP6 [28]. This polarity reflects depletion of holes in the 6PTTP6, and the on-state gate-to-source voltage, with the gate more negative, would deplete these holes further, and

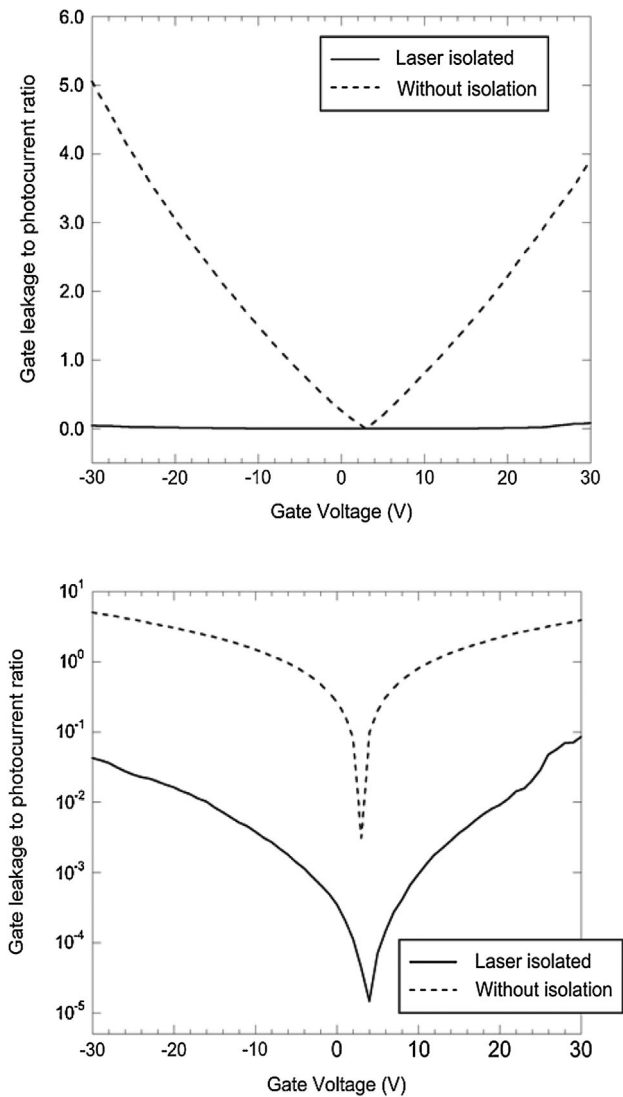


FIG. 5. Linear plot and log plot of measured gate leakage to photocurrent ratio in a representative ZnO/Relc FET. Solid curves are for the sample isolated by the laser; dot-dashed curves are for not isolated.

I_G would decrease. On the other hand, the off-state voltage, where the gate is positive, would reinject holes into the 6PTTP6 and I_G would increase. A similar current-blocking effect is observed for interfaces between Te and aluminum due to diffusion of oxygen through Te grain boundaries and to the semiconductor-metal interface [63]. Injection barriers commonly form due to chemical defects or oxidation between conjugated organic semiconductors and metals, particularly from metals deposited onto OSCs by vapor, but the barriers are typically difficult to observe due to low bulk currents in OSCs [66–69]. In terms of applications, the isolation procedure is clearly helpful in enabling the use of field-effect devices made from low band gap or extrinsically conductive semiconductors.

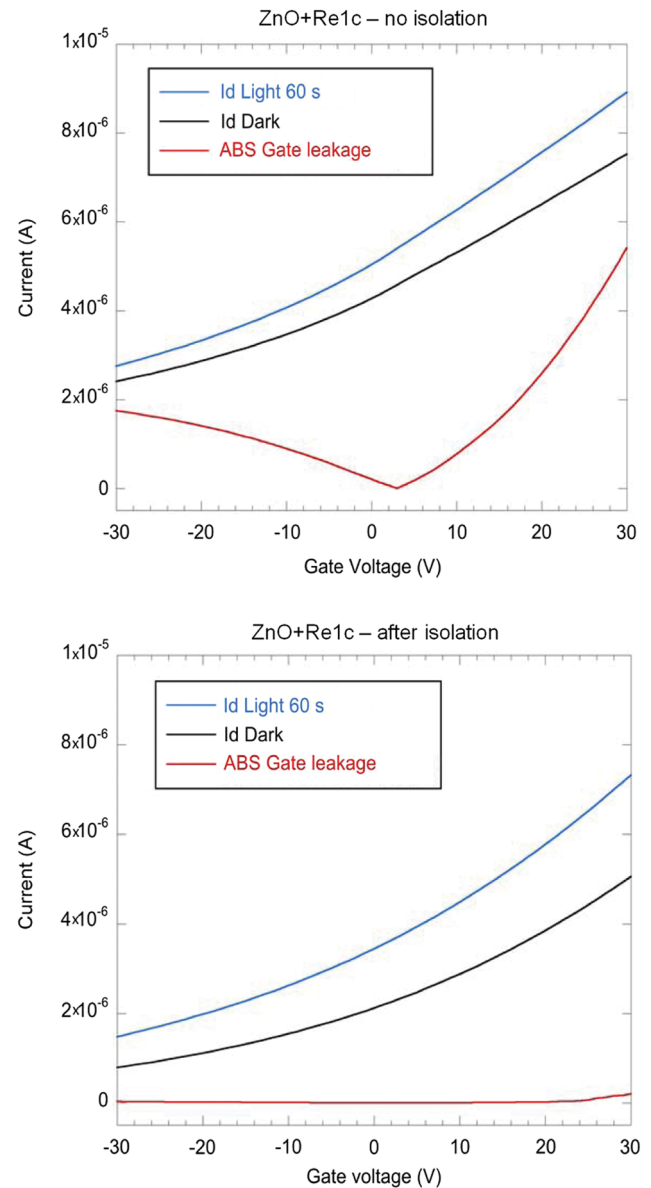


FIG. 6. Transfer curves for photomodulatable ZnO FETs with gate leakage, for devices without and with isolation.

V. CONCLUSIONS

Isolation is critically important for devices where sensitivity and a high signal-to-noise ratio at low power are required. LDW methods are extremely reproducible, and negligible variation in microstructural (i.e., trench depth, line-edge roughness) or FET parameters (i.e., field-effect μ) is observed between samples. Gate leakage is significantly reduced by the LDW method for the devices that we examine here, at least by the geometric area reduction of 2–3 orders of magnitude. The LDW method is shown to be an effective alternative for removing selected domains of both soft semiconductors and metal oxides of certain

relative hardness compared to that of the dielectric, a useful alternative for materials that can be easily damaged by photolithography and chemical etchants. The measured photocurrent for ZnO devices functionalized with donor molecules is initially masked by significant gate leakage current, and that photocurrent is substantially enhanced by the donor as deposited. Similarly, we emphasize that removing parasitic currents allows us to more clearly observe effects and behavior of the intrinsic dipole due to energy alignment of Te-OSC heterojunctions.

The preservation of lifetime characteristics, yield, and performance for devices using semiconductors other than Si will be driven by processing solutions which limit adverse thermal and chemical effects, while providing automation and high-volume scaling. The LDW method can be automated and is scalable, because successive beam splitters can be used to simultaneously pattern multiple arrays of circuits in parallel [70]. Ultrafast pulses allow for noninvasive and selective material ablation, ensuring a clean and precise isolation technique which improves FET electrical performance and eases FET performance assessment, thus making the LDW method a viable patterning alternative.

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