Chirality-Based Vortex Domain-Wall Logic Gates

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(Received 17 January 2014; revised manuscript received 23 May 2014; published 7 October 2014)

We use micromagnetic simulations to demonstrate the feasibility of creating magnetic logic gates that process binary data encoded within the internal magnetization structure of domain walls in ferromagnetic nanowires. In the simulated nanowires, domain walls take the form of magnetic vortices, where the magnetization circulates either clockwise or anticlockwise. By exploiting differences in how these two domain-wall states interact with both notch-shaped defects and junctions in the nanowires, we design nanowire segments that act as NOT, FAN-OUT, NAND, AND, OR, and NOR logic gates. Potentially, these gates could be cascaded to perform any desired logical operation. Our simulations demonstrate the possibility of a class of magnetic devices in which domain walls carry digital information rather than merely delineate it.

DOI: 10.1103/PhysRevApplied.2.044001

I. INTRODUCTION

Understanding the physical behavior and technological applications of domain walls (DWs) in planar ferromagnetic nanowires is currently a subject of intense research interest. In such nanowires, shape anisotropy confines the nanowires' magnetizations to point in one of the two directions along their lengths, and 180° DWs, with characteristic sizes of the order of the nanowires' widths, are formed between oppositely magnetized regions. These DWs have particlelike properties and may be propagated through complex networks of nanowires by using applied magnetic fields [1] or electric currents [2] in a similar manner to that in which electric charge is transported in conventional microelectronics. Experimental studies suggest promising applications in data storage and processing technologies due to the high propagation velocities of the DWs [1] and the intrinsic nonvolatility of magnetic data storage [3,4]. These properties have led to proposals for a range of prototype of DW devices, most famously DW logic [5] and racetrack memory [6].

In currently proposed DW technologies, information is stored by using the orientation of the magnetic domains separated by the DWs, with the magnetization of a given length or section of nanowire representing a single "bit" of information. However, the DWs themselves contain additional degrees of freedom that could hypothetically be used to store and process information. For example, in thick nanowires, DWs favor a vortex-type magnetization structure to reduce their magnetostatic energy [7,8]. In such vortex DWs (VDWs), the magnetization rotates either clockwise (CW) or anticlockwise (ACW) around a central out-of-plane vortex core, depending on the manner in which the DW is nucleated [9,10]. Hypothetically, these two circulation directions, or chiralities, can be used to represent binary 0 and binary 1 such that the DWs themselves act as information carriers, rather than the domains they separate. We note that such a scheme would represent an entirely digital form of data storage, as opposed to the analoglike nature of existing approaches [5], where the DW position, and thus the domain length, can vary continuously. Furthermore, previous results have provided strong evidence that domain-wall chiralities can be the determining factor in the manner in which DWs pass through nanowire networks [10,11].

In this paper, we use micromagnetic simulations to demonstrate the feasibility of nanowire-based logic gates that utilize the chirality of VDWs to store and process information. Logical operations occur by chirality-dependent interactions between DWs and both notch-shaped defects and junctions in the nanowire network. We show that by careful nanomagnetic engineering we can create segments of nanowires that act as NOT, AND, NAND, NOR, OR, and FAN-OUT logic gates. In principle, these gates could be cascaded to build a complete logic architecture.

II. SIMULATION METHOD

To demonstrate the feasibility of a chirality-based logic system, we perform micromagnetic simulations of 40-nm-thick $Ni_{80}Fe_{20}$ nanowires by using the Object Oriented Micro-magnetic Framework (OOMMF) software package from the National Institute of Standards and Technology [12]. Standard magnetization parameters are used to model the magnetic properties of $Ni_{80}Fe_{20}$: saturation magnetization $M_s = 860$ kA/m, exchange stiffness $A = 13$ pJ/m, and magnetocrystalline anisotropy constant $K_1 = 0$. The Gilbert damping constant is chosen to be $\alpha = 0.5$ for all simulations in order to suppress Walker breakdown transformations of the DW structure during propagation (and thus data loss). We note that assigning α this high value is

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physically reasonable, as $Ni_{80}Fe_{20}$ films doped with rare-earth materials have previously been shown to exhibit values of α of this order of magnitude [13]. Cell sizes of $5 \times 5 \times 40$ nm^3 are used for the NOT and FAN-OUT gates, whereas $2.5 \times 2.5 \times 40$ nm^3 cell sizes are used for the NAND, AND, NOR, and OR gates in order to obtain a more accurate rendering of small notch-shaped defects.

We perform all simulations for both tail-to-tail (T2T) and head-to-head (H2H) DWs. However, only results for T2T DWs are presented in this paper. For T2T DWs, binary "1" is assigned to ACW VDWs, and a binary of "0" is assigned to CW VDWs. Our simulations show that the logic gates performed equivalently for H2H VDWs but that the convention for binary 1 and 0 had to be reversed (i.e., ACW = 0 and CW = 1). This reversal reflects the fact that the symmetry of a VDW's spin configuration depends not only on its chirality, but also on its monopole character [14].

III. NOT GATE

In a NOT gate (or invertor), the output signal is the inversion of the input signal. The equivalent operation in our system of logic must therefore transform a CW VDW into an ACW VDW and vice versa. In our simulations, we observe that this transformation could be achieved by driving DWs through a large, double notch-shaped defect (Fig. 1).

Figure 1 demonstrates the NOT gate's functionality for a nanowire with width $w = 150$ nm and length $L = 1500$ nm. Identical triangular notches with depths d_{notch} and widths w_{notch}, both equal to 50 nm, are placed symmetrically at the top and bottom edges of the nanowire. An ACW T2T VDW is relaxed in the right-hand section of the nanowire [Fig. 1(a)1], and an applied field, $\mu_0 H_x$, is then quasistatically increased from 10 to 40 mT in increments of 0.5 mT to propagate a DW across the double notch. We note that the maximum field applied is below the Walker breakdown field (approximately 500 Oe) for the simulated nanowires. Limiting the field in this way ensures that any transformations observed are entirely due to the DWs' interaction with the notches rather than intrinsic dynamical phenomena associated with the DWs' propagation.

The simulation results indicate that, when the ACW VDW reaches the double notch, it encounters an energy barrier that blocks further propagation [Figs. 1(a)2 and 1(a)3]. As $\mathbf{H}_x$ increases, the bottom half of the pinned VDW expands, causing the vortex core to move towards the upper edge of the nanowire. At $\mu_0 H_x = 38$ mT, a new vortex with an inverted CW chirality is nucleated on the left-hand side of the notches [Fig. 1(a)4]. The inverted chirality of the nucleated VDW can be attributed to the uniform orientation of spins in the region between the two cores of the VDWs, which is necessary to avoid magnetic frustration [Fig. 1(a)4]. Finally, at $\mu_0 H_x = 38$ mT, the core of the initial ACW core annihilates at the upper edge of the nanowire and the newly formed CW VDW depins and propagates down the nanowire [Fig. 1(a)5], thus

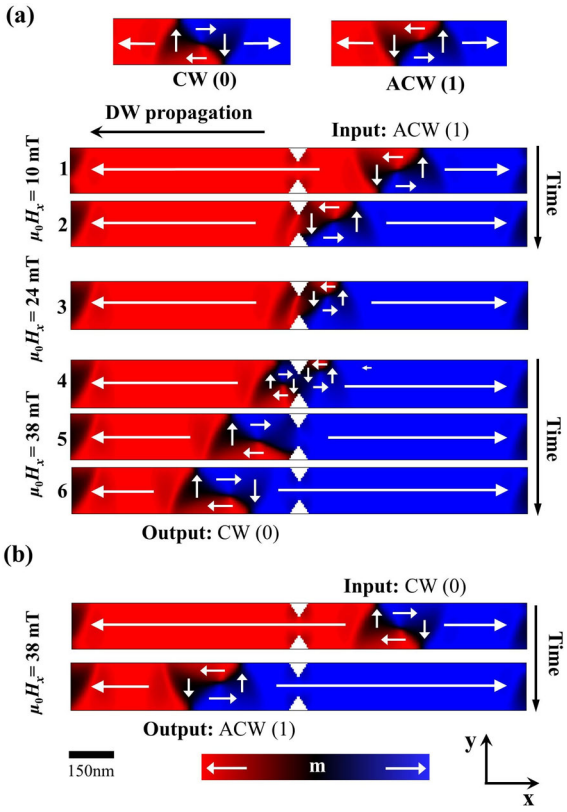

FIG. 1. Micromagnetic simulations illustrating the operation of a VDW NOT gate. The data convention used (CW = 0, ACW = 1) is illustrated at the top of the figure. (a) The input VDW has ACW chirality. (b) The input VDW has CW chirality. Details of the switching process are illustrated only for ACW input but are equivalent for CW input.

demonstrating the chirality-inverting properties of the double-notch defect. Figure 1(b) shows that with a CW VDW as an input the opposite process occurs, with an ACW being output as the result of the inversion process.

It is worth noting that the inversion process described above is observed only for nanowire with thickness $t > 32$ nm and for notches with d_{notch} and w_{notch} larger than approximately 30% of w. For 25 nm $> t > 32$ nm, we still observe inversion of the input DW but by a different magnetization process. In these cases, the original DW becomes transverselike just prior to depinning, and a new vortex is nucleated only after the DW has begun to propagate. Here, the inversion appears to be dependent on the specific manner in which the DW depins from the defect site, and thus we expect that the process would be less reliable and more susceptible to stochasticity than that previously described. For $t < 25$ nm, we observe a further depinning process that did not result in chirality inversion.

IV. FAN-OUT GATE

A FAN-OUT gate has a single input and two outputs that duplicate the input signal. Thus, the two-way FAN-OUT gate

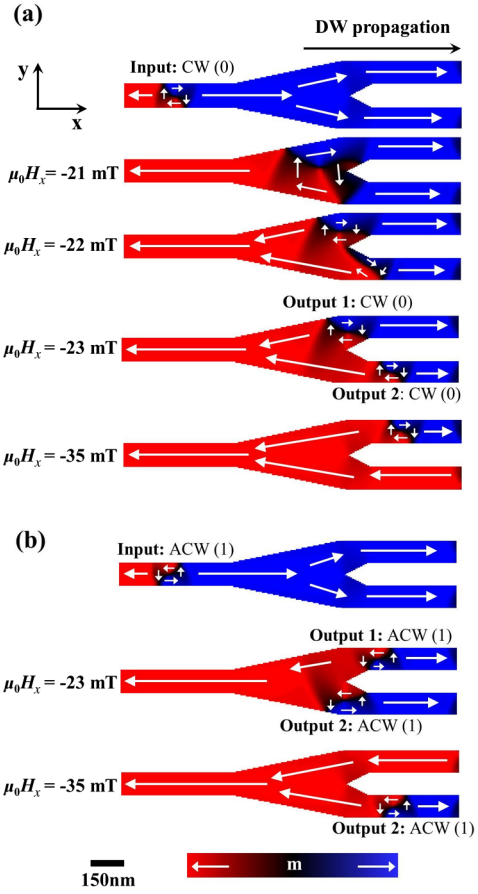

FIG. 2. Micromagnetic simulations illustrating the operation of a FAN-OUT gate. (a) The input VDW has CW chirality. (b) The input VDW has ACW chirality. Details of the switching process are illustrated only for CW input but are equivalent for ACW input.

will propagate two ACW (CW) VDWs from its two output terminals when an ACW (CW) VDW is propagated into its input terminal. In Fig. 2, we present simulations of a nanowire junction that demonstrates this behavior.

The Y-shaped gate has a length of $L = 1500$ nm, input and output nanowires of width $w = 100$ nm, and a junction of width $w = 300$ nm. A T2T CW VDW is initialized at the input terminal and is propagated through the junction by increasing the magnitude of $\mu_0 \mathbf{H}_x$ from 0 to -40 mT in steps of -1 mT. We observe that the DW propagates smoothly until reaching the junction at $\mu_0 H_x = -20$ mT, at which point increasing the magnitude of H_x causes the VDW to expand into the junction while preserving its CW chirality [Fig. 2(a) at $\mu_0 H_x = -21$ mT]. As the applied field is increased further, the region of the vortex where spin alignment is parallel to the applied field starts to expand (in this case, the lower half of the vortex). This expansion causes the core to be pushed upwards until, at $\mu_0 H_x = -22$ mT, the core shifts to the entrance of the output 1. Similar results that show how fractional topological edge defects (and therefore DW chirality) can control the trajectory of VDWs in Y-shaped interconnected nanowires have recently been reported by Pushp *et al.* [10].

The upward shift of the VDW core causes an elongated DW with magnetization pointing along $-y$ to be formed at the entrance of output 2. While the upper section of this boundary remains pinned at the internal apex of the junction, the lower half is free to extend into output 2 as the field further increases. At $\mu_0 H_x = -23$ mT this stretched DW detaches from the apex and forms the leading edge of a new VDW in output 2, thus defining its chirality to match the CW rotation of the input DW. Simultaneously, the original vortex core of the input DW forms a second CW VDW in output 1, thus completing the cloning of input DW chirality into both output nanowires.

Figure 2(b) shows the results of equivalent simulations performed with an ACW DW input. A process mirroring that shown in Fig. 2(a) occurs, resulting in the propagation of ACW DWs through both of the output nanowires.

V. NAND, AND, OR, and NOR GATES

NAND, AND, OR, and NOR logic gates have two inputs which are referenced to unique truth tables to determine the state of the output terminal. Similarly, VDW gates reproducing these operations must consist of Y-shaped junctions with two input wires and one output wire. To analyze the basic behavior of such a junction, we simulate the Y-shaped nanowire system illustrated in Fig. 3. The two nanowires on the left-hand side of the junction are used as inputs, while the single nanowire extending from the right-hand side of the junction is used as the output terminal. The overall length of the Y-shaped gate is 3500 nm. The input nanowires have widths of 150 nm, while the output nanowire has a width of 190 nm.

Initially, we perform simulations to investigate how the chirality of the output VDW depends on the chiralities and arrival sequence of the input DWs. To manipulate the arrival sequence, a triangular notch of depth 50 nm is introduced into the edge of one of the input nanowires [input 1 in Fig. 3(a) and input 2 in Fig. 3(b)], so that one of the two input VDWs will become pinned and propagate into the junction at a later point in the applied field sequence. For each notch position, we perform simulations for both (CW, CW) and (ACW, ACW) input pairs. The VDWs are driven through the junction by sweeping $\mu_0 H_x$ from -15 to -30 mT in steps of -1 mT.

The results of this study are presented in Fig. 3. They show that the chirality of the VDW at the output nanowire depends on the arrival sequence of the VDWs into the junction but not on the chirality of the input VDWs. The mechanism underlying this dependence on arrival sequence can be understood as follows: In Fig. 3(a), the notch is in input 1, and thus VDWs from input 2 arrive at the junction first, irrespective of their chirality. These DWs are pinned between the internal apex of the Y-shaped junction and the

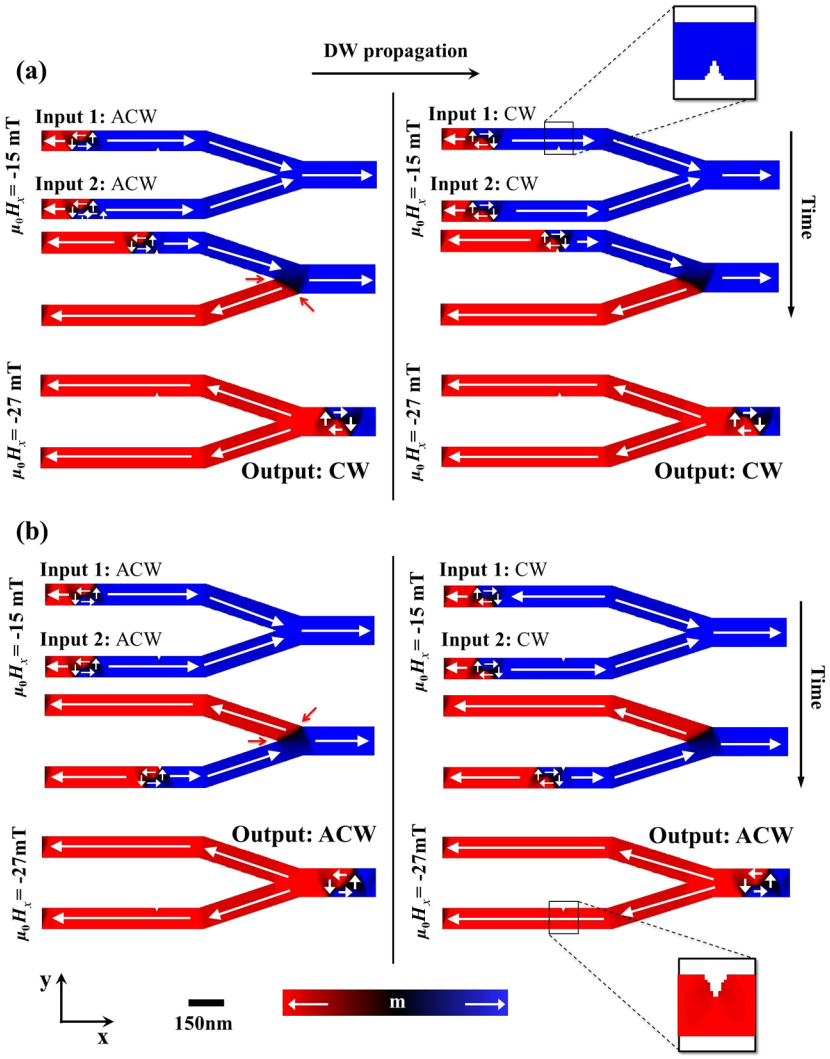

FIG. 3. Micromagnetic simulations investigating how the chirality of a VDW output from a two-in–one-out, Y-shaped junction depends on the arrival sequence and chirality of the input VDWs. (a) A notch is present in "input 1," delaying the arrival of the VDW in this wire. The evolution of the system is illustrated for both CW and ACW input VDW pairs. (b) The notch is present in "input 2." The images enclosed in dashed frames are an enlargement of the notch area.

apex of the corner between input 2 and the output nanowire [indicated by red arrows in Fig. 3(a)], thus giving magnetization of the junction a component along $-y$. As the field is further increased, the second VDW depins from the notch in input 1 and approaches the junction. The tension in the spin configuration between the two DWs causes the DW from input 2 to depin and merge with the DW from input 1 to form a new VDW. The leading edge of this VDW is formed from the preexisting spin configuration at the junction (aligned in the $-y$ direction), and thus the output VDW has CW chirality. Figure 3(b) shows that mirrored behavior occurs when the VDW from input 1 arrives at the junction first [Fig. 3(b)]. In this case, the magnetization of the junction is left with a magnetization component along $+y$ following the arrival of the first DW, yielding a VDW with ACW chirality following the arrival of the second DW.

The simulations described above indicate that the chirality of a VDW output from the Y-shaped junction is entirely controlled by the order in which DWs arrive from the input wires: A CW VDW is produced if the DW from input 2 arrives first, and an ACW VDW is produced if the DW from input 1 arrives first. Therefore, to create junctions that exhibit AND, NAND, OR, and NOR functionality, we must engineer junctions where the arrival order depends on the chirality of the input DWs. In the following, we demonstrate how this can be achieved, by using the example of a NAND gate.

The truth table for a NAND gate is illustrated in Table I. The output is always binary 1 except for the case where both inputs are binary 1, in which case the output is 0. Thus, for a VDW NAND gate, the output should always be ACW except for the case where both input nanowires contain ACW VDWs. As the chirality of the output VDW depends

TABLE I. Logic table used to design the VDW NAND gate.

Input 1	Input 2	Output	VDW required to enter junction first (input 1 or input 2)	Implied depinning field inequality
ACW 1	ACW 1	CW 0	Input 2 (ACW)	$H^{\mathrm{ACW}}_{\mathrm{input\,2}} < H^{\mathrm{ACW}}_{\mathrm{input\,1}}$
ACW 1	CW 0	ACW 1	Input 1 (ACW)	$H^{\mathrm{ACW}}_{\mathrm{input\,1}} < H^{\mathrm{CW}}_{\mathrm{input\,2}}$
CW 0	ACW 1	ACW 1	Input 1 (CW)	$H^{\mathrm{CW}}_{\mathrm{input\,1}} < H^{\mathrm{ACW}}_{\mathrm{input\,2}}$
CW 0	CW 0	ACW 1	Input 1 (CW)	$H^{\mathrm{CW}}_{\mathrm{input\,1}} < H^{\mathrm{CW}}_{\mathrm{input\,2}}$

on the arrival order of the input DWs, correct operation can be achieved only if the VDW in input 1 arrives first, except in the case where both input VDWs have ACW chirality. We control the arrival sequence of the DWs by adding triangular notch-shaped defects to the outer edges of both input nanowires of the Y-shaped junction shown in Fig. 3. VDWs will pin at these notches, impeding their further propagation until a critical field, $H^{\mathrm{ACW\ or\ CW}}_{\mathrm{input\,1\ or\ input\,2}}$, is applied, where the upper suffix indicates the chirality of the pinned VDW and the lower suffix indicates the input wire. It can be deduced from Table I that, to reproduce the function of a NAND logic gate, the inequality $H^{\mathrm{CW}}_{\mathrm{input\,1}} < H^{\mathrm{ACW}}_{\mathrm{input\,2}} < H^{\mathrm{ACW}}_{\mathrm{input\,1}} < H^{\mathrm{CW}}_{\mathrm{input\,2}}$ should be satisfied.

To design notches that satisfy the above inequality, we perform simulations of DW pinning in isolated nanowires with $w = 150$ nm. We place triangular notches at both the upper and lower edges of the nanowire and simulate depinning fields for both CW and ACW vortex DWs.

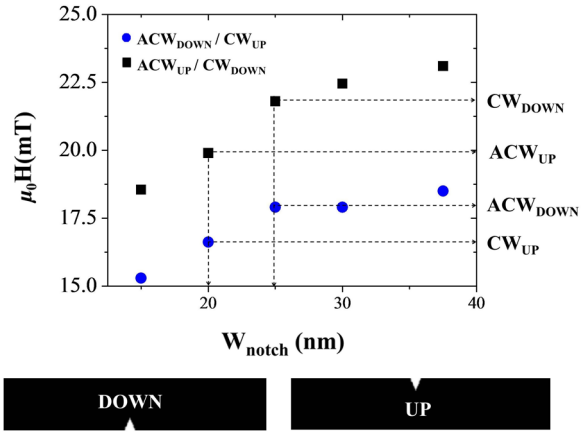

FIG. 4. Graph of the depinning field versus w_{notch} for VDWs in an isolated nanowire. $d_{\mathrm{notch}} = 20$ nm in all cases. Data are shown for notches in both the bottom edge (subscript = DOWN) and top edge (subscript = UP). Data are shown for both CW and ACW VDWs: Blue circles show data for $\mathrm{CW_{UP}}$ and $\mathrm{ACW_{DOWN}}$, while black squares illustrate data for $\mathrm{CW_{DOWN}}$ and $\mathrm{ACW_{UP}}$. The dashed lines indicate the switching fields of notches with $w_{\mathrm{notch}} = 20$ (UP) and 25 nm (DOWN), which satisfy the switching field inequality required for a NAND gate.

The notches have fixed depth $d_{\mathrm{notch}} = 20$ nm and variable width $w_{\mathrm{notch}} = 15$, 20, 25, 30, and 35 nm. The simulated depinning fields are plotted against w_{notch} in Fig. 4.

The simulated depinning fields for an ACW VDW pinned at a defect at the upper edge of the nanowire are greater than those of a CW VDW pinned at the same defect, with the situation reversed for a defect at the lower edge [15,16]. Furthermore, the depinning fields for an ACW VDW pinned at the upper edge are equal to those for a CW VDW pinning at the lower edge of the nanowire and vice versa. This result reflects the fact that the symmetry of a VDW reverses upon changing its chirality [14]. The depinning fields also increase with increasing notch width up to widths of 30 nm, beyond which the data become less linear. In combination, these features provide us with two parameters (notch position and notch width) with which to engineer the depinning field inequality described above. We note that, even with the relatively small 2.5-nm in-plane cell size used in these simulations, the profiles of the notches are not perfectly rendered (see the inset images in Fig. 5). To test the effect of these imperfections on our results, we also repeat these simulations by using a 1-nm in-plane cell size. These simulations showed phenomenological identical results to those in Fig. 4, with small differences (<6.5%) in the simulated depinning field values due to slight changes of the notch's edge profiles. Because of the relatively minor nature of these effects, we continue to use a 2.5-nm in-plane cell size in the following calculations in order to reduce computational overheads.

It can be deduced from Fig. 4 that placing a notch with width 20 nm in the upper edge of input 1 and a second with width 25 nm in the lower edge of input 2 will satisfy the depinning field inequality and thus create the desired VDW arrival sequence for a NAND gate.

To verify the correct operation of the NAND gate, we run simulations for all four sets of possible input combinations (Fig. 5). The applied $\mu_0 H_x$ is increased in magnitude from -10 to -40 mT in steps of -0.5 mT. The full switching sequence of the gate for (ACW, ACW) is shown in Fig. 5(a), while input and output configurations are shown for the other three input combinations in Figs. 5(b)–5(d). In all cases, the output DWs correspond with those expected from Table I, thus demonstrating that the junction successfully replicates the function of a NAND gate.

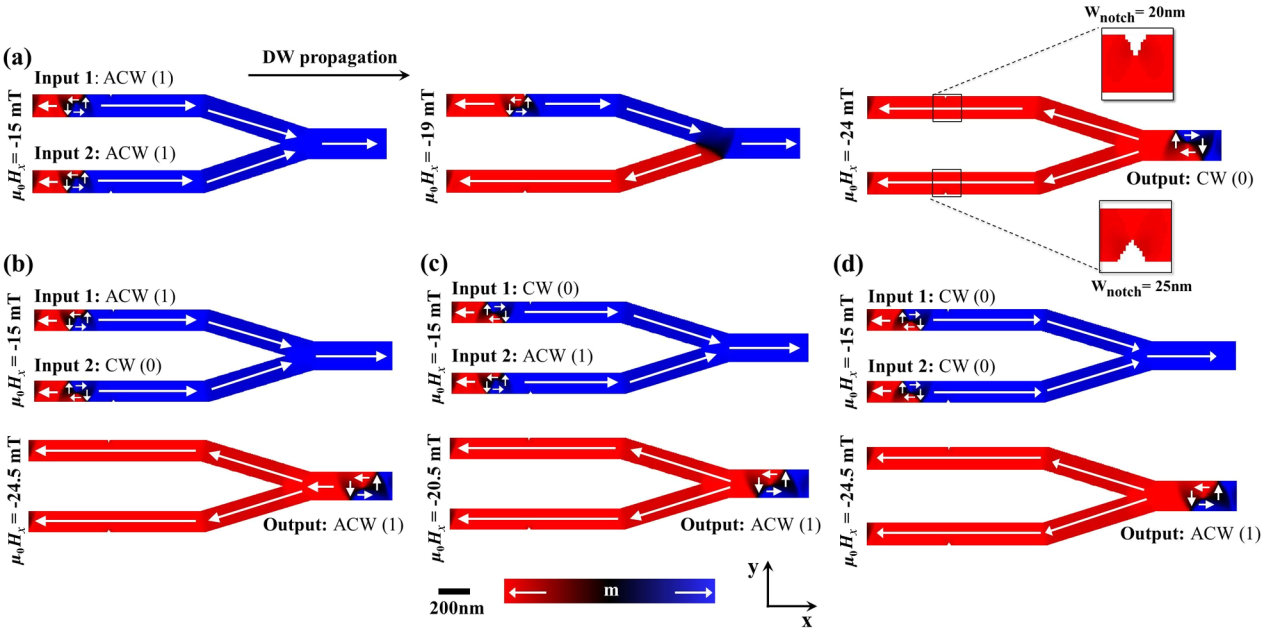

FIG. 5. Micromagnetic simulation illustrating the operation of a VDW NAND gate. (a) Switching of the NAND gate with input 1 = ACW and input 2 = ACW. Images in the dashed frames show enlarged images of notches in each nanowire (d_{notch} = 20 nm). (b) Initial and final states for input 1 = ACW and input 2 = CW. (c) Initial and final states for input 1 = CW and input 2 = ACW. (d) Initial and final states for input 1 = CW and input 2 = CW. Details of the switching process are illustrated only for (a) but are equivalent for all cases.

It is important to note that there are differences in the values of depinning fields from the notches in the Y-shaped nanowire (Fig. 5) compared to those obtained for the isolated nanowire (Fig. 4). These differences are attributed to the coupling effects between the DWs and the junction, both of which carry monopole moments. These interactions assist the depinning of the VDWs.

The same basic architecture used to create the NAND gate can be used to engineer AND, OR, and NOR gates by simply interchanging the sizes and orientation of the controlling notches, in order to alter the arrival sequence of the DWs. The configurations required for AND, OR, and NOR gates are presented in Table II. Simulations are run for each of these gates with all VDW input combinations. Each gate produces output VDWs in agreement with its truth table.

VI. DISCUSSION

The results presented in this paper demonstrate the basic feasibility of designing nanowire segments that replicate the operation of individual logic gates. However, any real logic technology must exhibit five characteristics: namely, a complete set of Boolean operations, gain, nonlinearity, feedback elimination, and concatenability [17]. The main body of this paper already demonstrates that our logic scheme can reproduce a full set of Boolean operations, and thus we will concentrate on the other four requirements here.

Gain is the requirement that the energy used to switch the system or duplicate signals must come from an external source rather than from the input. This requirement is essential to ensure that signal levels do not diminish as data progresses through a series of concatenated gates. In our

TABLE II. Summary of switching field inequalities and notch width and locations required to create NAND, AND, NOR, and OR VDW logic gates, for tail-to-tail magnetization configuration.

Gate	Inequality	Notch at input 1 (location and width)	Notch at input 2 (location and width)
NAND	$H^{CW}_{input\,1} < H^{ACW}_{input\,2} < H^{ACW}_{input\,1} < H^{CW}_{input\,2}$	Outer edge 20 nm	Outer edge 25 nm
AND	$H^{CW}_{input\,2} < H^{ACW}_{input\,1} < H^{ACW}_{input\,2} < H^{CW}_{input\,1}$	Inner edge 25 nm	Inner edge 20 nm
NOR	$H^{ACW}_{input\,2} < H^{CW}_{input\,1} < H^{CW}_{input\,2} < H^{ACW}_{input\,1}$	Outer edge 25 nm	Outer edge 20 nm
OR	$H^{ACW}_{input\,1} < H^{CW}_{input\,2} < H^{CW}_{input\,1} < H^{ACW}_{input\,2}$	Inner edge 20 nm	Inner edge 25 nm

simple system, this energy input comes from the externally applied field, which drives the DWs through the gates. The FAN-OUT gate shown in Fig. 2 provides an excellent example of this, with the energy input of the applied field allowing a single input signal to be cloned into two identical bits.

Nonlinearity requires that the signals used to represent data bits are not analog in nature but are definitive binary states. This requirement is present naturally in our system where clockwise and anticlockwise VDWs are bistable, with no intermediate states.

Feedback elimination requires that input signals uniquely determine output signals and not vice versa. In our system, this requirement can be understood as meaning that VDWs must propagate unidirectionally through the nanowires. We suggest that unidirectional propagation could be achieved by separating individual gates by short orthogonal sections of nanowire, such that they can be isolated from the preceding gate by applying an orthogonal field pulse. Figure 6 illustrates schematically how a pair of input DWs could be passed in order through a NAND gate, a NOT gate, and a FAN-OUT gate using this approach. Furthermore, by employing approaches similar to previously proposed DW "ratchets" [18,19], it may be possible to extend this scheme to allow continuous trains of data carrying H2H and T2T DWs to be propagated through such networks. An alternate approach would be to use geometries similar to those in Ref. [5], where rotating fields are combined with "loop-shaped" circuits to allow unidirectional motion of DW trains.

Finally, for a system to exhibit concatenability, it must be possible for multiple logic gates to be chained together in series. Here, the critical requirement is that the input and output signals take the same form, which is clearly the case in our scheme, where both input and output signals are represented by DW chirality. The propagation method described in the preceding paragraph would also allow the DWs to be driven through sequential gates in a well-defined manner.

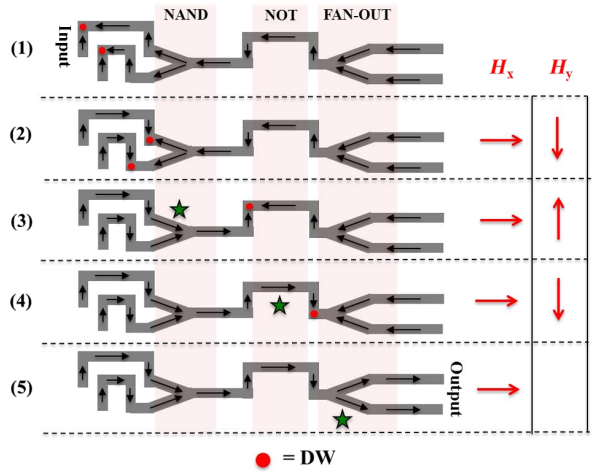

FIG. 6. Schematic diagram illustrating how a pair of DWs could be propagated through NAND, NOT, and FAN-OUT gates connected in series by using a train of orthogonal field pulses. A pulse along H_x and then a pulse along H_y precede each frame in the sequence. The star-shaped symbols indicate the points in the sequence where each gate has performed its operation.

A number of additional challenges still remain before the logic scheme we describe can be investigated experimentally. First, DW pinning and depinning has been widely observed to have stochastic character [20,21], a feature that would clearly disrupt the operation of gates. There are two possible causes of such behavior: Walker-breakdown-induced transformations of the DWs during propagation [22,23] and thermally induced effects once they are pinned [24]. In our simulations, we suppress Walker breakdown phenomena by using a high value of the Gilbert damping parameter ($\alpha = 0.5$). However, values of a similar order have been experimentally demonstrated for $Ni_{80}Fe_{20}$ by doping with rare-earth materials, suggesting that this aspect of our simulations has physical validity [13,25]. We believe that materials with elevated damping will be required to realize chirality-based DW devices, to suppress both stochastic behavior and data loss through dynamical transformations of DW structure. Our simulations do, however, neglect thermal effects, and strategies negating their contributions to stochastic pinning and depinning would have to be developed to successfully implement the logic scheme. Methods for controllably injecting and sensing VDW chirality have also not yet been fully developed. However, a technique for sensing DW chirality by measuring its stray field has been suggested [26], and there is experimental evidence that reliable injection of defined VDW chiralities is possible [9,10]. Furthermore, the operations of the NAND, AND, OR, and NOR gates are at least partially dependent on accurately fabricating pairs of notches with widths that differ by only tens of nanometers. Tolerances this small are likely to present a further practical challenge; however, any pinning method that would yield the desired arrival order of VDW in each gate is expected to produce the same function. Therefore, it may be that in a practical realization it would be preferable to explore further degrees of freedom in the design of the defects, for example, by mixing notches with profiles differing from the triangular shapes used here or utilizing protrusions from the nanowires edges [16], in order to find solutions that are less dependent on fabrication fidelity. Additionally, all current designs for DW devices currently suffer from a lack of truly efficient ways to transport DWs through nanowire networks. Here, we use applied fields to transport the DWs, which could be practically realized by fabricating nanowire networks on top of micropatterned strip lines. However, while this demonstration would be undoubtedly feasible in a laboratory, it may not ultimately prove to be a low-power approach in real devices [5]. Spin-torque effects [2] offer a further option (and a natural method of

transporting DWs unidirectionally) but may also require high current densities.

Finally, it should be noted that the simulations presented in this paper are performed in a quasistatic fashion, with the magnetization being allowed to relax to a stable configuration between field steps. In a real device, where competitive clock speeds of approximately 100 MHz would be required, this quasistatic approximation would not be valid, and thus it is important that the behaviors of the logic gates are investigated in the dynamic regime. As a preliminary investigation, we perform simulations where the field is ramped to a maximum in 10 ns and then held constant. We find that all gates perform as expected, although slight modifications to the geometry of the FAN-OUT gate are required to avoid erroneous DW nucleation from the nanowire junctions, while in the case of the NAND gate the maximum field has to be carefully tuned to 32 mT in order to prevent the output DW undergoing an anomalous transformation upon leaving the junction. Output DWs are produced within approximately 20 ns of the start of the field pulse, suggesting that clock speeds of approximately 50–100 MHz should be accessible relatively easily. Further studies will undoubtedly be required to gain a full understanding of the behavior of logic gates in the dynamic regime and to demonstrate propagation through multiple gates under a continuous external clock.

VII. CONCLUSIONS

In conclusion, we present micromagnetic simulations that demonstrate the feasibility of magnetic logic gates that use the internal spin structure of vortex DWs in planar magnetic nanowires to both encode and process information. Our designs exploit chirality-dependent interactions with both defects and nanowire junctions to create nanowire segments that exhibit NOT, FAN-OUT, AND, NAND, OR, and NOR-like functionality. The gates are expected to be cascadable and thus represent the fundamental elements of a complete nanomagnetic logical architecture. While a number of challenges remain before such an architecture can be implemented experimentally, our work demonstrates the possibility of a generation of devices where DWs are used to carry, rather than merely delineate, information.

ACKNOWLEDGMENTS

This work is supported by the Engineering and Physical Sciences Research Council (Grant No. EP/J002275/1). The authors thank Dr. Dan Allwood for useful discussion.

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