Device Physics of Vertical Static Induction Transistors

Yiyang Luo,[‡] Kairong Huang,[‡] Xiaoci Liang, Hanjing Ke, Sujuan Hu, Qian Wu, Baiquan Liu,[*] and Chuan Liu[†]

State Key Laboratory of Optoelectronic Materials and Technologies and the Guangdong Province Key Laboratory of Display Material and Technology, School of Electronics and Information Technology Sun Yat-Sen University, Guangzhou 510275, China

(Received 2 October 2022; revised 19 January 2023; accepted 17 February 2023; published 29 March 2023)

Vertical static induction transistors (SITs), with vertically arranged source, porous gate, and drain electrodes, were proposed in 1950s and have recently gained new attention because of their suitability as flexible substrates and for hybrid integration with light-emitting diodes. However, the understanding of them is hindered by Schottky gate leakage and relies on case-by-case simulations. Here, we derive concise expressions for the channel potential and current-voltage characteristics for ideal SITs, including the subthreshold swing, threshold voltage, and above-threshold region. The theory is verified by two-dimensional device simulation and agrees well with the reported experimental results. An ideal SIT can be approximated as a partially gated transistor in parallel with a resistance and needs a sub-500-nm pore diameter to exhibit sharp switching in transfer scanning and good saturation in output scanning. The proposed theories connect the device structure and electrical characteristics of SITs concisely, and conclusions are also applicable to permeable base transistors.

DOI: 10.1103/PhysRevApplied.19.034096

I. INTRODUCTION

Field-effect transistors (FETs) have been key components for logic computations, information display, biosensing, optoelectronics, etc. [1–3]. To meet the rapidly increasing demands for high-resolution displays, such as organic light-emitting diodes (OLEDs) and micro-LEDs, FETs should work under conditions of high operation frequency and current density [4–6]. Shortening the channel length L is the most direct way to ensure this, but this suffers from high production costs in an expensive lithography process [7,8]. Another alternative approach is the use of a vertical FET, whose vertical channel length is the submicron thickness of the semiconductor. Because of vertical transport, vertical FETs exhibit the benefits of submicron-channel FETs, and have great potential for integrating with OLEDs and applications in flexible electronics [9–11]. Therefore, vertical FETs have aroused attention in recent years and have been applied with organic semiconductors, oxide semiconductors, two-dimensional (2D) materials, and other novel materials, such as perovskite [11–16].

Among various vertical FETs, vertical static induction transistors (SITs) were proposed under the name "analogue transistors" as early as the 1950s [17]. They are also known as vertical triode and space-charge-limited transistors [9–11,18,19], achieved with inorganic semiconductors (SiC [20], GaAs [21], GaN [22,23], etc.) and organic semiconductors (also taking the form of an organic permeable base transistor) [24–26]. A summary of various types of SITs is shown in Fig. 1. In permeable base transistors, the vertical field between the emitter and collector drives carriers to transport vertically. The potential of the base electrode (gate) controls whether the carriers pass through the nanometer-sized pinholes in the base. One of the significant advantages of SITs is the feasibility of getting a cutoff frequency higher than that of lateral FETs due to the short channel length [26]. Permeable base transistors have achieved a record high transition frequency of 40 MHz [27] and the expected frequency is over 1 GHz [38], but such devices are still limited by reproducibility in fabrication processes [39]. In comparison, SITs can be regarded as the modified version of organic permeable base transistors as shown in Fig. 2(a), where the dielectric layers are covered above and below the porous base electrode. For SITs, it is possible to have low off-state current and to optimize the device performance by altering the aperture on the base electrode or the thickness of the semiconductor. However, despite the proposed mechanisms for the operation of permeable base transistors [40–43], clear device physics and concise current-voltage relations for complicated SITs are still lacking. Although vertical FETs have been extensively studied by experiments and numerical simulation [44–46], efforts to predict their operation with analytical models or

[*]liubq33@mail.sysu.edu.cn
[†]liuchuan5@mail.sysu.edu.cn
[‡]These authors contributed equally.

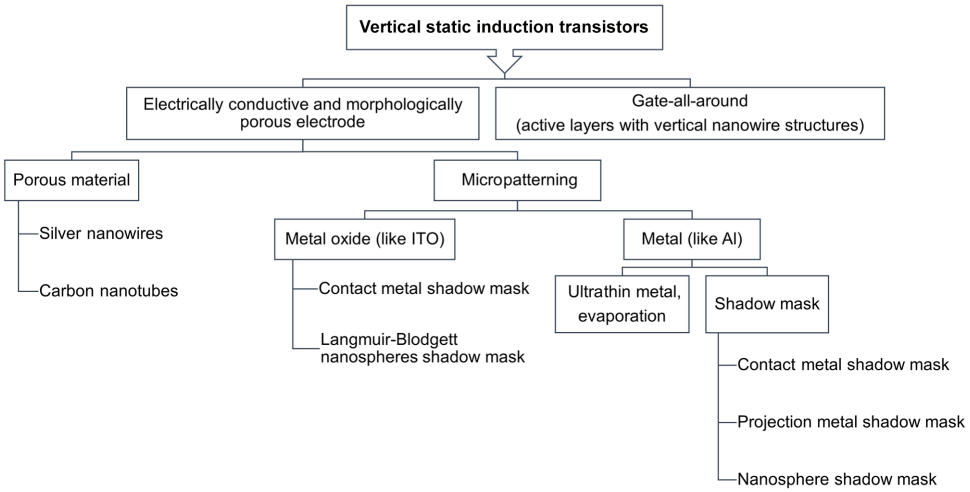

FIG. 1 Categories of vertical static induction transistors, summarized from references [21,22,26–37].

simplified models have mainly focused on vertical transistors with an electrode arrangement different from that of SITs; in the modeled transistors, drain, source, and gate have been arranged from the top to the bottom [47,48].

In this work, the device physics and electric performance of vertical SITs are investigated. We first discuss the ideal structure of SITs and the mechanisms by device simulation, especially considering how to prevent the reverse current. Then, we derive the expressions for electrostatic potential inside the channel region and the current-voltage equations of SITs according to the equivalent circuit. Based on these theories, we establish the connection between the structural parameters and electrical properties in subthreshold, transfer, and output characteristics, which are also applicable to permeable base transistors. Finally, we conclude with suggestions on optimizing device structure for designing and fabricating SITs.

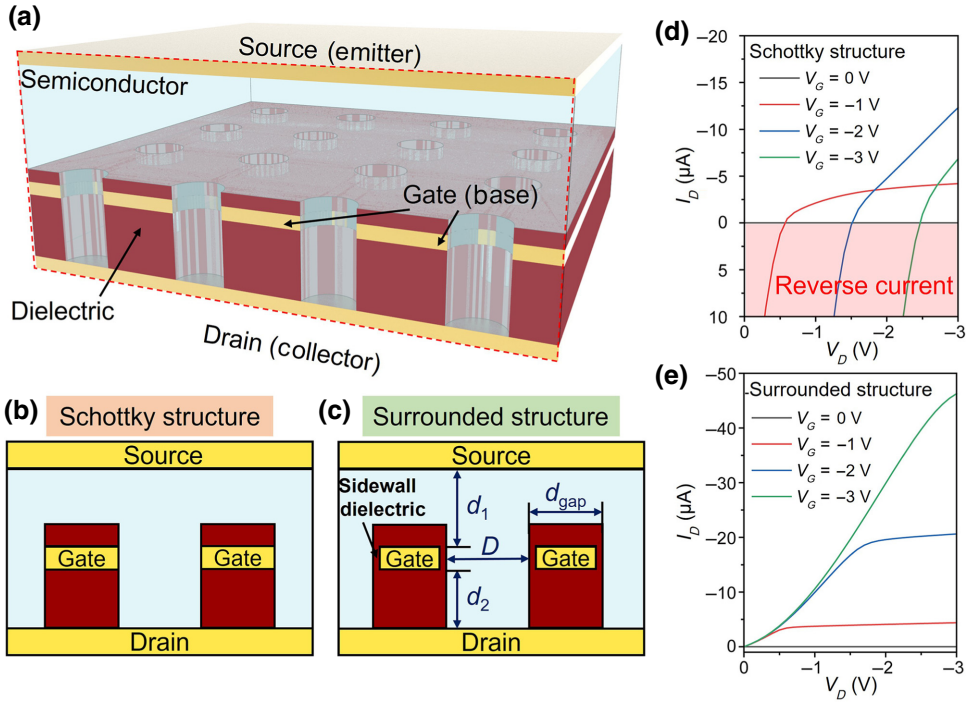

FIG. 2 Device concepts and simulated electrical properties. (a) Device structure of a SIT. (b),(c) Cross-sectional views of SITs in Schottky structure and surrounded structure, respectively. (d),(e) Simulated output curves of SITs in Schottky structure and surrounded structure. For *p*-type semiconductors, the positive drain current is identified as the reverse current.

II. IDEAL VERTICAL STATIC INDUCTION TRANSISTORS

According to the fabrication processes of SITs, the porous aluminum gate electrodes are usually made using top-down methods, such as the polystyrene sphere lift-off method or nanoimprinting [10,11,19]. Then, oxygen plasma treatment is applied to etch a channel area and to form aluminum oxide as the top dielectric layer, suppressing leakage current between gate and top electrodes. However, in some simulation studies, gate electrodes are surrounded by the oxide dielectric layer [49]. These two structures are referred to here as "Schottky structures" without the sidewall dielectrics with Schottky leakage [17] [Fig. 2(b)] and "surrounded structures" with the sidewall dielectric SITs [Fig. 2(c)]. We investigate them by simulation using technology computer-aided design (TCAD) with the material and geometric parameters summarized in Supplemental Material Table S1 [50]. The following study is based on a p-type channel and the discussion can also be applied to an n-type channel. The basic equations for numerical simulation include the Poisson equation, carrier continuity equations, and drift-diffusion equations learned from the theory of semiconductor physics and device principles [51]. The boundary conditions are set as Dirichlet boundary conditions for Ohmic contacts, where the surface potential ϕ_s and the carrier concentration are continuous. In the case with an injection barrier height ($q\phi_b$) at the metal-semiconductor interface, Schottky contacts are modeled and the surface potential is given by $\phi_s = \chi + E_g/(2q) + \ln(N_C/N_V) \times kT/(2q) - \phi_{SD} + V$, where the work function of the source or drain electrodes $\phi_{SD} = \chi + E_g/q - \phi_b$, in which χ is the electron affinity potential, E_g is the band gap, k is the Boltzmann constant, T is temperature, N_C and N_V are effective density of the conduction band and valance band, and V is the applied bias. The setting of the mesh and region in the simulation are shown in the Supplemental Material for the single-gate device and multigate device.

In the Schottky structure [Fig. 2(b) and the left panel of Fig. 3], gate electrodes are in direct Schottky contact with semiconductors. The equivalent circuit is that two Schottky diodes are connected back-to-back [Fig. 3(e)]. As in a bipolar junction transistor, the source-gate (emitter-base) diode and drain-gate (collector-base) diode operate in forward and reverse bias, respectively. The simulated I-V curves are distinct from those of conventional FETs, as shown in Fig. 2(d) and Supplemental Material Fig. S2 [50]. If V_D satisfies $|V_D| > |V_G + V_{BI}|$, where V_D and V_G are the applied voltages of drain electrode and gate electrode, respectively, V_{BI} represents the built-in voltage of the Schottky diode, the drain-gate diode operates in forward bias and the device exhibits a large positive drain current. The leakage current flows into the gate from both the source and drain electrodes [Fig. 3(a) and 3(d)] and causes unstable current directions, narrowing its effective working region [32]. Although the reverse current can be suppressed with Schottky contact in the drain (collector)

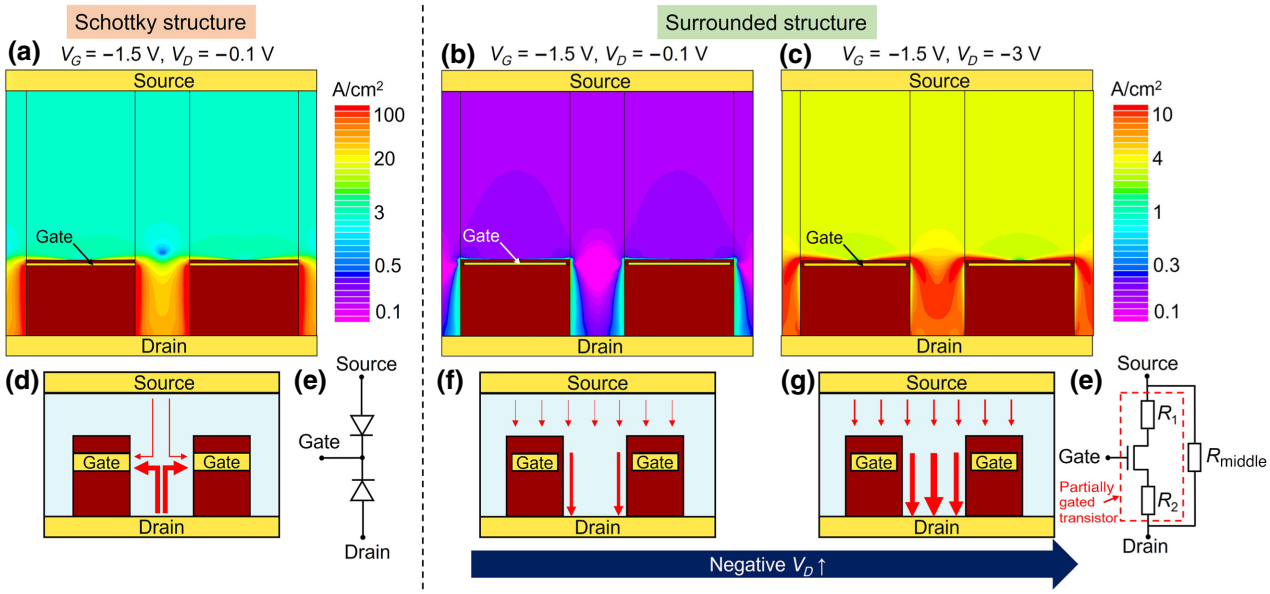

FIG. 3 Current distribution and device operation. (a)–(c) TCAD-simulated 2D distribution of current density in the semiconductor of Schottky and surrounded structures. (a) Schottky structure with the applied voltage of $V_G = -1.5$ V and $V_D = -0.1$ V. (b),(c) Surrounded structure with the applied voltage of $V_G = -1.5$ V and $V_D = -0.1$ V, or $V_G = -1.5$ V and $V_D = -3$ V. (d) Schematic representations of the current direction for Schottky structure corresponding to (a). (e) Equivalent circuit of Schottky structure. (f)–(g) Schematic of current direction and operation mode for surrounded structure corresponding to (b),(c), respectively. (h) Equivalent circuit of surrounded structure. R_1 and R_2 represent the resistances of the nongated channels near the source and drain, respectively.

electrodes, the overall current would be reduced [18], as simulated in Supplemental Material Figs. S2(c) and S2(d) [50]. Schottky contacts are used in the simulation of the Schottky structure in Sec. II [Figs. 2(d) and 3(a)], whereas Ohmic contacts are used for the simulation of the surrounded structure in Secs. II–V (Figs. 2(e), 3(b), and 3(c), and all the other figures).

In comparison, the surrounded structure [Fig. 2(c) and the right panel of Fig. 3] is more like a traditional transistor. The surrounded dielectric layers eliminate the gate leakage (Supplemental Material Fig. S3 [50]). To have large injection areas, the top electrodes, rather than the bottom ones, are taken as the source electrodes (Supplemental Material Fig. S4 [50]). The surrounded structure SIT can be taken as a partially gated transistor and a resistance R_{middle} in parallel [Fig. 3(h)]. For example, at $V_G = -1.5$ V and $V_D = -0.1$ V, injected carriers mostly transport along the interface of the dielectric layer (near the sidewall of the pores) due to the much lower resistance [Figs. 3(b) and 3(f)]. When increasing $|V_D|$, the resistance controlled by the gate gradually increases, but the resistance of the pore channel R_{middle} gradually decreases (as explained in Sec. V) [52], so that most carrier transport and current density are in the middle of the pore [Figs. 3(c) and 3(g)].

According to these results, the surrounded structure is more in accordance with reported experimental results in the references as listed previously, indicating that the oxide dielectric layers may surround the porous electrodes after O_2 plasma treatment in SITs. The structure is somewhat similar to gate-all-around (GAA) transistors [53,54] or permeable base transistors if the pore diameter is in the submicron scale. As the spontaneous sidewall dielectrics may not be enough to prevent leakage current at high voltages, additional surrounding dielectrics on the porous gates are needed [55]. We focus on the surrounded structure SIT in the following.

III. ELECTROSTATIC POTENTIAL

The electrostatic potential within the semiconductor near the gate is related to carrier density and electric field, and needs to be understood to reveal the device physics and working mechanism of the SIT. The potential distribution is first discussed for separate, single-gate electrodes and then for dense, adjacent gate electrodes. Note that the following surrounded structure model cannot be directly used for the Schottky structure as the latter case has leakage current from the gate to the source or drain electrodes.

First, when the pore diameter D is large, the coupling between gate electrodes is negligible and the transistor can be regarded as having separate single gates. In the horizontal plane [the red dashed line in Fig. 4(a)], the influence of the vertical field is assumed to be equal. The potential of the gate electrode (at $x = -20$ nm) is set as zero when $V_G = 0$ V. The potential within the semiconductor $\phi(x)$ follows the Poisson equation

$$\frac{d^2\phi(x)}{dx^2} = \frac{-\rho(x)}{\varepsilon_{\text{SC}}}. \tag{1}$$

The electric displacement vector $\vec{D}$ is assumed to be continuous at the semiconductor-dielectric interface [56], i.e., possible free charges at the interface are not considered,

$$\vec{D} = \vec{E}_{\text{SC0}}\varepsilon_{\text{SC}} = \vec{E}_{\text{ox0}}\varepsilon_{\text{ox}}, \tag{2}$$

where ε_{SC} is the permittivity of the semiconductor and $\rho(x)$ is the total space-charge density, ε_{ox} is the permittivity of the dielectric, E_{SC0} and E_{ox0} are the interface electric field of the semiconductor and dielectric, respectively. Notice that the impacts of fringe fields and boundary conditions away from the gate have been included in the numerical simulation (see Supplemental Material Figs. S6 and S7 [50]). Even though fringe fields and boundary conditions at the semiconductor-dielectric interface away from the gate are not included in our theory of $\phi(x)$, the concise model captures the potential provided by numerical simulations except for one case. This is shown in detail in the following.

To give a simplified solution, we consider carrier density to be related to the local potential $\phi(x)$ by a Boltzmann distribution and use the approximation expansion in Eq. (1) (see Supplemental Material for details [50]). The solutions in the semiconductor ($x > 0$) or the dielectric ($x < 0$) are simplified as [48]

$$\phi(x) \cong \phi_\infty + (\phi_0 - \phi_\infty)exp\left(-\frac{x}{L_D}\right), \ (x \geq 0); \tag{3}$$

$$\phi(x) = \phi_0 + \frac{\phi_0 - V_G}{t_{\text{ox}}}x, \ (x < 0), \tag{4}$$

where t_{ox} is thickness of sidewall dielectric; L_D is the Debye length, $L_D = \sqrt{\varepsilon_{\text{SC}}kT/[q^2(p_0 + n_0)]}$; k is the Boltzmann constant; T is the temperature in kelvins; p_0 and n_0 are hole density and electron density, respectively, at $x = \infty$; and ϕ_0 and ϕ_∞ are the potentials at $x = 0$ and $x = \infty$, respectively. To better describe the practical transistors, the stretched exponential form $(x/L_D)^\gamma$ replaces (x/L_D), due to the simplified first-order Taylor expansion [48]. For the boundaries, ϕ_0 can be solved by substituting E_{SC0} and E_{ox0} [the derivatives of Eqs. (3) and (4)] into Eq. (2). Then ϕ_∞ could be solved as the potential along the y direction at $x = \infty$ approximates the linear distribution $E = [(\phi_\infty - (V_S + \phi_{\text{BI}})]/d_1 = (V_D + \phi_{\text{BI}} - \phi_\infty)/d_2$. Here, ϕ_{BI} represents the built-in potential between semiconductor and gate, $\phi_{\text{BI}} = \phi_b - (E_F - E_V)/q$; d_1 and d_2 are film thickness as illustrated in Fig. 2(b); E_V and E_F are the maximum energy of valance band and Fermi energy,

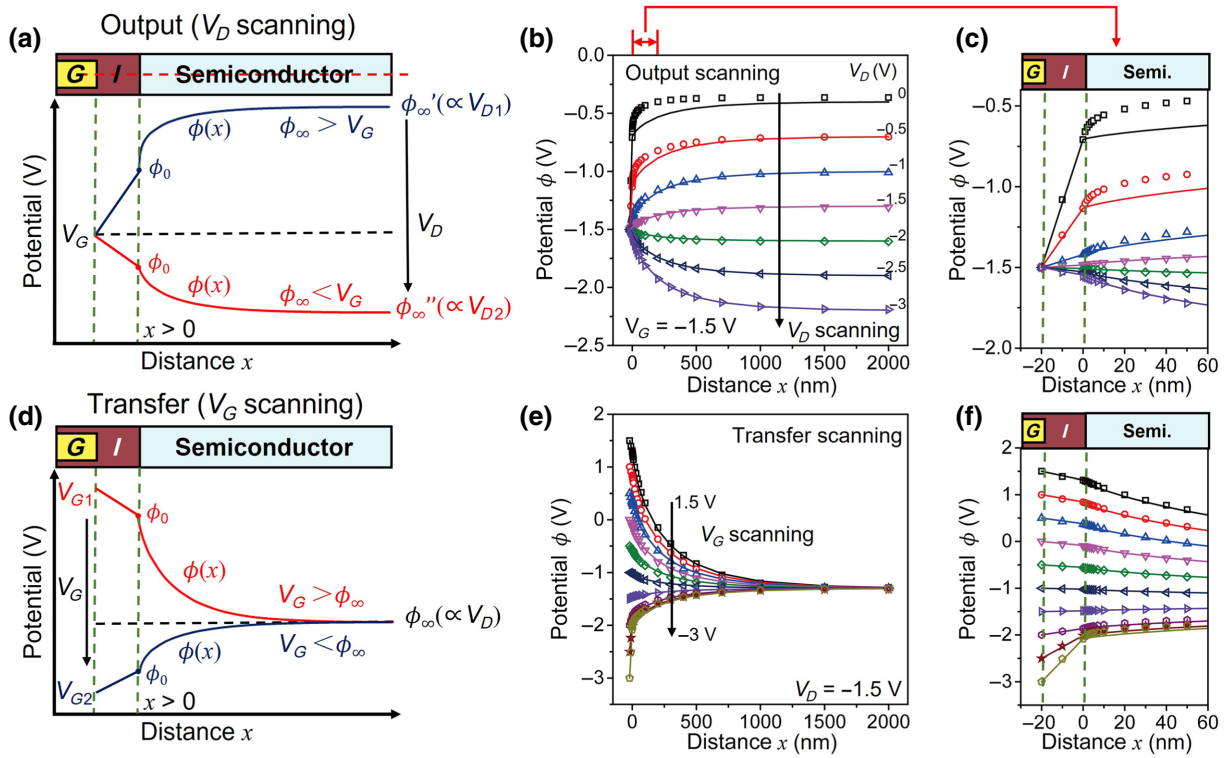

FIG. 4 Potential distribution along the gate electrode in a single-gate electrode device. (a) Schematic shows the potential along the gate electrode $\phi(x)$ at various V_D and fixed V_G, corresponding to output characteristics. (b) The $\phi(x)$ as a function of x at output scanning at $V_G = -1.5$ V, $V_D = 0$ to -3 V. (c) Enlargement of (b) at the interface of the gate electrode. (d) Schematic of $\phi(x)$ at various V_G and fixed V_D, corresponding to transfer characteristics. (e) The $\phi(x)$ as a function of x in transfer scanning at $V_D = -1.5$ V, $V_G = 1.5$ to -3 V. (f) Enlargement of (e) at the interface of the gate electrode. In (b),(c),(e),(f) dots are TCAD simulation, and the curves are fitted by Eqs. (3) and (5).

respectively; ϕ_b is energy offset between gate work function and E_V; and the source electrode is grounded with $V_S = 0$ V. The solutions of ϕ_0 and ϕ_∞ are

$$\phi_0 = \frac{C_{\rm ox}}{C_{\rm ox} + C'_{\rm SC}} V_G + \frac{C'_{\rm SC}}{C_{\rm ox} + C'_{\rm SC}} \phi_\infty; \tag{5}$$

$$\phi_\infty = \phi_{\rm BI} + \frac{d_1}{d_1 + d_2} V_D. \tag{6}$$

Here $C'_{\rm SC} = \gamma \varepsilon_{\rm SC} / L_D^\gamma$ represents the corrected semiconductor capacitance. The Eqs. (3)–(6) describe potential distributions in the horizontal direction.

The Eqs. (3)–(6) are used to fit the extracted potential from the 2D simulated device in output scanning [Fig. 4(a)], where the potential $\phi(x)$ has a fixed V_G and varying ϕ_∞ due to scanning V_D, and in transfer scanning [Fig. 4(d)], where $\phi(x)$ has a fixed ϕ_∞ (due to the fixed V_D) and varying V_G. In the off-state with $V_G > \phi_\infty$ [Figs 4(a) and 4(d), red curves], the theory of $\phi(x)$ provides a good fit in both transfer and output scanning to numerical simulation, as shown in Figs. 4(b) and 4(e), including the semiconductor-dielectric interface [Figs. 4(c) and 4(f)]. The same set of parameters ($L_D = 245$ nm, $\gamma = 0.77$, $d_1 = 0.75$ μm, $d_2 = 0.5$ μm) are used, where d_1 is smaller than that in the simulated device because of the band bending around the contact between the source and semiconductor. Here, L_D, d_1, and d_2 are fixed, γ is the fitting parameter, and ϕ_0, ϕ_∞, and $\phi(x)$ are calculated by using Eqs. (3)–(6). In the on-state with $V_G < \phi_\infty$ [Figs. 4(a) and 4(d), blue curves], holes are accumulated at the semiconductor-dielectric interface, which prevents the gate electric field from penetrating into the semiconductor and results in a sharp increase of potential. Thus, ϕ_0 cannot be directly calculated from the previous analysis and the extracted values are substituted into the model. The concise model and the simulations are generally consistent except for the cases with a small $|V_D|$ (e.g., $V_D = 0$ or -0.5 V). This is because, when $V_G < \phi_\infty$ (i.e., small $|V_D|$), many carriers are accumulated at the sidewall of the dielectric, leading to a sharp increase in the electric displacement vector, and the approximation given by Eq. (2) is not applicable. Nevertheless, the theory is generally consistent with the simulation results.

Second, when the pore diameters are small, the coupling effects from the adjacent gate electrodes should

be considered. The potential distribution is symmetric with respect to the center of the pore ($x = D/2$), i.e., $\phi(x=0) = \phi(x=D)$. Thus, $\phi(x)$ in Eq. (3) for a single gate should be rewritten for the multigate case. First, $\phi(x)$ within the gate dielectric ($x < 0$ or $x > D$) is

$$\phi(x) = \begin{cases} \phi_0 + \frac{\phi_0 - V_G}{t_{ox}} x, & (x < 0) \\ \phi_0 + \frac{\phi_0 - V_G}{t_{ox}} (D - x), & (x > D) \end{cases}. \quad (7)$$

The boundary ϕ_0 is (see Supplementary Material for details [50])

$$\phi_0 = \frac{C_{ox}}{C_{ox} + C''_{SC}} V_G + \frac{C''_{SC}}{C_{ox} + C''_{SC}} \phi_\infty,$$

where $C''_{SC} = d\eta(x)/dx|_{x=0}\varepsilon_{SC}$ denotes corrected semiconductor capacitance for simplicity [50]. Here,

$$\eta(x) = 1 - \exp\left[-\left(\frac{x}{L_D}\right)^\gamma\right] + exp\left[-\left(\frac{D}{L_D}\right)^\gamma\right] - \exp\left[-\left(\frac{D-x}{L_D}\right)^\gamma\right]$$

increases with D and is between 0 and 1 (γ is close to 1). Second, $\phi(x)$ within the semiconductor ($0 \le x \le D$) is

$$\phi(x) = \phi_0 + \left(\phi_{BI} - \phi_0 + \frac{d_1}{d_1 + d_2} V_D\right) \eta(x) \approx [1 - \eta(x)] V_G + \eta(x) \left(\frac{d_1}{d_1 + d_2}\right) V_D + \eta(x)\phi_{BI}, \quad (0 \le x \le D), \quad (8)$$

where ϕ_{BI} is the built-in potential between the semiconductor and the gate. The approximation in Eq. (8) holds when the dielectric thickness is very thin so that $C''_{SC} \ll C_{ox}$. The Eqs. (7) and (8) describe the potential distribution along the gate electrodes in SITs. For SITs with different pore diameters, $\phi(x)$ is extracted during transfer or output scanning [dots in Figs. 5(c)–5(f)]. The calculated potential distributions are highly consistent with the numerical simulation results [curves in Figs. 5(c)–5(f)]. We perform a simulation for the multigate case (using the zero derivative at the boundaries) and extract one of them to show in Figs. 5(c)–5(f), as the potential distributions in different pores are almost the same. The fitting parameters for

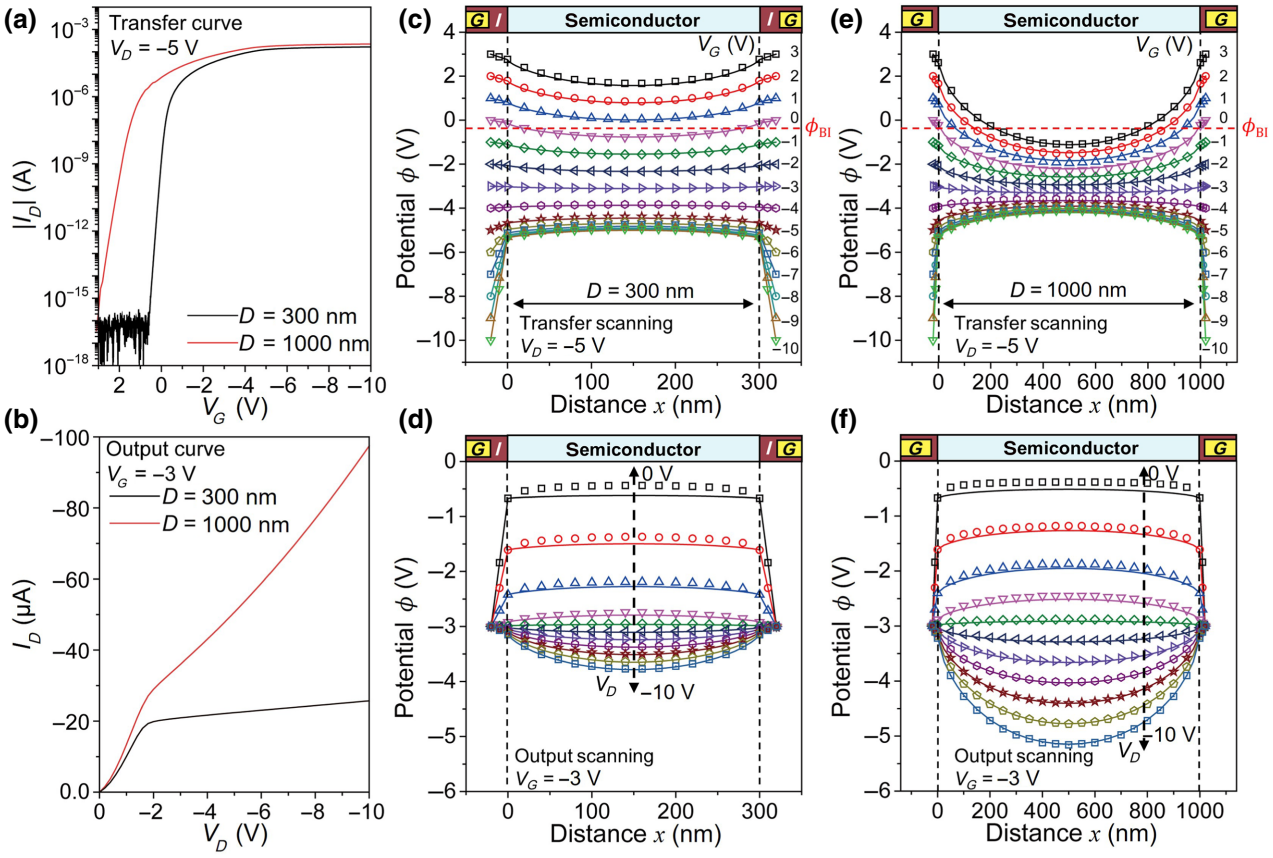

FIG. 5 Potential distribution with different pore diameters D and the impacts on electric characteristics. (a) Transfer curves for SIT with $D = 300$ or 1000 nm at $V_D = -5$ V, $V_G = 3$ to -10 V. (c),(e) The potential $\phi(x)$ distribution in SIT with $D = 300$ or 1000 nm corresponding to the scanning in (a). (b) The output curves for SIT with $D = 300$ or 1000 nm at $V_G = -3$ V, $V_D = 0$ to -10 V. (d),(e) The $\phi(x)$ with $D = 300$ or 1000 nm corresponding to the scanning in (b). In (c)–(f) dots are TCAD-simulation and curves are fitted by Eqs. (7) and (8).

Eq. (8) are $L_D = 410$ nm and $\gamma = 0.77$ when $D = 300$ nm, and $L_D = 310$ nm and $\gamma = 0.74$ when $D = 1000$ nm. The values of d_1 and d_2 are fixed at 0.8 and 0.5 μm, respectively. Along the horizontal direction, the electric field changes gradually within the semiconductor, whereas it sharply increases near the semiconductor-dielectric interface and at the corners under the gate electrodes in the case with a small $|V_D|$ and a large $|V_G|$.

This theory well explains the characteristics of the SIT. In transfer scanning, the potential $\phi(x)$ is pulled down by fixed V_D [Figs. 5(c) and 5(e)]. With a small D [300 nm, Fig. 5(c)], as the proportion of the relative change in potential $\eta(x)$ [defined following Eq. (7)] is small, the potential $\phi(x)$ is mainly determined by V_G and exhibits stronger V_G regulation, as compared with the device with a large D [1000 nm, Fig. 5(e)]. As a result, the transfer curve with a small D [Fig. 5(a), black] shows stronger V_G regulation, smaller subthreshold swing (SS), and near-zero threshold voltage (V_{th}), compared with that having a large D [1000 nm, Fig. 5(a), black]. In output scanning [Figs. 5(b), 5(d), and 5(f)], the device with a large D [1000 nm, Fig. 5(f)] has large $\eta(x)$, which achieves stronger V_D regulation than the device with a small D [300 nm, Fig. 5(d)]. The strong V_D regulation on potential $\phi(x)$ indicates the device with large D will hardly saturate as V_D increases, as confirmed by Fig. 5(b) (red). It then explains the unsaturated SITs in previous works and suggests that better saturation in output curves can be achieved by minimizing the V_D regulation of $\phi(x)$, e.g., by reducing D.

As we have discussed the potential distribution, in the following we study the current-voltage characteristics and then validate the model by numerical simulation to understand the threshold voltages, subthreshold swing, gate-tuning in transfer scanning, and saturation behaviors in output scanning. Then, we further investigate the impacts of the structural parameters, aiming to provide guidance for device design.

IV. SUBTHRESHOLD CURRENT-VOLTAGE CHARACTERISTICS

Ideal subthreshold I-V characteristics should have near-zero V_{th}, sharp subthreshold swing, and large on:off ratio. Taking a p-type SIT as an example, the semiconductor-dielectric interfacial potential $\phi(x)$ lowers when V_G scans toward the negative. When the potential $\phi(x)$ in the middle is lower than source potential, i.e., $\phi(x = D/2) \le \phi_{BI}$, drift current begins to generate in the middle, and the corresponding V_G is taken as V_{th} for simplicity. By using $\phi(x = D/2) = \phi_{BI}$ (built-in potential) in Eq. (8), V_{th} is expressed as [50]

$$V_{th} = -\frac{\eta[x = (D/2)]}{1 - \eta[x = (D/2)]}\left(\frac{d_1}{d_1 + d_2}\right) V_D + \phi_{BI}. \quad (9)$$

Here, $\eta(x = D/2)$ [defined after Eq. (7)] increases from 0 to approach 1 if D increases. Therefore, if D or $|V_D|$ increases (or $d_1 + d_2$ decreases), V_{th} shifts toward the opposite direction of the on-state to reach a large $|V_{th}|$, as verified in Fig. 6. If $D \gg L_D$, the potential in the middle $\phi(x = D/2)$ approaches ϕ_∞ [Eqs. (5) and (8)], which is always more negative than ϕ_{BI} for p-type transistors [Eq. (6)] or more positive than ϕ_{BI} for n-type transistors. Thus, the transistor cannot be totally turned off, but will have a small on:off ratio because of the drift current, as verified in Supplementary Material Fig. S8 [50].

Subthreshold swing or the reversed subthreshold slope SS symbolizes the switching speed of transistors. Unlike

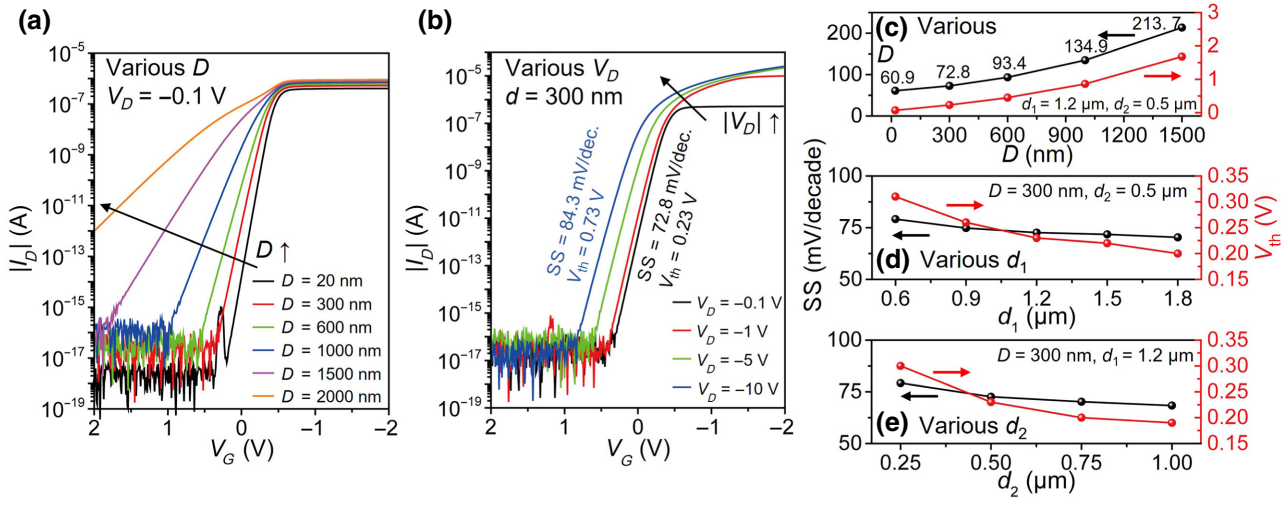

FIG. 6 Subthreshold swing and threshold voltage. (a),(b) Transfer curves in the subthreshold region for SITs with various D (a) or under different V_D (b). (c)–(e) Subthreshold swing SS and threshold voltage V_{th} for SIT changing with the structural parameters, such as D (c), d_1 (d), and d_2 (e). The SS and V_{th} are extracted when transfer scanning at $V_D = -0.1$ V.

the case of planar FETs, the SS value in SITs may be affected by the subthreshold current in the middle of the pores. The SS in a SIT is also deduced from $\phi(x = D/2)$ [50,57],

$$\mathrm{SS} = \frac{\partial V_G}{\partial \phi}\frac{kT}{q}\ln 10 \approx \frac{1}{1-\eta[x=(D/2)]}\frac{kT}{q}\ln 10. \quad (10)$$

When the pore diameter D is close to 0, SS approaches the thermodynamic limit of 59.6 mV/dec at room temperature ($T = 300$ K). As D increases, $\eta(x = D/2)$ also increases and thus the device exhibits large SS [Fig. 6(a) and 6(c)]. According to simulation results, SIT devices with pore diameters D of 300–500 nm can achieve similar SS values as bulk MOSFETs between around 60 and 90 mV/dec [57]. Other parameters, such as V_D, d_1, and d_2, slightly affect the SS through L_D, i.e., SS would slightly increase with larger V_D or thinner d_1 or d_2 [Figs. 6(b), 6(d), and 6(e)].

V. ABOVE-THRESHOLD CURRENT-VOLTAGE CHARACTERISTICS

Above V_{th}, the on-state current is determined by the partially gated channel transistor and R_{middle} in the equivalent circuit [Fig. 2(h)]. For R_1 and R_2 in the partially gated transistor, the possible conduction mechanisms include Ohmic conduction, space-charge-limited current (SCLC), Ohmic-to-SCLC transition, and trap-fill-limited SCLC, all of which can be uniformly described by $J = Q_0\mu(\Delta V^{\alpha}/d^{\beta})$ [58]. Here, Q_0 is the charge-density factor related to carrier concentration, μ is carrier mobility, d is transit length, and ΔV is the potential drop. The charge-transport coupling factor α represents the conduction types, such as Ohmic conduction ($\alpha = 1$) and Mott-Gurney law in SCLC conduction ($\alpha = 2$), with the parameter $\beta \cong 2\alpha - 1$ for the on-state device [40]. Therefore, in a partially gated transistor with two nongated channels gapping a gated channel, the current is

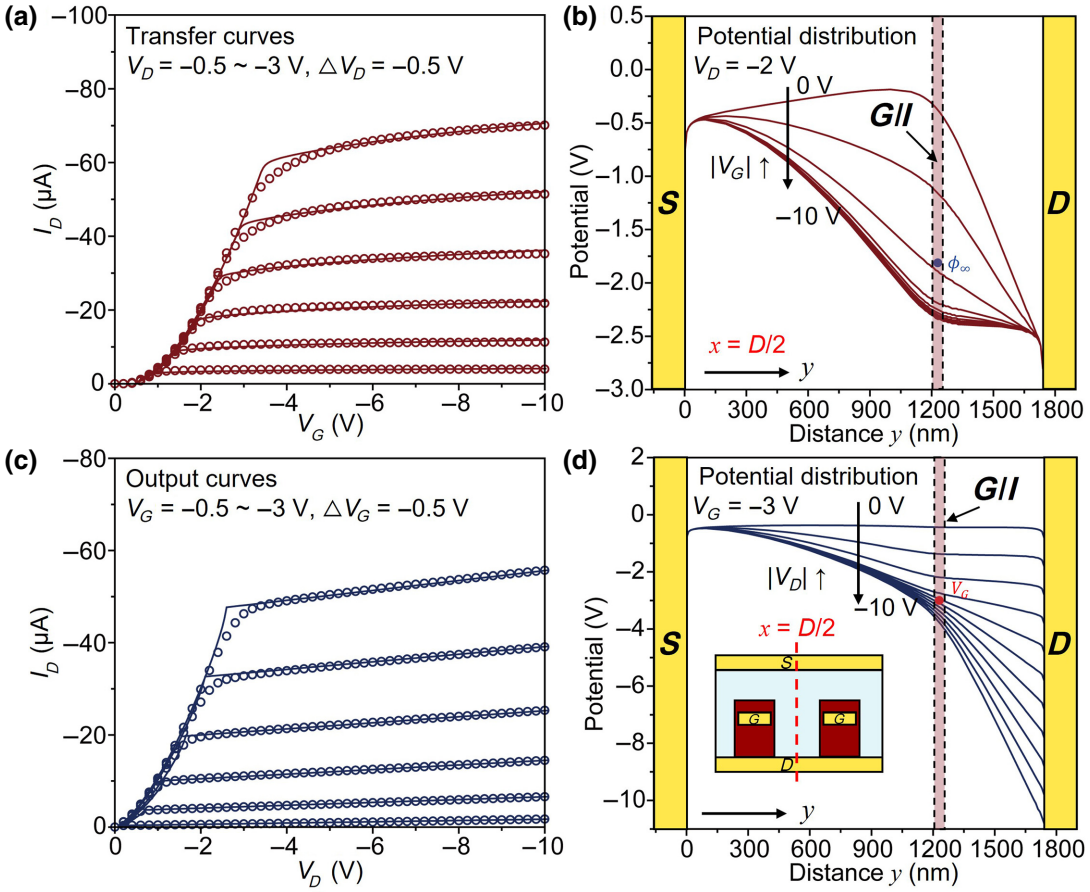

FIG. 7 Transfer and output characteristics. (a),(c) Transfer or output curves of SIT with $V_D = -0.5$ to -3 V, $\Delta V_D = -0.5$ V, or $V_G = -0.5$ to -3 V, $\Delta V_G = -0.5$ V, respectively. The dots are TCAD-simulated and curves are fitted by the proposed current model. (b),(d) Potential distribution at the middle of the pore channel during transfer scanning with $V_G = 0$ to -10 V, $\Delta V_G = -0.5$ V, and $V_D = -2$ V, or output scanning with $V_D = 0$ to -10 V, $\Delta V_D = -0.5$ V, and $V_G = -3$ V. The dashed red line in the inset of (d) shows the routine of potential extracted in (b),(d).

$$|I_{D,\text{side}}| = Q_{01}S_1\mu\frac{|V_1 - V_S|^\alpha}{d_1^\beta} = \frac{W}{L_{\text{gate}}}\mu C_{\text{ox}}\left|V_G - V_{\text{th}} - \frac{V_2 + V_1}{2}\right||V_2 - V_1| = Q_{02}S_2\mu\frac{|V_D - V_2|^\alpha}{d_2^\beta}. \quad (11)$$

Here, V_1 and V_2 are potentials at the beginning (near the source) and the end (near the drain) of the gated channel, W is the channel width, C_{ox} is the capacitance per unit area for the gate insulator, L_{gate} is the gate thickness, and Q_{0n}, S_n, d_n are the charge-density factor, electrode area, and length at the corresponding channel, respectively. As $|V_D|$ increases to reach the saturated regime ($|V_D| \geq |V_G - -V_{\text{th}}|$), the gated channel is pinched off and $V_2 = V_{\text{D,sat}} = V_G - V_{\text{th}}$. With the solution of V_1 and V_2 [50], the current of the partially gated transistor $|I_{D,\text{side}}|$ can be obtained and then the total current of the SIT is calculated by using Q_{0n}, α, and R_{middle} as fitting parameters,

$$I_{D,\text{tot}} = I_{D,\text{side}} + I_{D,\text{mid}} = I_{D,\text{side}} + V_D/R_{\text{middle}}. \quad (12)$$

The calculation of Eqs. (11) and (12) for SITs is simplified and presented in a HTML format with a user interface in the Supplementary Material [50], which could be used to calculate transfer and output characteristics.

The simulated transfer curves of the SIT shown in Fig. 7(a) (dots) are well fitted by the proposed model using Eqs. (12) and (13) (curves), with $\alpha = 1.5$. This indicates that the nongated semiconductor in the SIT exhibits Ohmic-to-SCLC transition in this device [59]. The fitting parameters are summarized in Supplementary Material Table S2 [50]. Unlike the case of common FETs, the transfer curves of SITs gradually saturate at large $|V_G|$ increases, which is caused by the large resistance near the source. As shown in Fig. 7(b), the potential drop is mainly between the source and the gate. This is similar to planar FETs with large contact resistance. In terms of output characteristics, common FETs achieve current saturation when $|V_D| \geq |V_G - V_{\text{th}}|$. Similarly, in a SIT, when $|V_D|$ increases to have the channel pinch-off with $V_2 = V_{D,\text{sat}} = V_G - V_{\text{th}}$, where V_2 is the potential at the end (near the drain) of the gated channel, the channel resistance rapidly increases. However, perfect saturation is not observed because the potential at the pore center $\phi(x = D/2)$ slightly changes with V_D [Fig. 7(d)], as derived from Eq. (8),

$$\frac{\partial\phi(x = D/2)}{\partial V_D} \approx \frac{d_1}{d_1 + d_2}\left[1 - \exp\left(-\frac{D}{2L_D}\right)^\gamma\right]^2 \geq 0. \quad (13)$$

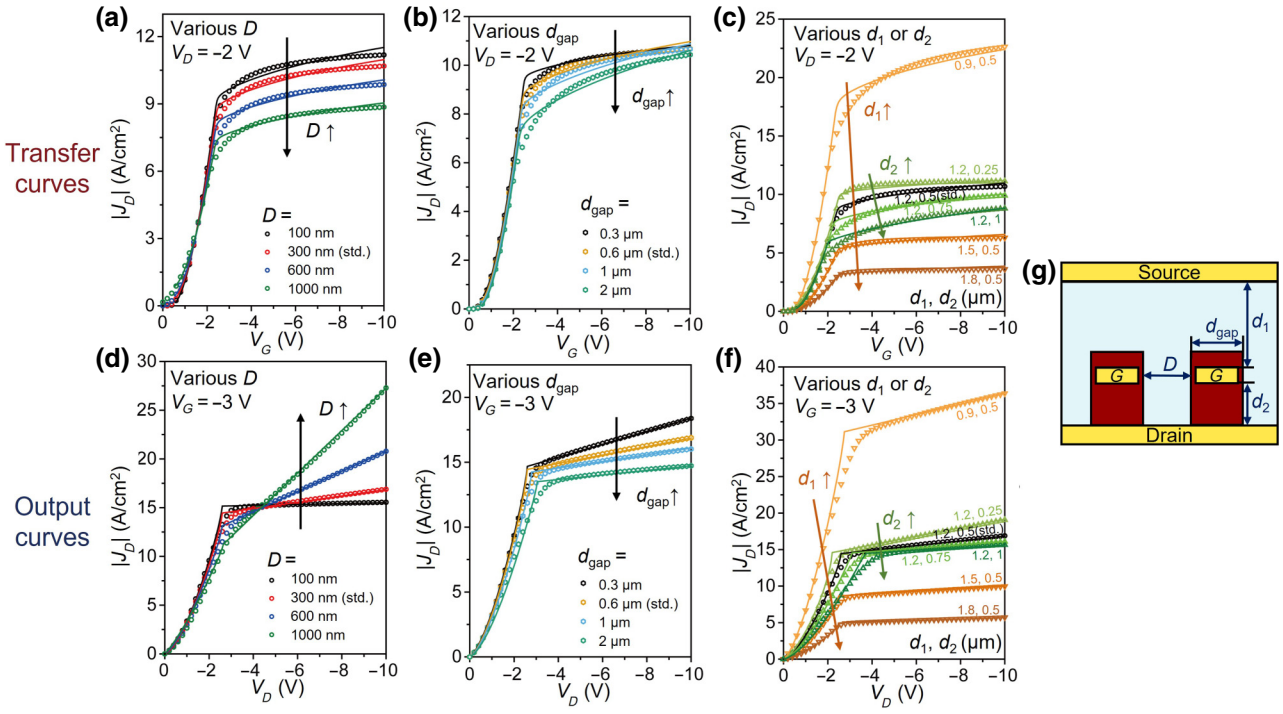

FIG. 8 Transfer and output curves with various structural parameters. (a)–(c) Transfer curves of SITs with different D, d_{gap}, d_1, or d_2 at $V_G = -2$ V. (d)–(f) Output curves of SITs with different D, d_{gap}, d_1, or d_2 at $V_G = -3$ V. The current density $|J_D|$ is used as Y axis to exclude the influence of device size. J_D is defined as $J_D = I_D/[W(D + d_{\text{gap}})]$, where W is the device width in the simulation. Simulated data and fitting results are plotted in symbols and lines, respectively. Reference curve with $D = 0.3$, $d_1 = 1.2$, $d_2 = 0.5$, and $d_{\text{gap}} = 0.6$ μm is marked by "(std.)" in the legends. (g) Parameters D, d_{gap}, d_1, and d_2 are illustrated.

The $\partial\phi/\partial V_D$ in Eq. (13) gives hints to why perfect saturation has rarely been achieved in the reported SIT experiments [39], and suggests the output saturation may be improved by minimizing $\partial\phi/\partial V_D$, e.g., reducing D and d_1. Because most charges transport through the middle of the pores, the current is dominated by R_{middle}. By using Eqs. (11) and (12) and extracting $R_{\text{middle}} = \partial V_D/\partial I_D$ in the saturation regime, the overall output characteristics determined by numerical simulation [Fig. 7(c), dots] can be well fitted by Eqs. (11) and (12) [Fig. 7(c), lines].

To investigate the impacts of structural parameters, transfer and output curves of SITs with various structural parameters are simulated, as shown in Fig. 8. All these curves are well fitted by the proposed current model (curves) and the impacts of parameters are discussed:

(i) With a small pore diameter D, the $\eta(x = D/2)$ [defined after Eq. (7)] in Eqs. (10) and (11) approaches 0 and, thus, transistors achieve near-zero V_{th}, large on:off ratio, small *SS*, and good output saturation [Fig. 8(d)]. Considering that the pore diameter is limited by the fabrication, the D around 300 nm is small enough.

(ii) With thick d_1 and d_2, the hole concentration in pores decreases, and thereby the Debye length L_D increases and $\eta(x = D/2)$ in Eqs. (10) and (11) approaches 0. Thus, SITs with thick d_1 and d_2 have near-zero V_{th}, small *SS*, and better output saturation [Figs. 6(d), 6(e) and 8(f)], but reduced I_D. For balance, the thickness of semiconductors in practical transistors should reach hundreds of nanometers [11] and the ratio d_1/d_2 should be smaller than 4.

(iii) The wider distance between pores, d_{gap}, leads to stronger gate controllability and better saturation in output curves [Fig. 8(e)], but the lower ratio of pore channels could result in reduced current density. Therefore, the size of d_{gap} should be of the same order of magnitude as pore diameter D.

(iv) The thinner thickness of sidewall dielectric, t_{ox}, results in better saturation in output curves (Supplementary Material Fig. S9 [50]). In practical devices, the sidewall and upper Al_2O_3 dielectric layers are oxidized from Al gate electrodes and the quality of the dielectric layers should be good enough to prevent the leakage current.

Note that permeable base transistors are similar to SITs with the pore diameter D as small as sub-100 nm and, therefore, these results are also generally applicable for permeable base transistors.

VI. CONCLUSION

The device physics theory for the vertical SIT is developed and concise potential distribution and *I-V* relations are derived. The dielectric layers should surround the porous electrodes in the ideal SIT, which is similar to a GAA device. An ideal SIT is approximately equivalent to a partially gated transistor and resistance connected in parallel. The expressions of the potential inside the pore channel $\phi(x)$ and the direct-current characteristics are derived, which connect the *I-V* characteristics and device structural parameters. In the subthreshold region, the ideal turn-on properties can be obtained in a SIT with a small pore diameter D around 300–500 nm, because of the strong gate regulation in potential distribution. During V_G scanning, the current is limited by the large resistance near the source and causes the transfer saturation. In output curves, pore channel resistance dominates the carrier transport when the partially gated transistor is saturated. The quantitative relation between current saturation and device parameters are revealed. Finally, the impacts of device structure on *I-V* characteristic are analyzed, which provide complete guidance for future study and fabrication of SIT devices.

ACKNOWLEDGMENTS

The authors gratefully acknowledge the financial support of the project from the National Natural Science Foundation of China (Grants No. 62004227 and No. 61922090).

[1] E. Fortunato, P. Barquinha, and R. Martins, Oxide semiconductor thin-film transistors: A review of recent advances, Adv. Mater. **24**, 2945 (2012).
[2] P. Lin and F. Yan, Organic thin-film transistors for chemical and biological sensing, Adv. Mater. **24**, 34 (2012).
[3] X. Yu, T. J. Marks, and A. Facchetti, Metal oxides for optoelectronic applications, Nat. Mater. **15**, 383 (2016).
[4] J. Sheng, T. Hong, H.-M. Lee, K. Kim, M. Sasase, J. Kim, H. Hosono, and J.-S. Park, Amorphous IGZO TFT with high mobility of ~70 cm2/(V s) via vertical dimension control using PEALD, ACS Appl. Mater. Interfaces **11**, 40300 (2019).
[5] J. Yeon Kwon and J. Kyeong Jeong, Recent progress in high performance and reliable n-type transition metal oxide-based thin film transistors, Semicond. Sci. Technol. **30**, 024002 (2015).
[6] J. W. Borchert, U. Zschieschang, F. Letzkus, M. Giorgio, R. T. Weitz, M. Caironi, J. N. Burghartz, S. Ludwigs, and H. Klauk, Flexible low-voltage high-frequency organic thin-film transistors, Science Advances **6**, eaaz5156 (2020).
[7] S. Jeon, A. Benayad, S.-E. Ahn, S. Park, I. Song, C. Kim, and U. I. Chung, Short channel device performance of amorphous InGaZnO thin film transistor, Appl. Phys. Lett. **99**, 082104 (2011).
[8] T. Hirose, T. Nagase, T. Kobayashi, R. Ueda, A. Otomo, and H. Naito, Device characteristics of short-channel polymer field-effect transistors, Appl. Phys. Lett. **97**, 083301 (2010).
[9] Y.-H. Lin, Y.-F. Chang, H.-F. Meng, H.-W. Zan, W. Hsu, and C.-H. Chen, Soldering of solution-processed organic vertical transistor and light-emitting diode on separate glass substrates by tin micro-balls, Org. Electron. **14**, 3052 (2013).

[10] X. Fang, C.-H. Lin, Y.-T. Sun, H.-T. Chin, H.-W. Zan, H.-F. Meng, S.-F. Horng, and L. A. Wang, A solvent-free lift-off method for realizing vertical organic transistors with low leakage current and high ON/OFF ratio, Org. Electron. **31**, 227 (2016).

[11] C.-H. Li, F. Stehlin, K.-R. Wang, Y.-H. Lin, F. Wieder, O. Soppera, H.-W. Zan, and H.-F. Meng, Achieving saturation in vertical organic transistors for organic light-emitting diode driving by nanorod channel geometric control, Appl. Phys. Lett. **102**, 163305 (2013).

[12] A. J. Ben-Sasson, Z. Chen, A. Facchetti, and N. Tessler, Solution-processed ambipolar vertical organic field effect transistor, Appl. Phys. Lett. **100**, 263306 (2012).

[13] M. Uno, Y. Tominari, and J. Takeya, Three-dimensional organic field-effect transistors: Charge accumulation in the vertical semiconductor channels, Appl. Phys. Lett. **93**, 173301 (2008).

[14] H.-I. Yeom, G. Moon, Y. Nam, J.-B. Ko, S.-H. Lee, J. Choe, J. H. Choi, C.-S. Hwang, and S.-H. K. Park, 60-3: Distinguished paper: Oxide vertical TFTs for the application to the ultra high resolution display, SID Symposium Digest of Technical Papers **47**, 820 (2016).

[15] T. L. Phan, Q. A. Vu, Y. R. Kim, Y. S. Shin, I. M. Lee, M. D. Tran, J. Jiang, D. H. Luong, L. Liao, Y. H. Lee, and W. J. Yu, Efficient gate modulation in a screening-engineered MoS2/single-walled carbon nanotube network heterojunction vertical field-effect transistor, ACS Appl. Mater. Interfaces **11**, 25516 (2019).

[16] J. Zhou, L. Xie, X. Song, Z. Wang, C. Huo, Y. Xiong, Z. Cheng, Y. Wang, S. Zhang, X. Chen, and H. Zeng, High-performance vertical field-effect transistors based on all-inorganic perovskite microplatelets, J. Mater. Chem. C **8**, 12632 (2020).

[17] J.-i. Nishizawa, T. Terasaki, and J. Shibata, Field-effect transistor versus analog transistor (static induction transistor), IEEE Trans. Electron Devices **22**, 185 (1975).

[18] Y.-C. Chao, M.-C. Ku, W.-W. Tsai, H.-W. Zan, H.-F. Meng, H.-K. Tsai, and S.-F. Horng, Polymer space-charge-limited transistor as a solid-state vacuum tube triode, Appl. Phys. Lett. **97**, 223307 (2010).

[19] H.-W. Zan, Y.-H. Hsu, H.-F. Meng, C.-H. Huang, Y.-T. Tao, and W.-W. Tsai, High output current in vertical polymer space-charge-limited transistor induced by self-assembled monolayer, Appl. Phys. Lett. **101**, 093307 (2012).

[20] R. Siergiej, R. Clarke, A. Aganval, C. Brandt, A. Burk, A. Morse, and P. Orphanos, in *Proceedings of International Electron Devices Meeting* (IEEE, 1995), p. 353.

[21] P. Campbell, W. Garwacki, A. Sears, P. Menditto, and B. Baliga, Trapezoidal-groove Schottky-gate vertical-channel GaAs FET (GaAs static induction transistor), IEEE Electron Device Lett. **6**, 304 (1985).

[22] M. Hartensveld, C. Liu, and J. Zhang, Proposal and realization of vertical GaN nanowire static induction transistor, IEEE Electron Device Lett. **40**, 259 (2018).

[23] W. Li, D. Ji, R. Tanaka, S. Mandal, M. Laurent, and S. Chowdhury, Demonstration of GaN static induction transistor (SIT) using self-aligned process, IEEE Journal of the Electron Devices Society **5**, 485 (2017).

[24] S.-y. Fujimoto, K.-i. Nakayama, and M. Yokoyama, Fabrication of a vertical-type organic transistor with a planar metal base, Appl. Phys. Lett. **87**, 133503 (2005).

[25] M. P. Klinger, A. Fischer, F. Kaschura, J. Widmer, B. Kheradmand-Boroujeni, F. Ellinger, and K. Leo, Organic power electronics: Transistor operation in the kA/cm2 regime, Sci. Rep. **7**, 44713 (2017).

[26] K. Kudo, M. Iizuka, S. Kuniyoshi, and K. Tanaka, Device characteristics of lateral and vertical type organic field effect transistors, Thin Solid Films **393**, 362 (2001).

[27] B. Kheradmand-Boroujeni, M. P. Klinger, A. Fischer, H. Kleemann, K. Leo, and F. Ellinger, A pulse-biasing small-signal measurement technique enabling 40 MHz operation of vertical organic transistors, Sci. Rep. **8**, 7643 (2018).

[28] M. Sarjidan, Prospect of silver nanowire (AgNW) in development of simple and cost-effective vertical organic light-emitting transistors, Appl. Phys. A **125**, 1 (2019).

[29] B. Liu, M. A. McCarthy, Y. Yoon, D. Y. Kim, Z. Wu, F. So, P. H. Holloway, J. R. Reynolds, J. Guo, and A. G. Rinzler, Carbon-nanotube-enabled vertical field effect and light-emitting transistors, Adv. Mater. **20**, 3605 (2008).

[30] Y. Watanabe, H. Iechi, and K. Kudo, Electrical characteristics of flexible organic static induction transistors under bending conditions, Appl. Phys. Lett. **89**, 233509 (2006).

[31] G. Feng, J. Jiang, Y. Zhao, S. Wang, B. Liu, K. Yin, D. Niu, X. Li, Y. Chen, and H. Duan, A sub-10 nm vertical organic/inorganic hybrid transistor for pain-perceptual and sensitization-regulated nociceptor emulation, Adv. Mater. **32**, 1906171 (2020).

[32] E. Guo, S. Xing, F. Dollinger, Z. Wu, A. Tahn, M. Löffler, K. Leo, and H. Kleemann, High-performance static induction transistors based on small-molecule organic semiconductors, Advanced Materials Technologies **5**, 2000361 (2020).

[33] H. Yu, Z. Dong, Jing Guo, D. Kim, and F. So, Vertical organic field-effect transistors for integrated optoelectronic applications, ACS Appl. Mater. Interfaces **8**, 10430 (2016).

[34] W.-L. Chen, H.-C. Chiu, H. Chu, J.-C. Hsieh, B.-X. Chen, Y.-C. Tian, S.-K. Liau, M.-J. Chan, C.-J. Lu, and H.-F. Meng, Electronic nano sponge breath ammonia sensors using hygroscopic polymers on vertical channel nanoporous structure, J. Mater. Chem. C **9**, 12938 (2021).

[35] W.-L. Chang, C.-C. Chang, Y.-T. Lee, A. D. T. Thi, C.-C. Chen, H.-F. Meng, H.-W. Zan, C.-J. Lu, M. He, and Y. Li, Gas emission from human skin positions detected by vertical-channel organic semiconductor sensor, Sens. Actuators, B **343**, 129994 (2021).

[36] E. Guo, S. Xing, F. Dollinger, R. Hübner, S.-J. Wang, Z. Wu, K. Leo, and H. Kleemann, Integrated complementary inverters and ring oscillators based on vertical-channel dual-base organic thin-film transistors, Nature Electronics **4**, 588 (2021).

[37] Z. Wu, Y. Liu, E. Guo, G. Darbandy, S.-J. Wang, R. Hübner, A. Kloes, H. Kleemann, and K. Leo, Efficient and low-voltage vertical organic permeable base light-emitting transistors, Nat. Mater. **20**, 1007 (2021).

[38] S.-J. Wang, M. Sawatzki, G. Darbandy, F. Talnack, J. Vahland, M. Malfois, A. Kloes, S. Mannsfeld, H. Kleemann, and K. Leo, Organic bipolar transistors, Nature **606**, 700 (2022).

[39] H. Kleemann, K. Krechan, A. Fischer, and K. Leo, A review of vertical organic transistors, Adv. Funct. Mater. **30**, 1907113 (2020).

[40] F. Kaschura, A. Fischer, M. P. Klinger, D. H. Doan, T. Koprucki, A. Glitzky, D. Kasemann, J. Widmer, and K. Leo, Operation mechanism of high performance organic permeable base transistors with an insulated and perforated base electrode, J. Appl. Phys. **120**, 094501 (2016).

[41] G. Darbandy, F. Dollinger, P. Formánek, R. Hübner, S. Resch, C. Roemer, A. Fischer, K. Leo, A. Kloes, and H. Kleemann, Unraveling structure and device operation of organic permeable base transistors, Advanced Electronic Materials **6**, 2000230 (2020).

[42] Y. Zhang, S. Yang, Y. Jiang, and B. Zou, Influence of contact resistance on the electrical characteristics of organic static induction transistors, Semicond. Sci. Technol. **34**, 095022 (2019).

[43] A. K. Baliga, B. Kumar, and Srishti, in *International Conference on Emerging Trends in Communication Technologies* (2016), p. 1.

[44] J. Liu, Z. Qin, H. Gao, H. Dong, J. Zhu, and W. Hu, Vertical organic field-effect transistors, Adv. Mater. **29**, 1808453 (2019).

[45] M. Greenman, G. Sheleg, C.-m. Keum, J. Zucker, B. Lussem, and N. Tessler, Reaching saturation in patterned source vertical organic field effect transistors, J. Appl. Phys. **121**, 204503 (2017).

[46] F. M. Sawatzki, D. H. Doan, H. Kleemann, M. Liero, A. Glitzky, T. Koprucki, and K. Leo, Balance of Horizontal and Vertical Charge Transport in Organic Field-Effect Transistors, Physical Review Applied **10**, 034069 (2018).

[47] A. J. Ben-Sasson and N. Tessler, Patterned electrode vertical field effect transistor: Theory and experiment, J. Appl. Phys. **110**, 044501 (2011).

[48] C. Liu, Z. Chen, K. Huang, S. Hu, X. Liang, and J. Chen, Vertical Transistors with Conductive-Network Electrodes: A Physical Image and What It Tells, Physical Review Applied **13**, 054066 (2020).

[49] H.-C. Lin, H.-W. Zan, Y.-C. Chao, M.-Y. Chang, and H.-F. Meng, Review of a solution-processed vertical organic transistor as a solid-state vacuum tube, Semicond. Sci. Technol. **30**, 054003 (2015).

[50] Supplemental Material at http://link.aps.org/supplemental/10.1103/PhysRevApplied.19.034096 provides details of derivation of equations and simulations.

[51] D. A. Neamen and B. Pevzner, *Semiconductor Physics and Devices: Basic Principles* (McGraw-Hill, New York, NY, 2012).

[52] P. Mark and W. Helfrich, Space-charge-limited currents in organic crystals, J. Appl. Phys. **33**, 205 (1962).

[53] Y. Guerfi and G. Larrieu, Vertical silicon nanowire field effect transistors with nanoscale gate-all-around, Nanoscale Res. Lett. **11**, 210 (2016).

[54] G. Larrieu, Y. Guerfi, X. L. Han, and N. Clément, Sub-15 nm gate-all-around field effect transistors on vertical silicon nanowires, Solid-State Electron. **130**, 9 (2017).

[55] P.-Y. Chang, S.-F. Peng, Y.-C. Chao, H.-C. Lin, H.-W. Zan, and H.-F. Meng, Vertical organic transistors withstanding high voltage bias, Appl. Phys. Lett. **106**, 153301 (2015).

[56] H. Fan and K. Y. Sze, A micro-mechanics model for imperfect interface in dielectric materials, Mechanics of Materials **33**, 363 (2001).

[57] I. Ferain, C. A. Colinge, and J.-P. Colinge, Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors, Nature **479**, 310 (2011).

[58] C. Liu, X. Li, Y. Luo, Y. Wang, S. Hu, C. Liu, X. Liang, H. Zhou, J. Chen, J. She, and S. Deng, How materials and device factors determine the performance: A unified solution for transistors with nontrivial gates and transistor–diode hybrid integration, Advanced Science **9**, 2104896 (2022).

[59] P. Zhang, Á. Valfells, L. K. Ang, J. W. Luginsland, and Y. Y. Lau, 100 years of the physics of diodes, Applied Physics Reviews **4**, 011304 (2017).