Three-Terminal VO₂-Based Device with Internal Read-Write Switching

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Memristive devices based on correlated Mott materials have great potential for memory applications, and specifically neuromorphic computations, due to their simple structure, miniaturization capabilities, power efficiency, and operation speeds. For these reasons, many efforts are made to design improved synaptic devices based on Mott materials. This work demonstrates a nonvolatile memristive three-terminal transistor based on the correlated oxide VO₂, which has a (Mott) metal-insulator transition near room temperature. An ultrathin VO₂ layer is incorporated in a metal-oxide-semiconductor field-effect geometry using alumina as the gate dielectric. A field effect is demonstrated to modify the channel's resistance in a nonvolatile and reversible fashion. However, only when the gate voltage is applied at the metallic state of the VO₂ does the resistance of the insulating state change. Thus, the metallic and insulating states, reached via heating and cooling, act as a write-read switch. Field-induced oxygen motion is the probable mechanism, and a model based on oxygen motion at the VO₂/Al₂O₃ interface reproduces the observed results well. This study provides a proof of principle for the development of high-performance electronic synaptic transistors utilizing Mott materials, where the fully solid-state composition simplifies fabrication and enables integration with silicon-based architectures for future applications.

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I. INTRODUCTION

The increasing interest in machine-learning and artificial-intelligence computations has been driving the search for efficient device architecture and materials that can enable operational realization of neuronlike functionalities and algorithms in electronic devices [1–3]. A major ingredient in these applications is the synaptic element, which should be able to continuously and bidirectionally change its resistance when stimuli are applied. Leading candidates to realize this portion include phase-change materials (PCMs) [4–6], resistive-switching (RS) oxides [7–9], and Mott materials with insulator-to-metal transitions (IMTs) [10–12].

Recently, ionic liquid gating was shown to enable the reversible motion of ions in IMT materials and a corresponding large change in the resistance. This introduces an additional third terminal gate, relative to the two-terminal PCM and RS systems, adding more control to the state of the system. Here, only when a gate is applied does the state of the system change and in a nonvolatile manner [13]. Ionic motion of oxygen ions [14–16], hydrogen [17,18], and others [19] are demonstrated by ionic liquid gating. In general, the large electric field at the interface is sufficient

to move the oxygen (or other) ions from an adjacent reservoir into the film and vice versa. This, in turn, can lead to large changes in the transport properties [20,21] and even other properties, such as magnetization [22,23].

A major drawback, however, is that fabrication and individually addressing multiple submicron-scale elements based on liquid-ion gating is complex. In addition, integration of such elements with standard complementary metal oxide semiconductor (CMOS) technologies does not lend itself easily. Solid-state gating may circumvent these problems, but usually the fields attained with such gating are not sufficient to induce ionic motion in the IMT materials. Recently, it was demonstrated that hydrogen ionic motion could be attained via gating a hydrogenated silica gate atop the IMT VO₂ in a reversible and controlled fashion [24]. Herein, we demonstrate it is possible to attain resistance changes with solid-state gating in VO₂, most likely due to oxygen motion, with additional functionalities, as discussed below.

 VO_2 is a transition-metal oxide in which a temperaturedriven IMT is accompanied by a structural phase transition. The transition temperature in the bulk is 342 K, i.e., above but close to room temperature. It is shown that the transition can be driven at ultrafast speeds [25–27]. We present a proof of concept for a three-terminal fieldeffect geometry device with an "internal" read-write switch and nonvolatile memory, based on a VO₂ active channel. Applying a gate voltage at low temperatures (below the

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phase transition) has virtually no effect on the low-Tsource-drain resistance (R_{SD}) . Applying the same gate voltage at high temperatures, above the IMT, does not change the channel resistance at high temperatures (of the metallic state). But, after cooling, one can find that it considerably alters the low-T resistance, in a nonvolatile way. The new R_{SD} is stable for many temperature cycles. But, it can be reversed by applying a gate voltage with opposite polarity at elevated temperatures. Thus, this three-terminal transistor shows nonvolatile behavior for the gate effect and has separate "read" and "write" states controlled by the corresponding VO₂ insulating and metallic phases [see Fig. 1(a) for a pictorial representation]. In addition, the resistance change is continuous, bidirectional, and nonlinear. We present device characteristics and suggest a model based on oxygen motion to explain the measured device behavior.

II. EXPERIMENTAL SECTION

A. Device fabrication

Our device is composed of a thinned (using wet etching) about 13-nm VO₂ channel that is 100 μ m wide; further details regarding the deposition, patterning, and thinning are available in Refs. [28,29]. On top of the VO₂ channel,

we sputter-deposit 50-nm vanadium contacts for source (*S*) and drain (*D*) electrodes. Then, we use atomic layer deposition (ALD) to deposit a 25-nm Al_2O_3 layer on the entire chip as the gate dielectric. Finally, we deposit a 50-nm platinum gate electrode, marked *G*, atop the dielectric and between the *S* and *D* contacts. The channel length is 100 µm.

B. Transport measurements

During all field effect transistor measurements, we verify that the S-D voltage is much smaller than V_G , $V_{SD} V_G$, so the gate voltage is symmetric along the channel. Additionally, we continuously monitor and measure the leakage current, I_{GD} , verifying that there is no gate leakage (maximum measured 0.15 nA) or dielectric breakdown during the measurements. Our measurement system consists of two Keithley 2400 instruments as voltage sources, while measuring the current. In typical measurements, $V_{SD} \sim 100$ mV, while V_{GD} is varied between -8 and 8 V.

III. RESULTS

Figures 1(b) and 1(c) shows the device scheme and a TEM cross section of the layer stack. The active channel is an about 13-nm VO₂ thin film, covered by a 20-nm Al_2O_3



FIG. 1. Realization of monolithic memory device. (a) Concept illustration of the three-terminal devices. (b) Realization of a threeterminal unit based on a thin film of VO₂ as a channel, 20-nm Al₂O₃ as a gate dielectric, and a heat reservoir as a read-write switch. (c) TEM image of the device cross section showing the order of the layers (colored lines marked to distinguish between layers). (d)–(f) Measured source-drain resistance, gate-voltage pulses, and the temperature versus measurement time, respectively. After applying V_G at low temperature (high-resistance state), R_{SD} temperature dependence does not change (sections I and II, black and red curves in (d). However, after applying a positive V_G at high temperatures, there is a drop of ΔR in the low- $T R_{SD}$ (section III, green). This low R_{SD} remains constant until a negative V_G is applied, causing an increase, ΔR , in the low- $T R_{SD}$ (section IV and blue curve). (g) R versus Tmeasurement of data in (d),(f). Color coding corresponds to the four sections of the protocol, as in (d).

gate dielectric, capped by a V/Pt gate electrode. Thin VO₂ is attained by wet-etch thinning of a 60-nm film, which maintains a large IMT resistance change, even for this thin film [28]. Source and drain electrodes of the same composition as the gate electrode are connected to the channel; the width and length are 80 and 100 µm, respectively. The operation of the device is exemplified in Figs. 1(d)-1(g). The temperature (T) is cycled between 300 and 360 K, and the R_{SD} of the channel is measured continuously. Due to the IMT, R_{SD} decreases upon heating from about 1 M Ω at 300 K to about 900 Ω at 360 K. We show that, after applying a V_G of 7 V at temperatures below the IMT, the low- $T R_{SD}$ does not change, as previously reported for VO₂-based field-effect measurements [30]. However, after a positive gate voltage (7 V) is applied at T = 360 K, i.e., while VO_2 is in the metallic phase, the following low-T R_{SD} decreases by a significant magnitude, marked as ΔR in Fig. 1(d) [the corresponding full R_{SD} versus T curves are shown in Fig. 1(g)], and remains unchanged for at least three days without the presence of any gate voltage (not shown). Reverting the effect, i.e., increasing the low- TR_{SD} , is achieved by applying a negative gate voltage at high T, as shown for a gate voltage of -8 V applied at 360 K, and results in an increase in resistance marked by ΔR in the image.

In Fig. 2, we show the main properties of devices with the same geometry as that described above. For clarity of the analysis, the following conventions are used. The low-T resistance is always acquired at 305 K. The initial device resistance, denoted by R_i , is measured before applying gate voltages. We measure how much the low-T resistance changes after applying the gate, $\Delta R = R - R_i$, where R is measured after applying V_G . In the measurements shown in Figs. 2(b) and 2(c), we start at a low-resistance state of the channel, and therefore, ΔR is positive. In Figs. 2(d) and 2(e), we start at a high-resistance state of the channel, resulting in a negative ΔR . Figure 2(a) shows the measurement protocol of applying different V_G and the subsequent change in R_{SD} . Figure 2(b) shows the change in resistance, ΔR , measured for different V_G applied at 364 K for 10 min. For negative V_G , between 0 and -5 V, there is almost no effect. For larger negative gate voltages, there is a considerable increase in ΔR . The change in resistance is only reversed when a voltage of opposite polarity (positive V_G)



FIG. 2. Device's main properties. (a) Measurement protocol for ΔR versus V_G . R_i is measured at 305 K; V_G is applied at 364 K for 10 min followed by the measurement of R at 305 K. (b) ΔR measurements of the protocol in (a). (c) ΔR versus run number of alternating voltage polarity (red squares indicate ΔR after setting $V_G = -7$ V, and blue squares indicate ΔR after setting $V_G = +7$ V). Inset, the change in resistance relative to the previous run. (d) ΔR versus the duration of gate voltage (+7 V applied at 364 K). (e) ΔR versus the temperature at which V_G is applied ($V_G = +7$ V). Inset, ΔR versus the metallic fraction, P, at each temperature that V_G is applied.

is applied, revealing hysteretic behavior. Here, the resistance starts to decrease at a smaller voltage of about 2.5 V. The maximum V_G that can be applied is limited by the dielectric breakdown of the device, around 9 V in our devices.

A sequence of applying alternating polarities of V_G (\pm 7 V) is shown in Fig. 2(c). For each successive run, an opposite V_G polarity is set at 365 K for 10 min followed by measurement of the low- $T R_{SD}$. The red squares are measurements after a negative V_G and blue are after a positive V_G . The change in resistance relative to the previous run, ΔR_P , is shown in the inset of Fig. 2(c). ΔR_P gradually decreases and seems to converge to a constant value. This indicates the effect is reversible and stable, and the amount of change in resistance also depends on the history of the device.

The effect of the duration of applying the gate voltage on the change in resistance is summarized in Fig. 2(d). Before each measurement, a voltage of -7 V is applied for 60 min at 364 K (bringing the channel to the high-resistance state) and is then cooled to measure the low-*T* resistance. The device is then reheated to 364 K and the gate is set to 7 V for a set time, followed by the low-*T* resistance measurement. It can be seen that the magnitude of ΔR gradually increases with gate duration, until about 50 min, at which point it saturates.

The change in resistance as a result of the temperature at which the gate is applied is measured in the following fashion. Starting with a device in the high-resistance state, the device is heated to the desired temperature. Then, V_G is set to 7 V for 10 min and then set to 0 V, resulting in a decrease in the device's low-T resistance. The device is then heated to 365 K before being cooled and the low-T resistance is measured. Figure 2(e) shows the dependence of ΔR on gate temperature; the line is a guide to the eye. A change in R_{SD} begins near the IMT (~338 K), grows with increasing temperatures, and saturates when the transition completes. The metallic fraction (P) is calculated, using the effective medium approximation [31], for each temperature at which V_G is applied. The plot of ΔR versus P is shown in the inset of Fig. 2(e). There is a significant change in resistance only if most of VO₂ in the device is in the metallic state.

IV. DISCUSSION

The most probable mechanism for the resistance changes reported here is electric-field-induced ion motion, which is temperature dependent. Electron trapping may also occur in the metal-oxide capacitor geometry. However, to date, there has been no experimental evidence that the field effect is sufficient to cause any considerable change in the source-drain resistance of the VO₂ channel. The most mobile ions available in the system are oxygen ions. Large changes in channel resistance due to oxygen

vacancies were previously reported for VO₂ when a liquid gate was applied [14,17–19]. Previous reports on low-T(at the insulating phase of VO₂) field effects using solid gate dielectrics did not result in any substantial resistance changes up to dielectric breakdown, similar to what we observe [30]. The effect of ionic hydrogen motion was recently reported to control the resistance in VO₂, using a hydrogenated silica gate [24], but there is no hydrogen reservoir in our device.

We observe that the nonvolatile gate-induced resistance change is highly temperature dependent, across the IMT. In the absence of any other option, the most probable mechanism is oxygen-ion motion, where the resistance of an oxygen-deficient layer decreases and the resistance of an oxygen-rich layer increases. We can envision several mechanisms that may increase the oxygen-ion mobility at elevated temperatures. Thermal activation must make some contribution; however, the strong correlation of the IMT to resistance changes indicates this is probably not the main contributing factor. It is possible that the structural transition changes the oxygen mobility, making it more susceptible to the electric field at the high-temperature tetragonal phase, possibly due to increased strain at the interface upon the structural transition. Recent reports showed changes in oxygen motion as a result of lattice strain in other oxides [32,33]. Finally, the large electron density of states at the high-temperature metallic phase can increase the electric field at the oxide-VO₂ interface, relative to the insulating phase. Here, due to the lower carrier density, the depletion (accumulation) region will be extended, altering the magnitude of the electric field at the interface layer.

Figure 3 illustrates the operation stages, starting from a fresh device at 300 K. By setting a positive V_G , the negatively charged oxygen in the interface, between VO₂ and Al₂O₃, is attracted toward Al₂O₃, leaving an oxygen-poor layer. In VO_x, the lower the oxidation state, the lower the resistivity. When the system is in the metallic state, the resistance of VO₂ is low, so R_{SD} is low, and therefore, not sensitive to the oxygen-poor channel. However, in the insulating phase, the total R_{SD} is significantly higher, and therefore, more sensitive to the new low-resistance layer parallel to the channel, as shown in Fig. 3(c). It is possible that oxygen penetrates into the Al₂O₃ layer, but ALD-deposited alumina should be oxygen saturated. This would lead to the oxidation of the upper VO₂ layer to V₂O₅.

The strong dependence of the effect on the conductivity of the channel (modified via the IMT) can be related to the magnitude of the electric field at the interface created by the gate voltage, as expressed above, recalling that the carrier density in VO₂ changes by over 3 orders of magnitude across the IMT [34]. Thus, the electric field at the oxide-VO₂ interface will also change, as conveyed above. Further investigation is required to verify that the mechanism is indeed oxygen motion and to resolve whether



FIG. 3. Illustration of writing mechanism. (a) VO₂ channel in its insulating high-resistance phase. (b) Application of a positive gate voltage at high temperatures (when VO₂ is metallic) and oxygen movement toward Al₂O₃, leaving an oxygen-poor layer. (c) Cooling the system below T_C , total R_{SD} is lowered due to a parallel connection of a conductive layer (which is the oxygen-depleted layer).

oxygen penetrates into Al₂O₃, accumulates at the interface, or accumulates at grain boundaries while leaving oxygen vacancies elsewhere.

We construct a heuristic model for the behavior of oxygen motion, following the effective circuit shown in Fig. 4(a). The VO₂ channel low-T resistance is composed of four parts, two variable resistors and two fixed resistors. The two variable resistors depict the layers of the channel under the gate where oxygen can move toward or away from the Al₂O₃ interface, changing the resistance of the layers: R_{poor} , the oxygen-poor layer with lower resistance; $R_{\rm rich}$, the oxygen-rich layer with higher resistance. The thicknesses of these layers change, at each other's expense, with oxygen movement. Thus, when a positive gate voltage is applied, the oxygen-poor layer (R_{poor}) grows at the expense of the oxygen-rich layer (R_{rich}) , and the total resistance decreases. The two fixed resistors are composed of VO_2 where no oxygen changes, and include (1) the edges of the channel not directly under the gate (R_S) , and (2) an additional layer under the gate that is not affected by oxygen movement (marked R_P). For simplicity, we assume that oxygen movement, or the thickness of the R_{poor} layer, changes linearly with time until a critical thickness, at which point it begins to change exponentially, so it will saturate at the fully-oxygen-rich or fully-oxygen-poor state in a physical manner (i.e., not abruptly). The equations used for the change in thickness of the R_{poor} layer over time are

increasing:
$$\frac{dm}{dt} = s_{up} \left(1 - H(m - nl_{up}) \frac{m - nl_{up}}{1 - nl_{up}} \right),$$

decreasing:
$$\frac{dm}{dt} = s_{down} \left(1 - H(nl_{down} - m) \frac{nl_{down} - m}{nl_{down}} \right).$$

Here, *m* is the fraction of the layer that is oxygen poor, i.e., m = 0 indicates the virgin state when all the layer is oxidized, and in general 1 - m is the fraction of the layer that is oxygen rich. S_{up} (S_{down}) indicates the speed at which the oxygen-poor layer is increasing (decreasing) when applying a positive (negative) gate voltage. *H* is the Heaviside function, and *nl* is the point where *m* starts to change nonlinearly. We assume that $nl_{\text{down}} = 1 - nl_{\text{up}}$, i.e., that the point of change from linear to nonlinear is the same, regardless of increasing or decreasing thickness. The resistance of the two layers is calculated by

$$R_{\text{poor}} = \frac{R_{\text{poor},0}}{m} , R_{\text{ox}} = \frac{R_{\text{rich},0}}{(1-m)},$$
$$R_{\text{total}} = R_s + (R_{\text{poor}}^{-1} + R_{\text{rich}}^{-1} + R_p^{-1})^{-1}$$

The total resistance of the device is calculated from the resistor model in Fig. 4(a). We optimize the fitting parameters, so they best reconstruct data of Fig. 2(b). The refined fitting parameters are $S_{up} = 0.053(1/s) \pm 2.6\%$, $S_{down} = 0.044(1/s) \pm 3\%$, $nl = 0.80 \pm 5\%$, $R_{poor,0} = 69.8 \text{ k}\Omega \pm 6\%$, $R_{rich,0} = 685.5 \text{ k}\Omega \pm 14\%$, $R_s = 18.9 \text{ k}\Omega \pm 21\%$, and $R_p = 50.7 \text{ k}\Omega \pm 9\%$. We show the resulting simulated change in resistance of the channel versus run number in Fig. 4(c). This model captures the changes in resistance



FIG. 4. Numerical simulation. (a) Model schematic of the VO₂ channel. (b) Simulated ΔR versus duration of gate voltage. (c) Simulated (black stars) ΔR versus run number of alternating voltage polarity (red and blue squares indicate measured ΔR).

over runs well. We can explain the decrease in resistance over a number of cycles from an asymmetry in the oxygenmotion speed, between removing and returning the oxygen ions to the VO₂ layer ($S_{up} > S_{down}$). Using the refined parameters above, we simulate the change in resistance with time [from Fig. 2(c)], as shown in Fig. 4(b). This is possible, since, in both measurements, the same gate voltage is applied. The simulation captures the behavior of the channel well, with no adjustment of fitting parameters. We note that this is a minimal model, so it does not account for the gate-voltage dependence or the temperature dependence of the resistance change. These effects are highly nonlinear, so an in-depth understanding of oxygen-motion mechanisms is needed to model their contributions, which is beyond the scope of our paper.

V. CONCLUSION

We present a solid-state three-terminal device with a VO_2 channel. The insulator (metal) phases of VO_2 act as an internal read-write switch, while the magnitude and duration of the gate voltage determine the nonvolatile change in R_{SD} . The physical mechanism is well explained by a model based on ion motion, and due to the construction of the device, it is most likely oxygen-ion motion. Thus, we demonstrate that the efficiency of oxygen motion in VO_2 can change considerably with the phase of the material. We propose a model where, in the metallic phase, there is a larger field at the interface of the device, relative to the insulating phase, resulting in oxygen motion for our solidstate gate, with no need for ion-liquid gating. However, we do not rule out that there may be other mechanisms leading to changes in oxygen-ion mobility across the IMT. We note that for some applications a long timescale of seconds or minutes might be fine, but for most computations the timescale should be much shorter. The timescale can be reduced by using larger gate voltages for ionic motion and using a high-intensity laser or local joule heating to shorten heating and cooling times [26,27].

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