Superconducting Resonators with Voltage-Controlled Frequency and Nonlinearity

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Voltage-tunable superconductor-semiconductor devices offer a unique platform to realize dynamic tunability in superconducting quantum circuits. By galvanically connecting a gated InAs-Al Josephson junction to a coplanar waveguide resonator, we demonstrate the use of a superconducting element with wideband gate tunability. We show that the resonant frequency is controlled via a gate-tunable Josephson inductance and that the nonlinearity of the InAs-Al junction is nondissipative as is the case with conventional AlO_x-Al junctions. As the gate voltage is decreased, the inductive participation of the junction increases up to 44%, resulting in the resonant frequency being tuned by over 2 GHz. Utilizing the wide tunability of the device, we demonstrate that two resonant modes can be adjusted such that they strongly hybridize, exhibiting an avoided-level crossing with a coupling strength of 51 MHz. Implementing such voltage-tunable resonators is the first step toward realizing wafer-scale continuous voltage control in superconducting circuits for qubit-qubit coupling, quantum limited amplifiers, and quantum memory platforms.

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I. INTRODUCTION

Advances in materials growth, fabrication, and device design have paved the way for the success of superconducting quantum systems based on solid-state platforms [1–6]. Recently, fixed frequency superconducting qubits have shown coherence times greater than 1 ms [7,8]; however, static *ZZ* crosstalk and parasitic coupling limits two-qubit gate fidelity [9]. On the other hand, flux-tunable circuits have garnered attention for their ability to eliminate unwanted interactions [10–13]. In addition, they have allowed for fast (approximately 30 ns) high-fidelity ($> 99\%$) two-qubit gates [14], as opposed to cross-resonance-based gates that typically take 150–200 ns [15,16]. These circuits are almost exclusively realized by flux-sensitive superconducting quantum interference devices (SQUIDs) [14,17–20]. However, conventional flux-tunable circuits have qubit phase coherence limited by low-frequency flux noise [21–24]. Alternatively, superconductor-semiconductor hybrid structures can be employed to provide voltage tunability for fast and low-power control. The fast gate switching times offered by transistorlike device architectures could be utilized for high-speed coupling and two-qubit gates. In addition, the local control imposed by voltage-tunable devices can offer a flexible design feature for large-scale device footprints.

In a Josephson junction (JJ) with a semiconductor weak link, Cooper pair transport is facilitated by Andreev reflections at the superconductor-semiconductor interface [25]. Multiple, coherent reflections form current-carrying Andreev bound states. As the Fermi energy tunes the occupation of each state, such as by an applied gate voltage V_G, the total critical current I_C can be controlled. Such tunability has been routinely demonstrated in current-biased devices [26–30] and utilized in qubit manipulation, specifically with gatemon qubits [31–42]. Furthermore, semiconductor weak links can directly find applications in the form of couplers [43–45], amplifiers [46], superconductor-coupled quantum dot devices [35,47–50] due to their voltage-tunability and potential for fault-tolerant quantum computation [51–53].

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In this work we present a wideband, wafer-scale implementation of a voltage-tunable resonator. The device is based on an InAs 2DEG and contacted with epitaxial Al fabricated into a Josephson junction embedded in a coplanar waveguide (CPW) resonator. We show that the Josephson inductance L_J is modified electrostatically by an order of magnitude, allowing for the resonant frequency to be tuned within a 2 GHz band. In addition, by studying the high-power response of the device we find that the junction exhibits nondissipative nonlinearity. The tunability of the resonator frequency allows for strong hybridization with another resonator on the chip. With a maximum coupling strength of $g = 51$ MHz, we achieve strong coupling between the two resonators.

II. DEVICE DESIGN

The devices are fabricated on a superconductor-semiconductor heterostructure grown via molecular beam epitaxy [54–57]; details of the growth are discussed in Appendix A. The weak link of the JJ is a high-mobility InAs 2DEG grown near the surface and contacted *in situ* by a thin aluminum film. The epitaxial heterostructure is grown on a 500-μm-thick InP substrate. We use a III-V wet etch to define the microwave circuit and an Al wet etch to define the JJ. The junction gap is 100 nm long and 35 μm wide. We then deposit a 60 nm AlO_x gate dielectric, followed by a gate electrode made of layers of Cr and Au that are 5 and 50 nm, respectively. A stitched optical image of the wirebonded device is shown in Appendix B in Fig. 8.

Measurements are conducted in a dilution refrigerator at a temperature of 30 mK. A schematic of the measurement setup is shown in Appendix C in Fig. 9, along with further details of the measurement setup. Using a vector network analyzer, we measure the complex transmission coefficient S_{21} as a function of probe frequency f . Power is referenced to the output of the vector network analyzer. A method of fitting S_{21} to a circle in the complex plane described in Ref. [58] is used to extract internal and external quality factors, Q_{ext} and Q_{int}, and resonant frequencies f_r.

A schematic of the chip design is shown in Fig. 1(a) with design parameters described in Table I. The designs were made using Qiskit metal [59]. The chip has four CPW resonators with a central conductor width $w = 35$ μm and spacing from the ground plane $s = 20$ μm. This implies a characteristic impedance of $Z_0 = 48.430\Omega$ calculated using a standard conformal mapping technique [60–62] assuming a dielectric constant of $\epsilon_r = 12.4$ for the InP substrate. The capacitance and inductance of the coplanar waveguides are then given by $C_0 = \pi/4Z_0\omega_0$ and $L_0 = 1/\omega_0^2 C$ with $\omega_0 = 2\pi f_0$, where f_0 is the resonant frequency calculated using finite-element analysis simulations [63]. These simulations also help us obtain Q_{ext}, characterizing the coupling to the common feedline. In three resonators a Josephson junction is galvanically connected to the end of the CPW, shunting it to ground. We call these devices tunable resonators (TR1, TR2, TR4). The Josephson inductance L_J is tunable by an applied gate voltage V_G via the top gate. One bare resonator (R3) does not include a shunting Josephson junction and is used as a reference. In this work we focus on devices TR1, TR2, and R3.

TABLE I. Design parameters of the coplanar waveguide resonators. The resonant frequency f_0 and the external quality factor Q_{ext} are calculated by finite-element analysis. The capacitance and inductance C_0 and L_0 are calculated analytically.

Resonator	l (mm)	f_0 (GHz)	Q_{ext}	C_0 (pF)	L_0 (nH)
TR1	4.936	5.967	270	0.433	1.645
TR2	4.136	7.111	201	0.363	1.380
R3	4.536	6.491	180	0.398	1.512
TR4	3.736	7.559	152	0.341	1.298

III. THIN-FILM KINETIC INDUCTANCE

In order to accurately determine the inductance contribution of the tunable JJ, we must properly characterize the kinetic inductance of the superconductor thin film. For an Al thickness of approximately 10 nm, we expect an appreciable kinetic inductance contribution to the total inductance of the resonator. We measure the kinetic inductance fraction $\alpha_K = 1 - (f_r/f_0)^2$ of a bare CPW, where f_r is the measured frequency of the CPW [64]. Figures 2(a) and 2(b) shows measurements of the phase and magnitude of complex transmission data S_{21} of the resonant mode of R3. We find the measured resonant frequency to be $f_r = 6.204$ GHz while the frequency based on the geometry of the resonator is found to be $f_0 = 6.491$ GHz, leading to a kinetic inductance fraction of $\alpha_K = 0.0867$. Considering the geometric inductance of R3, we find a kinetic inductance per square of $L_K^{\square} = 1.012$ pH. Using a two-fluid model to describe the contribution of kinetic inductance to the total inductance of the CPW [65], we fit $\Delta f_r(T) = f_r(T) - f_r(0)$ to the equation

$$\frac{\Delta f_r}{f_r(0)} = -\frac{\alpha_K}{2\left[1 - \left(\frac{T}{T_C}\right)^4\right]} + \frac{\alpha_K}{2}, \tag{1}$$

TABLE II. Critical power extraction parameters: summary of the parameters used to plot f_B in terms of the reduced units $\Omega = 2Q_L(f_r - f_B)/f_r$ and P/P_C.

V_G (V)	f_r (GHz)	Q_L	P_C (dBm)
5	6.114	435 ± 5	−64.3
0	6.114	473 ± 2	−64.5
−4	6.113	536 ± 2	−65.6
−8	6.100	497 ± 1	−64.7

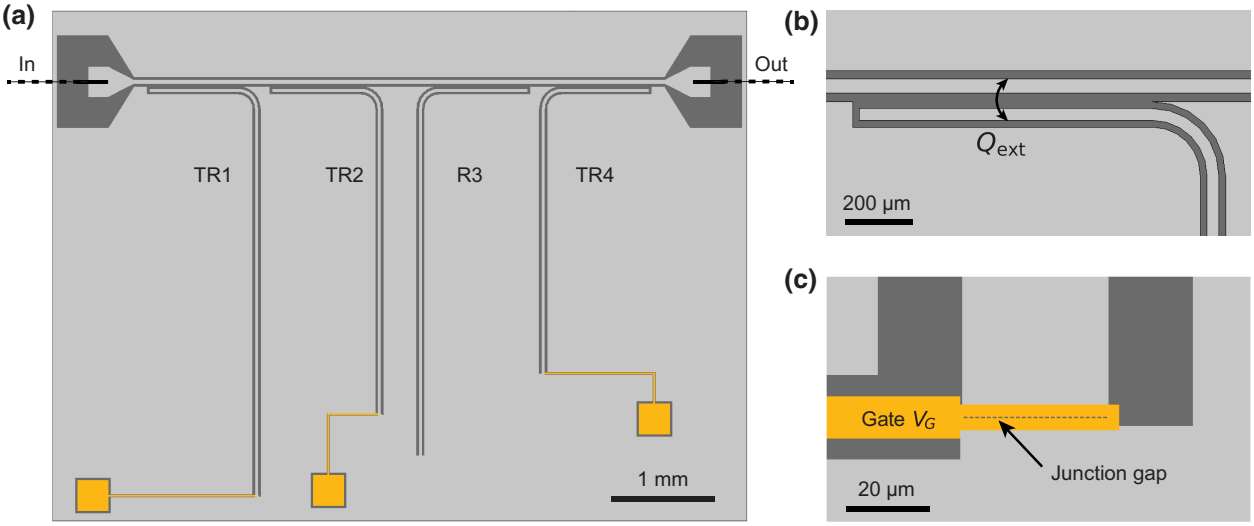

FIG. 1. Schematics of the chip design. (a) The design consists of four resonators coupled to a common transmission line. Three $\lambda/4$ coplanar waveguides (TR1, TR2, and TR4) are shunted to ground through a Josephson junction and biased by an applied top gate voltage V_G. One bare coplanar waveguide (R3) that does not have a junction is used as a reference for kinetic inductance characterization. The inset illustrates the coplanar waveguide geometry layout. (b) The resonators are capacitively coupled to the transmission line with an external quality factor of Q_{ext}. (c) A closeup illustrating the junction shorting the bottom end of the resonator to ground and the gate.

where T_C is the superconducting critical temperature and $f_r(0\text{ K}) \approx f_r(50\text{ mK})$. For $\alpha_K = 0.0867$, we find that $T_C = 1.244 \pm .060$ K corresponding to a superconducting gap of $\Delta_0 = 1.75 k_B T_C = 187 \pm 9$ μeV consistent with reported values for Al thin films [26,51]. We note that the kinetic inductance probes the superconducting condensate that also has a contribution from the InAs 2DEG along with the thin Al film [66].

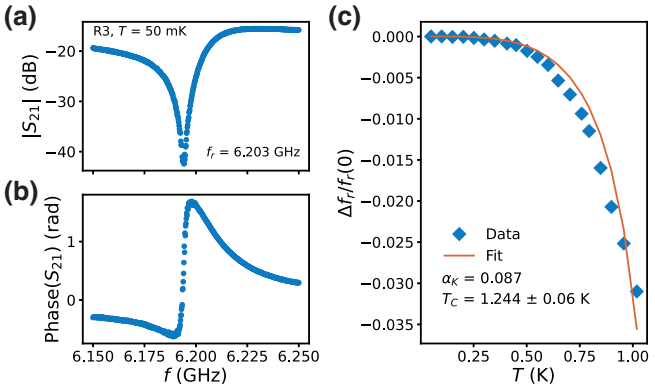

FIG. 2. Kinetic inductance extraction from R3. (a) Magnitude and (b) phase of the complex transmission S_{21} shown as a function of frequency. (c) Change in frequency δf_r as a function of temperature T as well as a fit to a two-fluid model with T_C as a fitting parameter and α_K fixed. Data are taken at a power corresponding to $\langle n \rangle \sim 3 \times 10^4$ photons in the cavity.

IV. GATE-VOLTAGE TUNABILITY

In order to achieve a wide tunability band, the junction must participate highly in the circuit. By galvanically connecting the junction to the CPW, we create an element that is continuously tuned in a wide dynamic range. In Fig. 3(a) we show $|S_{21}|$ vs f while varying the gate voltage V_G of TR2. The data taken here are at a power of −96 dBm. Two resonances are observed corresponding to the TR1 and TR2 modes at frequencies f_1 and f_2, respectively. As V_G tunes the occupation of the current-carrying conduction channels in the JJ, there is a resulting decrease in the critical current I_C, which is related to the Josephson inductance through $L_J = \Phi_0/2\pi I_C$, where Φ_0 is the magnetic flux quantum. We find consequently that the TR2 mode is tuned to lower frequencies as the gate voltage decreases, showing a range of 2 GHz between $V_G = 0$ and −14 V, beyond which the resonant frequency drops outside of the measurement bandwidth of our setup.

Using $L_K^{\square}$ calculated from R3, we can simulate the effect of the varying Josephson junction L_J on the TR2 mode. By accounting for the effect of kinetic inductance in finite-element simulations, we calculate the resonant frequency as a function of L_J, which is represented by a lumped element inductor. Comparing these results to the measured frequencies, we obtain L_J and I_C as a function of V_G shown in Fig. 3(b). We find that L_J is highly tunable, increasing more than an order of magnitude between the highest and lowest V_G points. One can define the Josephson inductive participation ratio in this circuit to be $p_J = L_J/(L_J + L_0 + L_K)$. Using the value of L_0 for TR2 and L_K calculated by

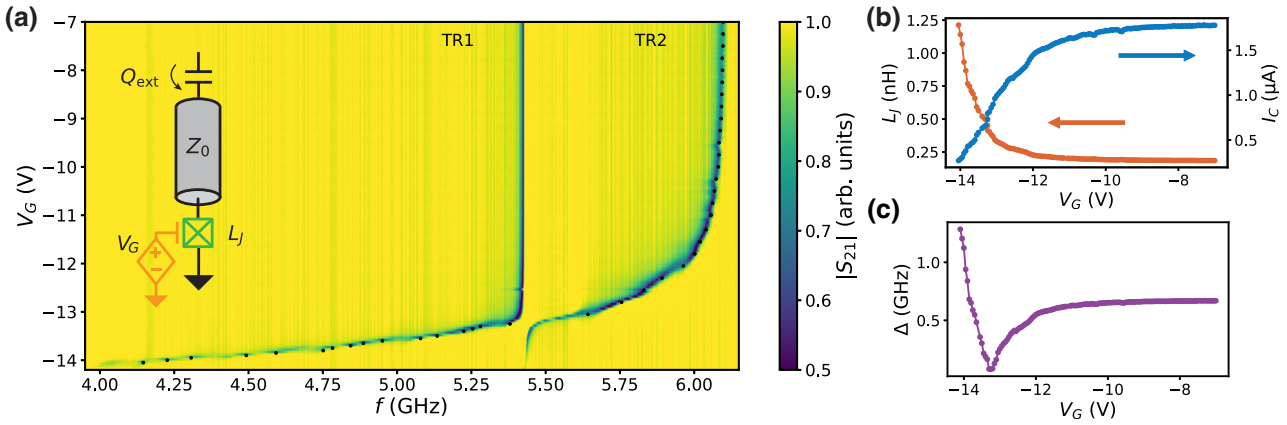

FIG. 3. Gate-voltage tunability of TR2. (a) The magnitude of the complex transmission coefficient S_{21} as a function of probe frequency f and gate voltage V_G, voltage applied to the top gate of TR2. Two resonant modes can be seen, TR1 at 5.4 GHz, and TR2 that starts at 6.1 GHz and is tuned to lower frequencies as V_G decreases. (b) Extracted resonant frequencies of TR2 are mapped to Josephson inductance values L_J of TR2 evaluated from finite-element calculations. Mirrored is the junction critical current $I_C = \Phi_0/2\pi L_J$, where Φ_0 is the magnetic flux quantum. (c) The detuning $\Delta = |f_+ - f_-|$ between mode TR1 and TR2 as a function of V_G.

the kinetic inductance fraction, we find that at the lowest gate voltage measured $p_J = 44.72\%$, implying significant participation of the junction in the circuit. Previous studies based on InAs-Al nanowires have been restricted by either a limited tunability range or discrete switching of the coupler frequency [43,67]. The wide range and continuous tunability of this 2DEG-based device are advantageous for tunable coupling schemes.

Near $V_G = -13$ V we find that the two modes undergo an avoided-level crossing. We define the difference in frequencies of the two modes as the detuning $\Delta = |f_+ - f_-|$, where f_+ and f_- are the high- and low-frequency modes, respectively. We show Δ versus gate voltage in Fig. 3(c) and find that at 0 V applied, $\Delta = 669$ MHz, while at the strongest coupling, Δ decreases to 79 MHz. At large negative gate values, Δ then increases to 1.285 GHz at the lowest frequency of the TR2 mode. The on:off coupling ratio can then be determined as the detuning at the weakest coupling divided by the detuning at the strongest coupling. We find that the on:off coupling ratio at no applied gate voltage with $f_2 > f_1$ is 8.47, and at large negative gate voltage with $f_2 < f_1$ is 16.27. The latter value is limited by our measurement setup bandwidth and can be expected to increase further. We note that outside the strong-coupling regime, the frequency of the TR1 mode remains unchanged due to the local effect of the TR2 gate, resulting in no detectable crosstalk.

V. JOSEPHSON JUNCTION NONLINEARITY

One outstanding question in using voltage-tunable junctions is whether the gate-voltage control introduces power-dependent dissipation to the system along with the nonlinearity. This has previously been studied by embedding a JJ in a CPW and studying its high-power response [68]. We employ a similar study as in Josephson tunnel junctions to understand the impact of gate voltage on the junction nonlinearity.

A combined CPW-JJ system can be described classically by a Duffing oscillator [69,70], where the nonlinearity gives rise to a power-dependent resonant frequency. At low input powers P, the response has a familiar Lorentzian line shape centered around the resonant frequency f_r with a linewidth Q_L. As P increases, the resonant frequency shifts to lower values, and at a critical power P_C, the response becomes multivalued with two metastable solutions existing at a single frequency. This phenomenon is known as bifurcation and is the basis for Josephson bifurcation and parametric amplifiers [46,71–74].

In order to keep track of the frequency at which bifurcation develops, we look at the susceptibility $-\partial|S_{21}|/\partial f$. We label the frequency at which the susceptibility is maximum f_B. Assuming the low damping limit following Refs. [68,70], one can rescale f_B to the reduced frequency $\Omega = 2Q_L(f_r - f_B)/f_r$. In this way, we expect Ω to be described by the curve

$$P/P_C = \frac{1}{12\sqrt{3}}\Omega^3\left[1 + \frac{9}{\Omega^2} \mp \left(1 - \frac{3}{\Omega^2}\right)^{2/3}\right] \quad (2)$$

for powers $P > P_C$ and

$$P/P_C = \Omega\sqrt{3}/2 - 1/2 \quad (3)$$

for $P < P_C$.

Figures 4(a) shows the power-dependent response of the TR2 mode with a gate voltage $V_G = -4$ V applied to the gate electrode of TR2. We keep all other gates grounded. As the power increases, the resonant frequency

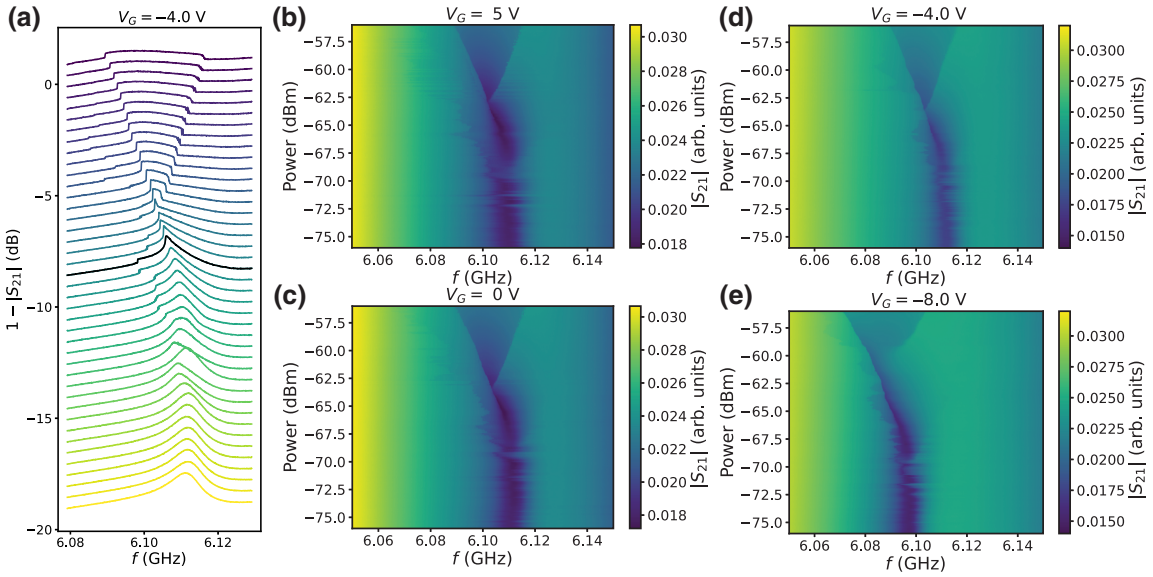

FIG. 4. Nonlinear response of TR2. (a) The magnitude of the complex transmission S_{21} plotted versus frequency f at various different input powers, where the top curve is at the highest power of $P = -56$ dBm while the bottom curve is at $P = -76$ dBm. The curve that corresponds to S_{21} at $P = P_C$ is shown in black. (b–e) Power dependence of the Josephson bifurcation at different gate voltages.

shifts towards lower values, and when $P > P_C$, an apparent discontinuity appears in the data. This is due to the hysteretic behavior of the bifurcation. Since we sweep the frequency in the positive direction, we probe only one solution branch at a time at powers greater than P_C, and the apparent discontinuity corresponds to a jump from low- to high-amplitude solution branches. We find P_C by identifying when the susceptibility first diverges. Further details on the procedure used to extract P_C are described in Appendix E and shown in Fig. 11. For $V_G = -4$ V, we find that $P_C \sim -66$ dBm; the curve at this power is shown in black in Fig. 4(a). We note that the bifurcation of the TR2 mode is absent in the R3 mode. This implies that the nonlinearity in TR2 is mainly caused by the presence of the Josephson junction and not by the kinetic inductance of the thin Al film, as has been reported in other high kinetic inductance superconducting materials [75–77].

We analyze the power-dependent response at different gate voltages shown in Figs. 4(b)–4(e). We find that as the gate voltage is decreased, P_C decreases as expected. Plotted in terms of the reduced frequency, in Fig. 5 we show Ω vs P/P_C at four different gate-voltage values plotted with the theoretical curves predicted by Eqs. (2) and (3). To rescale f_B to the reduced frequency Ω, Q_L and f_r are extracted from the fit of the resonance at $P = -76$ dBm. A discussion on rescaling the data with the reduced parameters is in Appendix E.

We find that when plotted in terms of the reduced parameters, the data fall on the theoretical curve. Since the solutions to the Duffing model assume the low damping limit, agreement between the data and the theoretical prediction implies that the nonlinearity present in the superconductor-semiconductor junction is not caused by nonlinear dissipative effects. Furthermore, we find that this is true at all four gate voltages, reassuring the fact that applying a gate voltage introduces no additional power-dependent dissipation to the junction. Similar results showing the

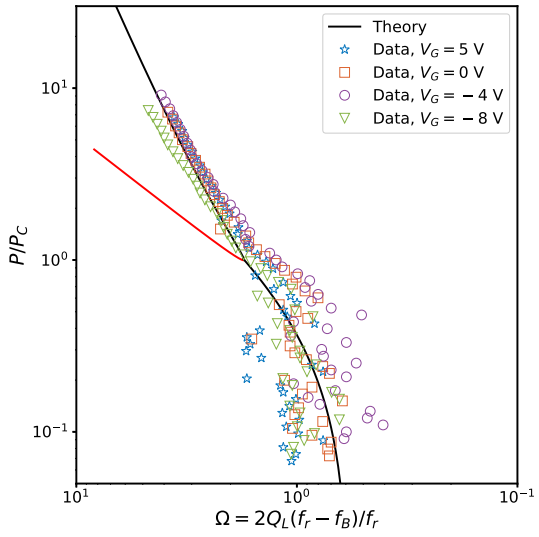

FIG. 5. Frequencies at which the susceptibility $-\partial S_{21}/\partial f$ is maximum, plotted in terms of reduced parameters Ω and P/P_C for different gate voltages. Solutions to the Duffing equation are shown in black and red, with the two solution branches meeting at $P = P_C$. When plotted in these reduced units, we find there is good agreement between the data and the universal curve.

absence of power-dependent dissipation has been previously reported in AlO_x-Al junctions [68], indicating that InAs-Al junctions have a similar nonlinearity. A discussion about microwave loss mechanisms and mitigation is provided later in this text. Deviations from the expected theoretical curve are most likely due to underestimating f_r by taking it at a relatively high power $P = -76$ dBm compared with the critical powers here.

VI. AVOIDED-LEVEL CROSSING

The wideband voltage tunability allows for coupling different resonators on the same chip. The coupling mechanism can be understood by studying the electric field distribution in the coupled and decoupled regimes, calculated using finite-element analysis methods. We find that in the decoupled scenario, at each resonant frequency, the electric field squared is distributed in the corresponding resonator, as expected, in Fig. 6(a). This occurs when L_J of the tunable resonator is set to $L_J = 0.00$ nH. By tuning L_J of the tunable resonator towards the frequency of the lower-frequency mode, the two modes begin to hybridize, with the electric field energy now occupying both resonators. This corresponds to the strongly coupled regime, occurring when $L_J = 0.38$ nH with a negative applied gate voltage.

The data presented in Fig. 6(b) show such hybridization between TR2 and TR1 as TR2 is tuned to $V_G = -13$ V resulting in an avoided-level crossing. By extracting the resonant frequencies of the two modes, we fit the data to a simple two-oscillator picture,

$$f_{\pm} = \frac{1}{2}(f_1 + f_2) \pm \sqrt{\left(\frac{g}{2\pi}\right)^2 + \frac{1}{2}(f_1 - f_2)^2}, \qquad (4)$$

where $g/2\pi$ is the coupling strength, and f_1 and f_2 are the uncoupled frequencies corresponding to the TR1 and TR2 modes, respectively. In this narrow gate-voltage range, we assume the TR2 mode to have a frequency f_2, which is approximately linear with the gate voltage changing at a rate of 0.628 ± 0.033 GHz/V. The TR1 mode is fixed at $f_1 = 5.427$ GHz. Extracting the frequencies f_+ and f_- from the data, we fit the two curves to obtain a coupling strength $g/2\pi = 51.203 \pm 1.104$ MHz, as shown in Fig. 6(c). This value for $g/2\pi$ taken from the fit to a two-oscillator model is consistent with the conventional definition for $g/2\pi$ being equal to half the minimum detuning, $\min(\Delta)/2$, which yields $g/2\pi = 51.765$ MHz. We note that the coupling strength at this lower power is a bit larger than that which is found at higher power and shown in Fig. 3 of $\min(\Delta)/2 = 39.489$ MHz.

We hope to show that this device exhibits the basic necessary working principles to implement a tunable coupler using this architecture. The wideband tunablity of the InAs 2DEG device in particular demonstrates the advantage of using this over InAs nanowire-based devices. In addition, the large coupling to another device on the same chip demonstrates a proof-of-principle experiment in which this tunable element can be used to couple different superconducting circuit elements on the same chip. We hope to use this device architecture for various applications that include as a tunable coupler between, say, two fixed frequency transmons or two gatemons. It has been shown that, for a coupler with a 10-μs lifetime, a 50-ns CZ gate can be implemented with a gate fidelity of 99.5% [44]. An alternative use case for this circuit is to implement a quantum memory that utilizes dynamically tunable couplers to access "storage cavities" that can store information. More details of such a device can be found in Ref. [45]. We hope to demonstrate in this report the ability to continuously tune the tunable resonator over a wideband, and in future experiments we would like to test dynamic tunability by sending high-frequency control signals through the gate-voltage line.

TABLE III. Summary of samples measured for microwave loss characterization, with TR2 and R3 samples mentioned earlier in the report. Deposition conditions for samples with *in situ* Al are nominally identical and yield an approximately 10-nm-thick film. The substrate refers to both the 500-μm-thick InP substrate, as well as the III-V overlayers, referred to here as "buffer." Tunable resonator samples with a Josephson junction and gate are specified with the gate electrode material, being either a Cr and Au combination or Al.

Device	Superconductor	Substrate	Gate
S1-TR2	10 nm *in situ* Al	1-μm buffer	Cr-Au
S1-R3	10 nm *in situ* Al	1-μm buffer	
S2	100 nm sputtered Al	InP	
S3	10 nm *in situ* Al	400-nm buffer	
S4	10 nm *in situ* Al	1-μm buffer	Al

VII. MICROWAVE LOSS MEASUREMENTS

A necessary consideration for the implementation of materials for superconducting qubit circuits is microwave loss. While semiconductor 2DEGs can offer wideband gate-tunable JJs, in this section we try to understand mechanisms that limit coherence in our devices.

We fabricate and measure a series of CPW resonators and obtain internal quality factors Q_{int} for each sample. These samples aim to study loss mechanisms introduced by specific device conditions. These include loss due to the substrate, the epitaxial III-V layers, the thin-film superconductor, and the gate electrode. Details of the devices are discussed in Table III and further information can be found in Appendix B.

We show a summary of these measurements in Fig. 7 where we present power dependence of Q_{int} for all samples. We find an internal quality factor for the CPW on

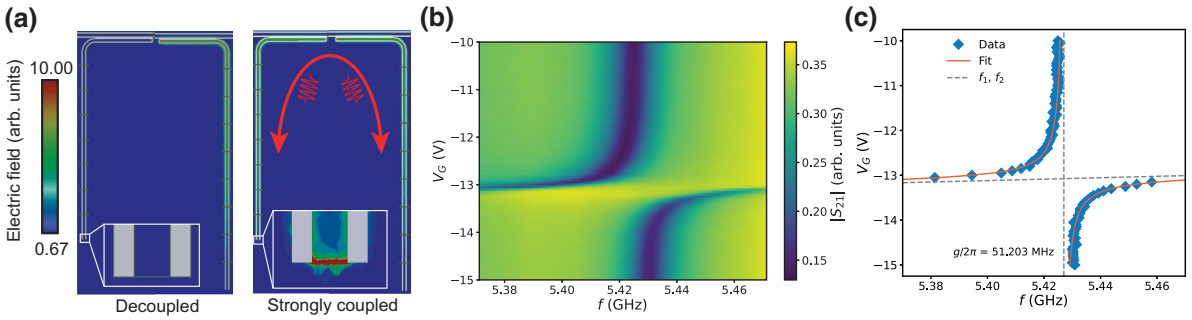

FIG. 6. Avoided-level crossing of TR1 and TR2 via the gate-voltage tuning of TR2. (a) Finite-element calculations of the electric field distribution at a frequency of 5.967 GHz are shown at two values of Josephson inductance. In the "decoupled" scenario, the two modes are detuned, where the Josephson inductance is $L_J = 0.00$ nH, corresponding to 0 V applied gate voltage. In the "strongly coupled" scenario, the TR2 mode is brought into resonance with TR1 and the two are able to exchange energy mediated by photon swap. This occurs when the Josephson inductance $L_J = 0.38$ nH, corresponding to a large negative applied gate voltage. (b) Color plot of the magnitude of S_{21} versus probe frequency f and gate voltage V_G. Near $V_G = -13$ V, strong coupling occurs between the TR2 and TR1 modes and an avoided-level crossing is observed. Data are taken at a power corresponding to $\langle n_{\text{photon}} \rangle \sim 13$ photons. (c) Extracted frequencies as well as a fit to a two-oscillator model. The fit yields a coupling strength of $g/2\pi = 51.203 \pm 1.104$ MHz.

InP to be $Q_{\text{int}} = 2.58 \times 10^4$ at an average photon number of $\langle n_{\text{photon}} \rangle = 21$. This is consistent with other reports of Q_{int} for CPW resonators on InP substrates [35] and piezoelectricity has commonly been attributed as the dominant loss mechanism [78,79]. By growing the III-V heterostructure on Si, it should be possible to increase the upper bound on Q_{int} for these circuits to more than 10^6 [80]. Alternatively, one can use a flip-chip device design, to concentrate the energy participation in a low-loss probe wafer [81].

We compare the results for CPWs on the InP substrate to the bare resonator device, R3 on sample S1. We find that at low power, $Q_{\text{int}} = 2.25 \times 10^3$. To understand the source of this added loss, we also measure a sample with a 400-nm epitaxial III-V layer, S3. We find that Q_{int} is almost identical to that of R3 in sample S1 that has a 1-μm epitaxial III-V layer. The differences in energy participation of the buffer layers for the 400-nm and 1-μm buffers are

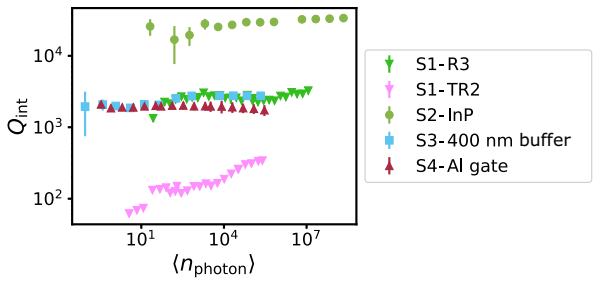

FIG. 7. Microwave loss measurements. (a) Internal quality factor Q_{int} as a function of the average number of photons in the cavity $\langle n_{\text{photon}} \rangle$ for CPWs on four different samples: a bare CPW, R3, and tunable resonator, TR2, bare CPW on an InP substrate, a bare CPW on a 400-nm buffer layer, and a tunable resonator with an Al gate electrode.

3.5% and 7.0%, respectively. Details of the participation ratio calculations can be found in Appendix F. Despite the increased epitaxial III-V layer participation, we find that in our devices the epitaxial III-V layers do not significantly affect Q_{in}. Thus, we believe this decrease in Q_{int} is due to the Al thin film. This has previously been observed in other high kinetic inductance materials, such as Nb-Ti-N thin films and nanowires [77,82,83].

We next consider loss due to the gate electrode. While the large participation of the Josephson junction in the circuit provides considerable frequency tunability, the electric field across the junction may couple to the gate electrode. We find that in sample S1, at low power, the TR2 mode has $Q_{\text{int}} = 1.43 \times 10^2$, an order of magnitude lower than

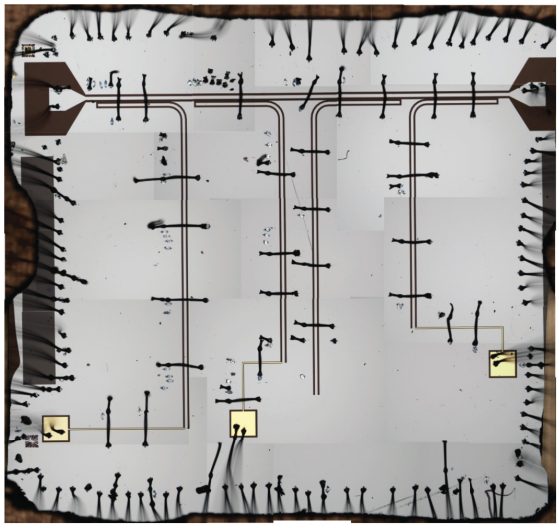

FIG. 8. Fabricated chip image. Stitched optical image of the wirebonded device loaded in the microwave sample holder.

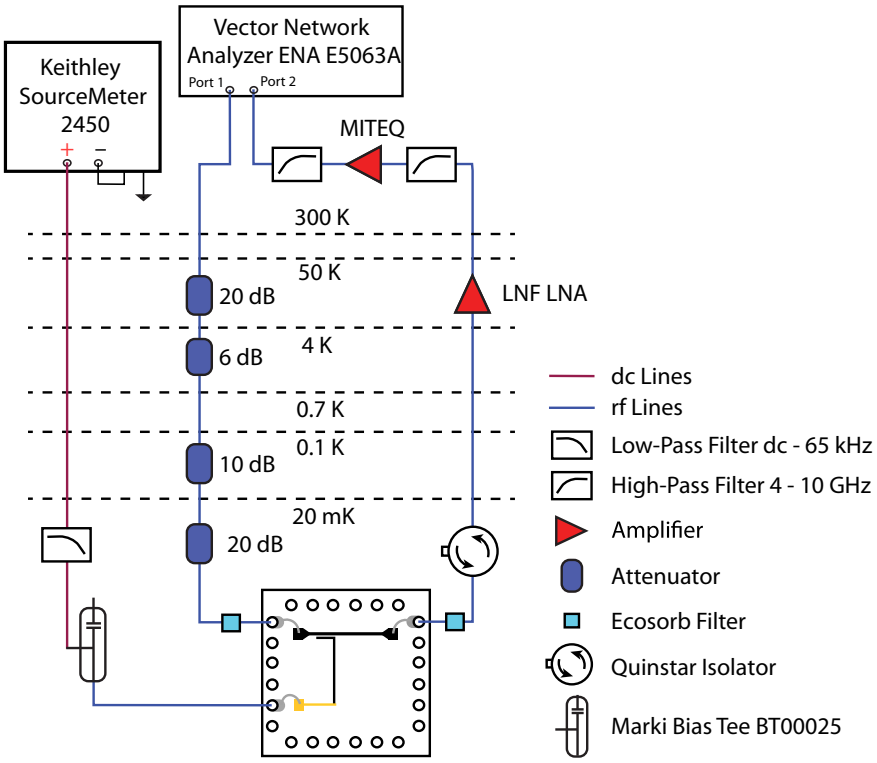

FIG. 9. Measurement setup. A schematic of the cryogenic and room-temperature measurement setup.

that of R3 on the same chip. We compare this to sample S2 that has a tunable resonator that replaces the Cr-Au gate with Al. We find that Q_{int} of this device is 1.83×10^3 at low power, approaching that of S1-R3 and S3. This suggests that TR2 has coherence limited by the Cr-Au gate electrode. In addition to the findings raised here, promising directions in reducing losses in these materials are using hexagonal boron nitride (h-BN) as a gate dielectric, [84,85]. This discussion hopefully provides a path forward for increasing the Q_{int} of tunable resonators on InAs 2DEGs.

VIII. CONCLUSION

In conclusion, we demonstrate the wideband tunability of a superconductor-semiconductor-based tunable resonator. We show that the gate-voltage-tunable junction has a nondissipative nonlinearity, ideal for implementing in superconducting qubit circuits. After adjusting for the kinetic inductance of the Al thin film, we find that the Josephson inductance is tunable by up to an order of magnitude, achieving a high participation in the circuit of 44%. This high participation enables us to continuously tune the resonant frequency of the tunable resonator mode by more than 2 GHz. We also show that by tuning the tunable resonator mode into resonance with another resonator on the chip, we observe hybridization of the two modes through an avoided-level crossing, with a coupling strength of 51 MHz. The wide tunability range results in large detuning of the two modes resulting in an on:off detuning ratio of approximately 16 at a large negative gate voltage and approximately 8 at 0 V applied. While Q_{int} is quite low, we find that the coherence is limited by the normal metal gate line and we discuss tangible improvements that can be made to material and device design that can significantly enhance Q_{int} of InAs 2DEG tunable resonators. The ability to achieve strong coupling and large detuning between the two modes makes this device design an ideal platform for qubit-qubit coupling schemes and quantum information storage where the TR mode, acting as a coupler, can be brought into resonance with a fixed frequency mode by dynamically pulsing the gate.

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APPENDIX A: MATERIALS GROWTH

The devices studied are fabricated on a heterostructure grown by molecular beam epitaxy. On an epi-ready, semi-insulating 500-μm-thick InP (100) substrate, a 50-nm-thick $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ superlattice of ten periods is grown followed by a 50-nm-thick $In_{0.52}Al_{0.48}As$ layer and a 800-nm-thick $In_xAl_{1-x}As$ graded buffer layer in which the composition is step graded between $x = 0.52$ and 0.81 in steps of $\Delta x = 0.02$. This is followed by a 50-nm $In_{0.81}Al_{0.19}As$ virtual substrate. The structure is then modulation doped with Si at a density of $n_D = 1 \times 10^{12}$ cm^2. Following a 6-nm $In_{0.81}Al_{0.19}As$ spacer, an InAs near-surface quantum well is then grown between two layers of $In_{0.81}Ga_{0.19}As$, where the top barrier layer is 10 nm thick and the bottom barrier layer is 4 nm thick. The structure is then capped with a 10-nm layer of Al grown *in situ*. Further details on the materials growth procedure are provided in Refs. [54–57]. Through low-temperature magnetotransport measurements, we find the wafer used in this device has a two-dimensional electron density of $n = 9.49 \times 10^{11}$ cm^{-2} and an electron mobility of $\mu = 1.45 \times 10^4$ cm^2/Vs measured along the [110] crystal direction. This corresponds to an electron mean free path of 233 nm. With the Josephson junction weak link being 100 nm long, the junction is expected to be in the short ballistic regime [26].

APPENDIX B: DESIGN AND FABRICATION

The design is constructed using Qiskit metal [59] and rendered in ANSYS's high-frequency simulation software (HFSS) [63] to simulate for the expected resonant frequency, external quality factors, and electromagnetic field distribution. We use electron-beam lithography to define patterns in spin-coated PMMA resist. To define the microwave circuit, Al is removed with Transene Al etchant type D followed by a wet etch down to the buffer layer using a III-V etchant consisting of phosphoric acid (H_3PO_4, 85%), hydrogen peroxide (H_2O_2, 30%), and deionized water in a volumetric ratio of 1:1:40. To define the Josephson junctions, we etch away a 100 nm long, 35 μm wide strip of aluminum from the CPW mesa. We then deposit 60 nm of AlO_x to serve as a gate dielectric by atomic-layer deposition at 120 °C. This is followed by another electron-beam lithography patterning step to define the gate pattern and an electron-beam deposition of the gate electrode, consisting of 8 nm of Cr and 80 nm of Au. An optical image of the fabricated and wirebonded chip is shown in Fig. 8.

A series of samples are used to fabricate CPW devices for Q_{int} measurements. The first is a CPW with 100 nm Al deposited on an InP substrate. The second is a 400-nm-thick III-V heterostructure grown by MBE with a thin *in situ* deposited Al film. The last is a CPW on the same wafer as that which is reported here, but with superconducting Al as the gate electrode as opposed to a combination of Cr and Au. The 400 buffer resonator is fabricated on the thin *in-situ* aluminum on a similar layer structure as mentioned in this report, but with graded buffer layer steps of 20 nm rather than 50 nm, giving rise to a total thickness of approximately 400 nm. The Al growth conditions are nominally identical to that of the wafer presented previously. The InP wafer has 100 nm aluminum sputtered by dc magnetron sputtering after an Ar plasma cleaning in order to etch the native oxide. The design consists of a common feedline with hanger $\lambda/4$ CPW resonators with the same central conductor width and spacing to the ground plane as the device in the main text. The simulated Q_{ext} for each CPW is 7830. The measured resonant frequency of the InP resonator is $f_r = 7.717$ GHz and that of the 400-nm buffer resonator is $f_r = 7.415$ GHz.

APPENDIX C: MEASUREMENT SETUP

A schematic of the measurement setup is shown in Fig. 9. Measurements are conducted in an Oxford Triton dilution refrigerator. The sample is embedded in a QCage, a microwave sample holder manufactured by QDevil, and connected to the printed circuit board by aluminum wirebonds. Probe signals are sent from a vector network analyzer (port 1) attenuated by −56 dBm with attenuation at each plate as noted. Attenuators are made by XMA. The signal then passes through a 1–18 GHz bandpass filter made by a copper box filled with cured Eccosorb castable epoxy resin. The signal is sent through the sample and returned through another Eccosorb filter, passed through an isolator with 20 dB isolation and 0.2 dB insertion loss, and then amplified with a low noise amplifier mounted to the 4K plate, as well as a room-temperature amplifier (MITEQ) at room temperature. The gate electrode is connected to a voltage source and passed through a QFilter, a low-pass filter manufactured by QDevil, mounted at the mixing chamber plate.

APPENDIX D: TUNABLE RESONATOR DESIGN

The details of the tunability the junction provides depends heavily on aspects of the design. The device presented in the manuscript has the JJ at the bottom of the resonator, directly shorting it to ground. Here, we also consider two other cases where the junction is in the middle and at the top of the resonator. As seen in Fig. 10, having the junction at the bottom of the resonator provides slightly more tunability in f while enhancing the value of Q_{ext} compared with the two other cases. On the other hand, having the junction at the top (right before the bend) of the resonator provides slightly less tunability in f while barely

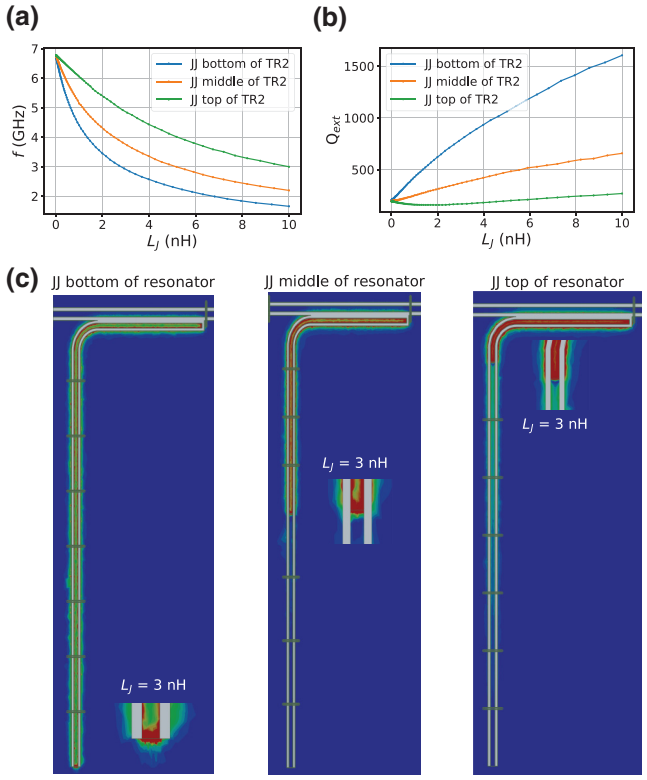

FIG. 10. Effect of changing the position of the JJ in the tunable resonator. (a) Resonant frequency f and (b) Q_{ext} presented as a function of L_J for three different cases: where the junction is at the top, middle, and bottom of the resonator. (c) Finite-element calculations of the electric field distribution for each case with $L_J = 3$ nH. The inset shows a zoom in image of the junctions.

changing Q_{ext}. The range tunability of Q_{ext} can be modified further by changing the initial value of Q_{ext} and by switching the open and grounded ends of the CPW.

Figures 10(c) presents the electric field profile of TR2 for the three cases with $L_J = 3$ nH. The distribution and concentration of the field can be seen to vary with the position of the junction. With the junction at the top of the resonator, the field can be seen to be restricted to the top part of the resonator while the rest of the resonator is isolated. This kind of isolation is ideal for superconducting quantum memory [45].

APPENDIX E: CRITICAL POWER EXTRACTION

In the bifurcation analysis we find the critical power P_C by analyzing the signal $S(f,P) = -|S_{21}(f,P)|$, which is a function of frequency f and input power P. By discrete differentiation with respect to f for fixed P, we get $(\partial S/\partial f)_P$. The data is sampled with 1201 points in a span of 100 MHz. The frequency at which the curve exhibits the highest derivative $\max(\partial S/\partial f)_P$ is defined as f_B and the value of the derivative at this point is $(\partial S/\partial f)_{f_B,P}$, which depends on the power P.

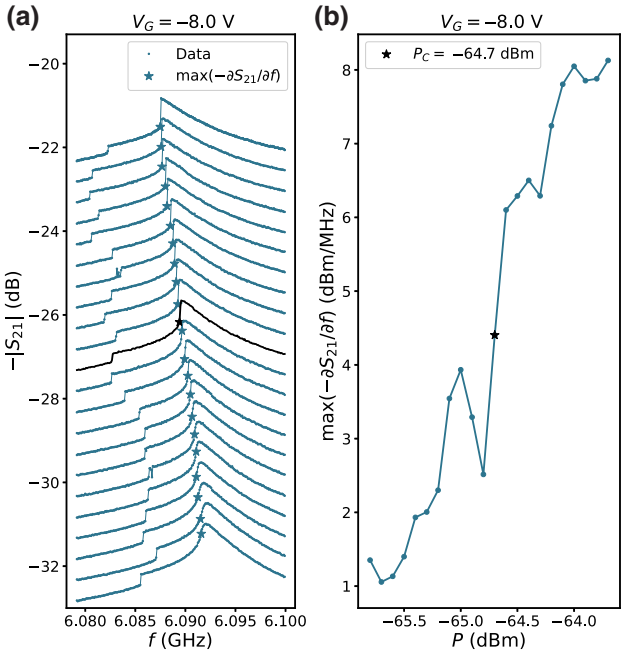

FIG. 11. Extracting the critical power P_C. (a) Linecuts of $-S_{21}$ as a function of probe frequency f plotted at different input powers P with linecuts spaced for clarity. The top trace has $P = -56$ dBm and the bottom trace has $P = -76$ dBm. (b) The derivatives of $\max(-\partial S_{21}/\partial f)$ evaluated as a function of P. The power at which this function is maximum is the critical power P_C, shown for this set of data as -64.7 dBm.

As P increases, the critical point can be identified when $\partial S/\partial f$ first diverges. This divergence is due to the nature of the multivalued solution of the Duffing equation that governs the systems behavior. When sweeping the frequency forward (from negative to positive), we find that the vector network analyzer probes only one solution branch at a time at powers greater than P_C. This gives rise to an apparent discontinuity in the data as seen in Fig. 11(a). We note that both solutions can be observed if one were to probe the system by sweeping frequency in the backward direction.

In order to identify the critical point, we look for a sharp increase in $(\partial S/\partial f)_{f_B,P}$ as a function of P. By taking a second derivative with respect to P, we identify at which power a sharp increase occurs by finding the maximum,

$$\max\left(\frac{\partial}{\partial P}\left[\left(\frac{\partial S}{\partial f}\right)_{f_B,P}\right]\right).$$

The critical power P_C is the power P at which this occurs. Here, $\partial P = 0.1$ dBm. An example of such an extraction for $V_G = -8$ V is presented in Fig. 11 and we summarize the various P_C extracted for different gate voltages shown in Table II. We also include the frequencies f_r and loaded quality factor Q_L used to rescale f_B for Fig. 11.

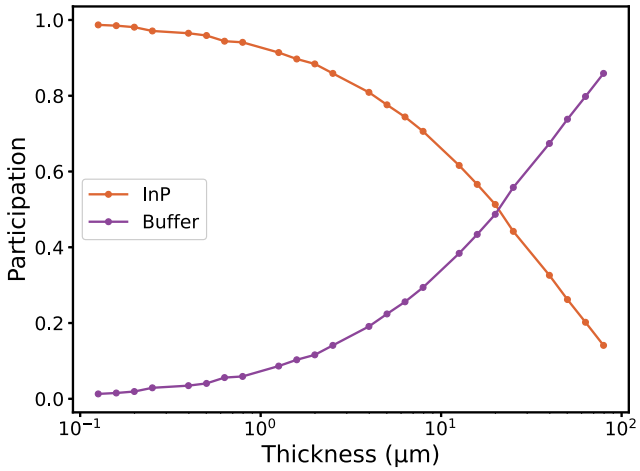

FIG. 12. Participation ratio of buffer and InP as a function of buffer layer thickness.

APPENDIX F: PARTICIPATION RATIO CALCULATIONS

We further understand the buffer layer contributions to the loss by calculating the participation p_i of the buffer layer and substrate as a function of buffer layer thickness using finite-element analysis (HFSS [63]). The participation ratio is the ratio of the total electric field squared integrated over each volume V_i,

$$p_i = \int_{V_i} \frac{|E^2|}{|E^2_{\text{tot}}|} dV.$$

Here i only takes into account the 500-μm InP substrate and the buffer layer. Figures 12 shows p_i of the buffer layer and InP as a function of the thickness of the buffer layer. The participation ratio of the buffer layer is seen to increase with the thickness of the buffer layer, which is expected.

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