Temperature Control of Diffusive Memristor Hysteresis and Artificial Neuron Spiking

D.P. Pattnaik,[1,*,‡] Y. Ushakov,[1,‡] Z. Zhou,[2] P. Borisov,[1] M.D. Cropper,[1] U.W. Wijayantha,[3] A.G. Balanov,[1] and S.E. Savel′ev[1,†]

[1] *Department of Physics, Loughborough University, Loughborough LE11 3TU, United Kingdom*

[2] *Loughborough Materials Characterisation Centre, Loughborough University, Loughborough LE11 3TU, United Kingdom*

[3] *Department of Chemistry, Loughborough University, Loughborough LE11 3TU, United Kingdom*

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Memristive devices are promising elements for energy-efficient neuromorphic computing and future artificial-intelligence systems. For diffusive memristors, resistive switching occurs because of the sequential formation and rupture of conduction filaments between device electrodes due to drift and diffusion of silver nanoparticles in the dielectric matrix. This process is governed by the applied electric voltage. Here, both in experiment and in simulations we demonstrate that varying temperature offers an efficient control of memristor states and charges transport in the device. By raising and lowering the device temperature it is shown that the memristive state can be reset, even if it cannot be done by varying the applied voltage. In addition, a change in the spiking regime is observed when the spiking is generated in the memristive circuit at a constant applied voltage, but different device temperatures. Our simulations demonstrate a good qualitative agreement with the experiments, and help to explain the effects reported.

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I. INTRODUCTION

In its simplest form, a memristor consists of an insulating or semiconducting film sandwiched between two metallic electrodes. The switching layer [1,2] undergoes dynamic material reconfiguration under the influence of external electric field or current. This reconfiguration manifests as a recurring change in the device resistance switching between a low resistance state (LRS) and a high resistance state (HRS) observed in various devices and films [3–6].

Among different types of memristors, diffusive memristors, which are based on metal atom diffusion and spontaneous formation and rupture of conduction filament (CF), hold much promise for the next-generation neuromorphic applications [7–9]. The general mechanism of this switching process is explained by the electric-field-induced migration of metal atoms in the form of metal nanoparticle (NP) suspended in a dielectric matrix [10–12]. Such a migration can be modeled by an electrically biased diffusion, where the diffusion constant changes in time due to Joule heating [13] affecting device temperature and, thus, NP diffusion constant. The external field promotes the metal NP to form CFs between the electrodes. The formation and dissolution of these CFs are dictated by the surface energy of the nanoparticles [14,15].

Due to inhomogeneities in the composition of the dielectric film [16] and roughness of the electrodes, the NPs forming CFs can be pinned [17,18]. That affects CF rupture and the endurance and eventually can cause degradation of the memristive devices. In this case, degradation of a memristor is manifested as a device failure in which the memristor resistance is stuck in a highly conductive state due to permanent CFs formed between the electrodes [19]. Subsequent voltage sweeps cannot rupture the CFs and reset the memristor resistance state. This is a major drawback of these diffusive memristor devices for technological applications where endurance and retention time are key characteristics [20–22]. To date, no approaches have been proposed to rupture CF. Together with the bias voltage, the Joule heating plays a useful role in nanoparticle dynamics, however, the effects of the dielectric matrix temperature on the process of filament formation and the related charge transport are poorly understood

In this work, we experimentally study the impact of the memristor device temperature on its current-voltage characteristics and voltage oscillations generated in a memristive circuit of an artificial neuron [23]. Our theoretical analysis confirmed that the device temperature can

*D.Pattnaik@lboro.ac.uk
†S.Saveliev@lboro.ac.uk
‡D.P. and Y.U. contributed equally to the paper.

control and reconfigure the formation and dissolution of CFs in diffusive memristors comprising Ag nanoparticles suspended in SiO_x dielectric matrix. We find out that by appropriate tuning of the temperature one cannot only reset the resistive memristor states, but also efficiently control the dynamical regimes of a memristive circuit. Our theoretical modeling well agreed with the results of experiments. Thus, our findings open another avenue for development and design of memristive elements for future electronics.

II. EXPERIMENTAL DETAILS

A schematic of the device structure is shown in Fig. 1(a). A platinum bottom electrode (30 nm) is deposited on a SiO_2/Si(100) wafer by magnetron sputtering using a thin-film deposition system from PVD Products Inc., with a fixed substrate to target distance of 15 cm. This is followed by co-sputtering Ag and SiO_x using 99.99% pure Ag and SiO_2 targets. The deposition is performed in Ar and O_2 atmosphere at room temperature. The growth pressure is maintained at 5 mTorr, and Ag and SiO_2 magnetron powers are set to 20 W (0.1 Å/*sec*) and 300 W (0.3 Å/*sec*), respectively. To optimize the Ag concentration and obtain a relatively low Ag deposition rate, the Ag target is masked using a rectangular stainless steel racetrack that covered approximately 85% of the target area. The top electrodes of Pt of thickness 20 nm [top part of Fig. 1(a)] are then sputter deposited through a shadow mask with circular apertures of 100 μm in diameter.

The *I-V* measurements are taken using a Keithley 4200 SCS with an attached Everbeing probe stage. Figure 1(b) presents a typical dependence of the absolute values of the current through the memristor on the applied voltage for positive (red) and negative (black) voltage cycles. Both graphs evidence clear hysteretic behavior once the voltage magnitude first increases and then decreases, thus evidencing a memristive properties of the device.

X-ray photoelectron spectroscopy (XPS) at the Ag 3*d* and Si 2*p* levels is used to verify the silver concentration. XPS is performed on a Thermo K-Alpha using an Al Kα monochromated (1486.6 eV) source with an overall energy resolution of 350 meV. Area mapping and line scans with a resolution of 100 μm are carried out in each corner of the sample and in the middle to check for homogeneity. For each location a survey is collected to preview the elements on the immediate surface, subsequent high-resolution scans are then performed on the elements of interest before fitting their peaks to identify elemental state. All scans are charge corrected to adventitious C1s (C-C, C-H) peak at 284.8 eV. The recorded XPS curves for the samples at different sites are shown in Fig. S1 and Table S1 within the Supplemental Material [24]. TEM specimens are prepared using the FEI Nova 600 nanoLab focused ion beam (FIB) and scanning electron microscope. A carbon layer is deposited on the film surface followed by a standard Pt deposition in the FIB as surface protection layers to preserve the outermost structure of the film. In addition, the carbon layer provides a gap between the FIB deposited Pt and the sputtered Pt top electrode to ensure accurate measurement of layer thickness and chemical analysis.

The TEM lamella had a thickness of approximately 100 ± 20 nm for energy dispersive x-ray spectroscopy (EDS) and the tapered edge of 30 nm for high-resolution imaging. TEM imaging and chemical analysis are performed using a FEI Tecnai F20 field-emission gun-scanning transmission electron microscope (FEGSTEM) equipped with a high-angle annular-dark-field detector

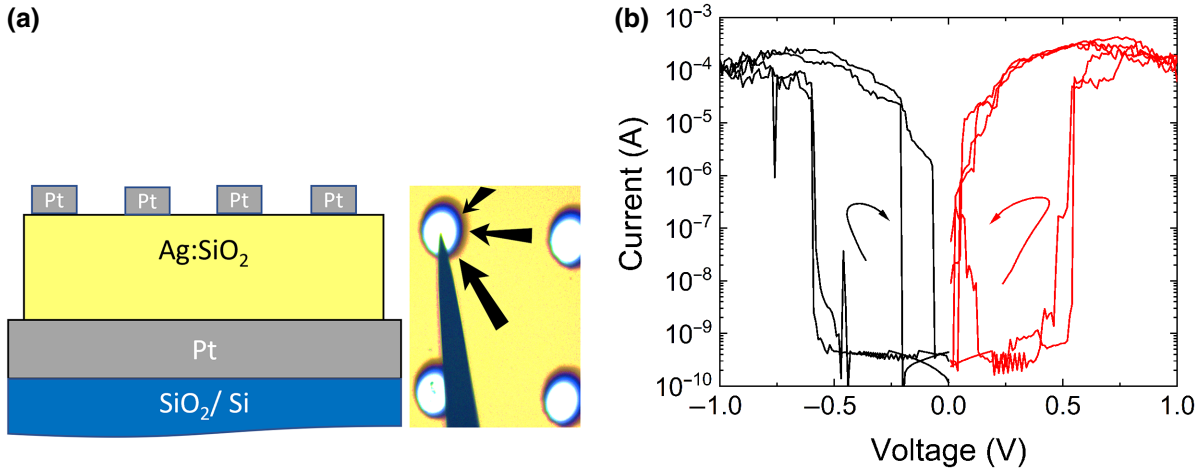

FIG. 1. (a) A side view schematic of a diffusive memristor device, Si/SiO_2/Pt(30 nm)/Ag:SiO_x(100 nm)/Pt(20 nm), and a top view photograph of the top Pt electrodes (100 μm in diameter) with a probe tip placed for *I-V* measurements. Black arrows show possible diffusion directions of NPs to the space under the top electrode (see Sec. IV A). (b) Typical *I-V* characteristics of a device measured in both positive (red line) and negative (black line) voltage cycles. The arrows indicate the direction of the change in device resistance.

(HAADF) and Oxford Instruments X-Max 80 windowless x-ray detector for EDS.

III. THEORETICAL MODEL

To qualitatively describe the resistive switching in a diffusive memristor we utilize a modified phenomenological model that previously explained the experimental findings in Refs. [12,13,25–27]. The main dynamical equation describes one-dimensional motion of a silver NP under the influence of electric field and thermal noise:

$$\dot{x} = -U'(x) + V/2 + \sqrt{T}\xi(t), \tag{1}$$

where an effective potential $U(x)$ accounts for the interaction of NP with various inhomogeneities and other NPs, as well as with various electrochemical potentials. We introduce notations V, T, and $\xi(t)$ representing voltage applied to the memristor terminals, nanoparticle temperature, and zero-mean δ-correlated white Gaussian noise ($\langle\xi\rangle = 0$, $\langle\xi(0)\xi(t)\rangle = \delta(t)$), respectively. Silver NPs are neutral, but can accumulate induced charge in the presence of voltage [28]. Time and coordinate derivatives are denoted by $\dot{x} \equiv dx/dt$ and $U' \equiv \partial U/\partial x$, respectively. The position of the nanoparticle defines the resistance of the device, which is modeled as $R(x) = \cosh(x/\lambda)$ with all resistances normalized by the lowest resistance R_0 of the memristor. This approximation implies exponential electron tunneling through the particle between tips of the almost formed CF, where λ is the tunneling length [25]. Here, instead of modeling many diffusing NPs and estimating the device resistance by considering many competing paths connecting the top and the bottom memristor electrodes through NPs, we assume that the resistance of the modeled memristor is actually determined by a bottleneck of size L linking two low-resistance clusters (see, e.g., Ref. [29]). In this case, x can be interpreted as a position of the single NP inside the bottleneck. Under these circumstances, the shape of $U(x)$ can be hardly evaluated from the microscopic calculation and may be influenced by the distribution of particles around the bottleneck, which in turn depends on many factors including the bath temperature T_0. Here, we examine several potentials and concluded that the main features of the memristor switching are robust against details of the potential, which can be chosen phenomenologically from TEM image analysis and I-V measurements on the device. Note that Eq. (1) is dimensionless, which means that time is normalized by $t_{\text{norm}} = \eta L^2/\Delta U$ with the viscosity η of Ag clusters in SiO_2 matrix and the depth ΔU of the potential well corresponding to LRS of the memristor [Fig. 2(a)]; the voltage is normalized by $V_{\text{norm}} = 2\Delta U/q_0$, where q_0 is the aforementioned induced Ag cluster charge; and the temperature is normalized by $T_{\text{norm}} = \Delta U/2k_B$ with the Boltzmann constant k_B.

In contrast to the previous works, here we use a double-well potential [Fig. 2(a)] to reflect the observation that the device can be steady both in HRS and LRS. Within the framework of our model, the position of the nanoparticle in the vicinity of $x = -1$ corresponds to HRS of the device, while the one in the vicinity of $x = 0$ defines LRS.

The nanoparticle temperature T in Eq. (1) is a dynamical variable depending on V and $R(x)$, obeying the equation

$$\dot{T} = \frac{V^2}{C_h R(x)} - k(T - T_0), \tag{2}$$

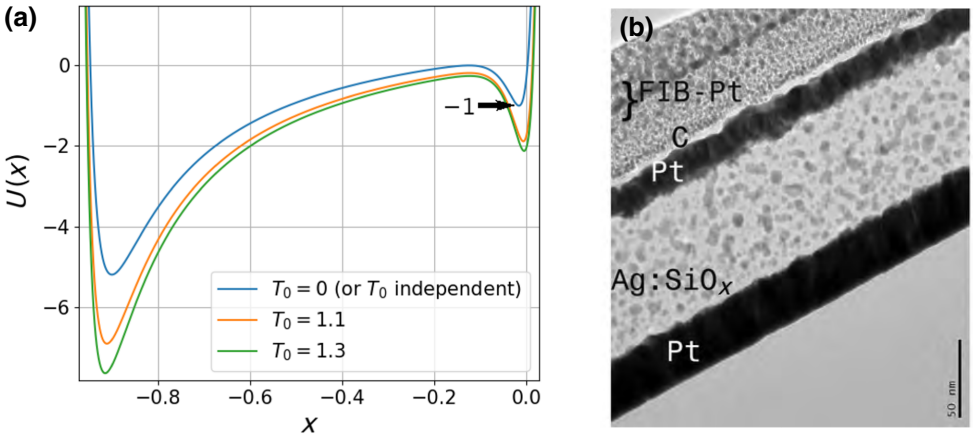

FIG. 2. (a) Normalized potential energy profile of a single Ag nanoparticle traveling between two shoulders of almost completed CF (the tip of the left shoulder has a coordinate $x = -1$, while the tip of the right one corresponds to $x = 1$). When NP is located near $x = -1$, the resistance of the memristor is high (HRS), while when the particle is near $x = 1$, the memristor is in LRS. We consider two possibilities: (i) temperature-independent case, in which $U(x)$ is only represented by the blue curve; (ii) temperature-dependent case, in which the potential is modified with the increasing temperature (in this case, the potential shape at $T_0 = 0$ fully coincides with the temperature-independent one). The normalization is done such that the local minimum near $x = 0$ is equal to minus one at $T_0 = 0$. (b) Cross-section TEM image of an as-grown sample. Darker Ag nanoparticles can be seen uniformly distributed in the SiO_x matrix. A thin white layer is carbon grown between two Pt layers.

where C_h and k denote the heat capacity of the device and heat transfer coefficient, respectively. Equation (2) reflects the famous Newton cooling law describing heat dynamics due to the Joule heating and heat transfer to the substrate [30]. As shown in Refs. [26,27], the interplay between heat, Ag-cluster diffusion, and electron transport can result in a variety of dynamical features for a diffusive memristor.

Noise is multiplicative in the system of Eqs. (1) and (2), but there is no Ito-Stratonovich dilemma [31] as $\sqrt{T}$ [multiplier of $\xi(t)$] does not depend on x explicitly.

We select dimensionless parameter values as well as the shape and temperature dependence of the potential in order to provide a qualitative agreement between the theory and experiment (see the exact expressions in the Supplemental Material [24]). Also, further justification behind the model is provided in Appendix B. A question may arise regarding the variation of the temperature during the switching of our diffusive memristor from HRS to LRS. We estimate the temperature variation by solving Eq. (1) (see Fig. S4 within the Supplemental Material [24]). It is seen that the temperature change between such a transition is relatively low.

IV. RESULTS AND DISCUSSION

A. Memristor reset

Figure 2(b) presents a bright-field TEM image of the cross section of an as-grown device prior to applying any voltage cycles to the Pt electrodes. Silver nanoparticles (dark gray dots) can be observed rather uniformly

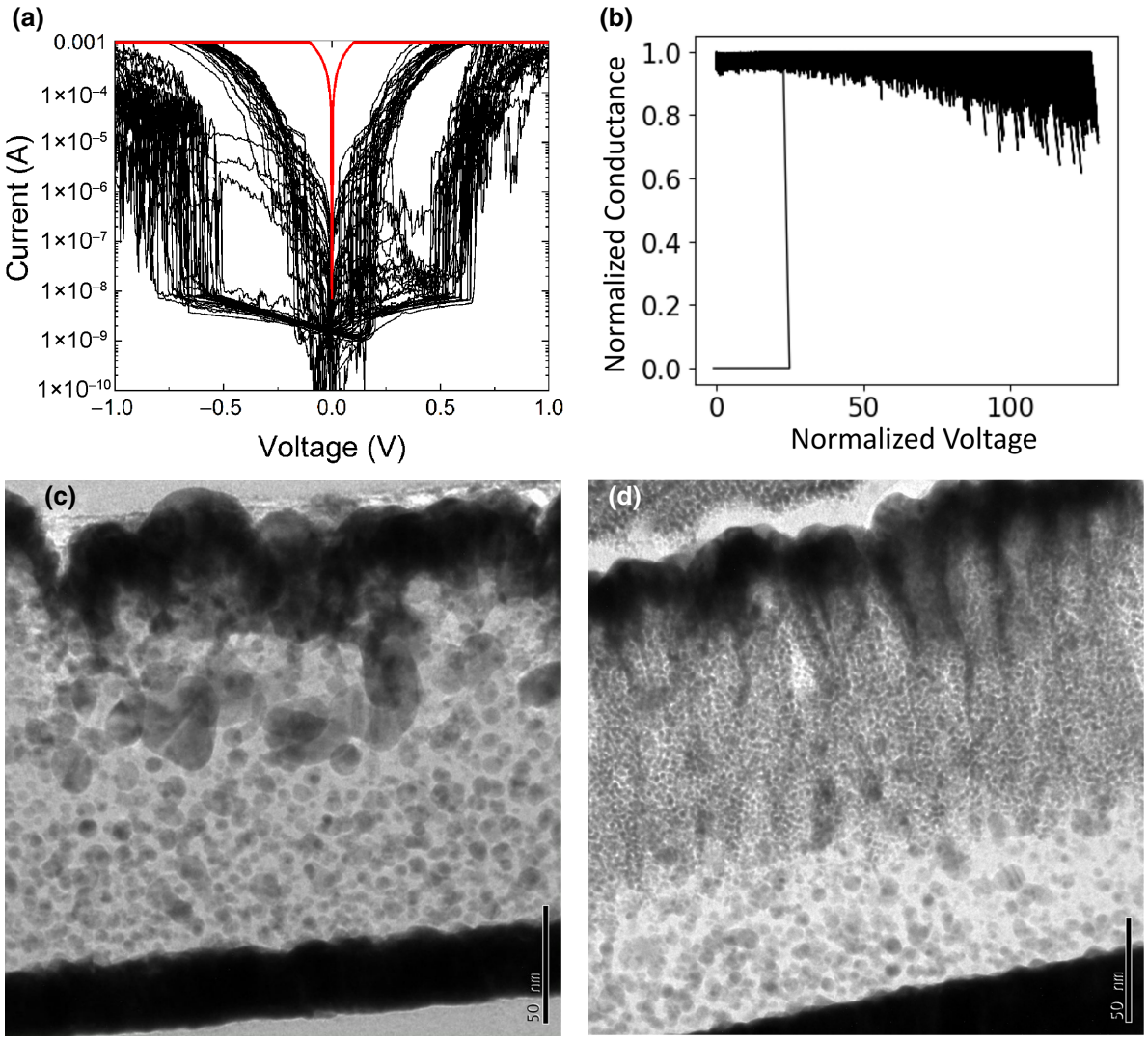

FIG. 3. (a) Experimental I-V curve. Initial I-V switching (black lines) transforms into a permanent LRS (red line) after multiple voltage cycles. (b) Simulated behavior of the conductance $[1/R(x)]$ of a diffusive memristor in response to external voltage. The normalization constants are discussed in the Supplemental Material [24]. When the NP is trapped in the metallic state at position $x = 0$ [see Fig. 2(a)], the device conductance stays high ($T_0 = 0.1$). (c) Cross-section TEM images of samples at room temperature when in permanent LRS, and (d) after the substrate temperature is raised to 50 °C to break the Ag clusters at the top electrode site.

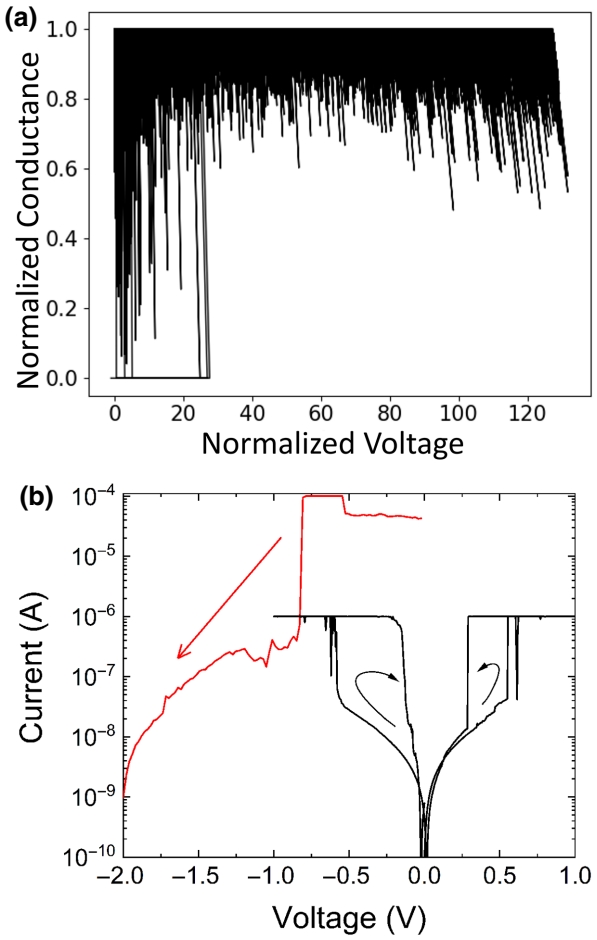

FIG. 4. (a) Simulated memristor conductance at raised device temperature ($T_0 = 1.5$). A volatile switching between LRS and HRS is observed at $V \approx 30$ and at $V \approx 0$ [cf. Fig. 2(a)]. (b) Experimental I-V curves demonstrating the first electroforming sweep assisted by external heat (red line) by placing the sample on a temperature controlled stage at 50 °C.

distributed in the SiO_x dielectric matrix sandwiched between the top and bottom Pt electrodes. A typical I-V hysteresis during application of an external voltage to the top and bottom Pt electrodes at the room temperature as previously shown in Fig. 1(b) demonstrated a volatile switching behavior for both voltage polarities.

After a number of voltage cycles where the device showed distinct I-V hysteresis switching [Fig. 3(a), black lines], the memristor switched into permanent LRS. Subsequent voltage cycles, either positive or negative, did not reset the device to HRS [see red curves in Figs. 3(a), which do not demonstrate hysteresis anymore]. Analysis of TEM images [Fig. 3(c)] revealed that this state of the device is typically characterized by the presence of relatively large silver clusters near the top electrode and densely packed Ag NPs near the bottom one. Movie S1 within the Supplemental Material, depicting the motion of Ag nanoparticles in the dielectric matrix, is provided [24]. To understand such behavior, let us consider qualitatively the mechanisms behind the filament formation in the device. When an external voltage is applied to the memristor terminals, the charged NPs start to drift towards the bottom negative electrode [28,32]. As such a field-dependent drift takes place only below the top positive Pt electrode, the neighboring neutral Ag nanoparticles diffuse to the region of the lower Ag concentration. Comparing Figs. 2(b) and 3(c), one can notice that the Ag concentration definitely increases between the electrodes. Due to the lack of an Ag reservoir layer to compensate for the depleting of Ag density at the top (as in previous works [25,33,34]), the only source of NPs is the surrounding space of the top electrode, which can be recognized as a small spot in Fig. 1(a). So, when electrical field is turned on, the formation process of CF starts over under the top positive electrode to create a conductive bridge, which switches the memristor to LRS.

When the value of the applied voltage decreases, the CF breaks due to thermal fluctuations and diffusion processes, so the memristor switches back to HRS with incomplete and partial CFs. Similar mechanisms are realized also for opposite voltage polarity.

Multiple repeating cycles of formation and rupturing of CFs, which are highly stochastic processes, can eventually lead to development of an asymmetry in the particle distribution. In our case, it manifests itself in asymmetric clustering near the top and bottom electrodes. Namely, while the vicinity of the top electrode is occupied by rather large clusters of Ag nanoparticles (spatial dark volumes), the bottom electrode accumulates much lesser fraction of the NP clusters. Such asymmetry could be explained by the difference in concentration of the pinning sites on the top and bottom electrodes, which is caused due to the higher roughness of the top electrode [18,28,35], as evident from the TEM images [see Figs. 2(b), 3(c) and 3(d)]. Appearance of such pinning centers, which attract and trap nanoparticles, is conditioned by a number of factors including the surface tension, cohesion forces, and the Rayleigh instability [36]. The huge NP clusters at the top serve as an extension of the top electrode making the switching layer effectively thinner, i.e., comparable in size with a few NPs. Thus, the short-circuiting CF formation may occur with higher probability.

To get a deeper insight into the mechanisms of setting the memristor to the permanent LRS we employ the model (1) and (2). We consider both temperature-independent $U(x)$ (used for Figs. 3 and 4) and temperature-dependent $U(x, T_0)$ (used for Figs. 5 and 6). In Fig. 2(a), the temperature-independent potential is the one corresponding to $T_0 = 0$. Here, we simplify the analysis by considering the potential shape suitable for positive applied voltages only. Appendix B describes how it can be extended to negative voltages. The attractive pinning centers near the top electrode get reflected by the left well of $U(x)$. LRS corresponds to the situation when NP arrives to the

vicinity of $x = 0$, where $R(x)$ reaches its lowest value. As the device can get stuck in LRS, we assume that there is a potential minimum near $x = 0$.

At T_0=0.1 [blue in Fig. 2(a), temperature-independent case], the model reproduced the experimental situation as illustrated by the conductance (inverse resistance) curve in Fig. 3(b), namely, the system starts from HRS and then eventually switches to LRS as the applied voltage increases. Then, any further increases and decreases of the voltage do not produce any hysteresis in the conductance curve, and the corresponding curves, albeit becoming noisy, demonstrate rather the same path. Such a behavior of the model suggests that NP is trapped in the potential well corresponding to LRS. We hypothesize that additional energy stimulating particles escape from the potential minimum could be pumped in by increasing the temperature of the device T_0. At least, in the corresponding TEM image [Fig. 3(d)], which is taken for the heated sample, one can observe that the mentioned top silver clusters have been broken into smaller ones. In other words, the increased temperature improved the agility of NPs.

The hypothesis is easily verified in simulations. Figure 4(a) presents resetting of the hysteretic behavior as T_0 is set to 1.5. At this temperature, changing of voltage returned the system to HRS and restored a hysteresis in the I-V curves.

To test the hypothesis in practice, a sample in the permanent LRS is placed on a temperature-controlled sample stage, and the stage temperature is gradually increased to 50 °C. A negative voltage sweep is first applied followed by a complete positive and negative voltage cycle. The negative voltage sweep (electroforming) assisted by the external thermal contribution pushed the filaments from LRS to HRS. When the voltage was cycled at low temperature again, the device demonstrated I-V hysteresis [characteristic Fig. 4(b)]. During electroforming to negative voltages at 50 °C, the device current dropped to low values (shown by red line), and when a subsequent full voltage sweep is performed, the memristor starts from HRS and shows a hysteresis current voltage characteristic (shown by black lines, with the arrow representing the direction of resistance switching).

Besides broken top silver clusters, the net Ag% at the surface is also shown to increase (see Table S1 within the Supplemental Material [24]), and there is a shift in the Ag 3d peaks. The shift in the metallic Ag peaks can be correlated with the size difference of NPs [37].

It is worthwhile to note, a further theoretical analysis shows that decreasing the thermal conductivity or the specific heat capacity of the memristor could also reset the permanent LRS. For example, the conductance behavior is modeled for different values of the specific heat capacity C_h and the heat-transfer coefficient k using Eq. (2), and shown in Fig. S2 within the Supplemental Material [24]. However, implementation of such control requires complex design of the device, which is beyond the scope of this paper.

To understand the reason why increasing T_0 or decreasing C_h or k allows for resetting the device, one can analyze switching conditions. To switch to LRS the system should escape from the potential well near $x = -1$ corresponding to HRS. When voltage increases (assuming V being positive), as soon as the force $V/2$ exceeds the maximum restoring force $V_c/2 = \max_{-1<x<0} |\partial U/\partial x|$, the NP diffuses to $x = 0$ (LRS). When voltage decreases, the particle remains trapped at the well $x = 0$, and only temperature fluctuations can push the particle to hop over the barrier back to HRS. Therefore, the bath temperature T_0 should be about the barrier height, which is $T_0 \approx 1$ in the chosen dimensionless units.

B. Dependence of switching threshold upon temperature

To further investigate the temperature influence, we vary T_0 in a range between 25 °C and 200 °C. For the experiment, we use a fresh sample, which did not demonstrate switching into permanent LRS yet. External voltage is applied between 0 to 3 V with a sweep rate of 50 mV/s and corresponding I-V characteristic is recorded for each hold temperature. Figure 5(a) represents nine I-V cycles at different hold temperature. Remarkably, as T_0 varies, the voltage thresholds for switching the memristor to HRS and LRS change in a counterintuitive way, namely, they increase with temperature, i.e., it becomes harder to switch the memristor, when temperature noise is higher. Figure 5(b) presents how the averaged over five cycles threshold voltage for switching to LRS (black) and to HRS (red) change with variation of the device temperature. While the averaged voltage to switch to LRS significantly grows with increase of T_0, the threshold voltage for setting the memristor to the HRS weakly changes (if it changes at all).

In Appendix A we argue that such behavior is possible because of the multiwell nature of the real (unknown) potential, which we approximate by the $U(x)$ function. Indeed, a particle can be sent by intensive fluctuations to a narrow deep well, which is hard to escape from if the external voltage is not high enough.

We assert that the unexpected increase of the switching threshold can be effectively modeled by the temperature-dependent potential $U(x, T_0)$ with deeper wells at higher T_0, see Fig. 2(a). Our theoretical model with the potential depending on T_0 demonstrates a good qualitative agreement with the results of experimental measurements. For example, Fig. 5(a) presents the hysteretic behavior of the I-V curve for $T_0 = 2.3$. When scaled, the model data fits the experimental points very well. The calculated dependencies of the voltage thresholds for switching to LRS and

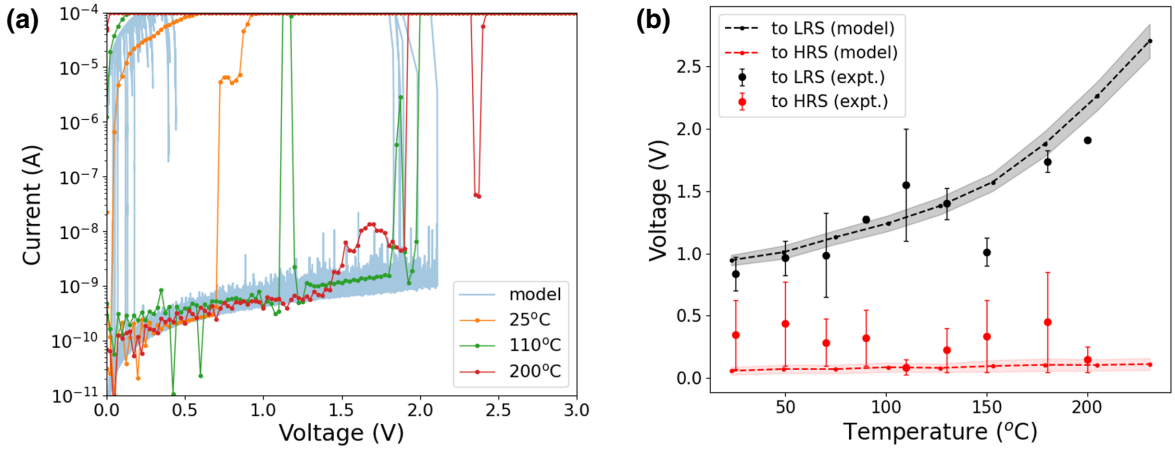

FIG. 5. (a) Experimental I-V loops measured at different hold temperatures showing distinct threshold voltage for HRS to LRS transition. In the background there is the simulated I-V curve at $T_0 = 2.3$ (scaled to fit the experimental one) for the temperature-dependent potential shown in Fig. 2(a). (b) Experimental and simulated variation of switching voltage for HRS to LRS (black) and LRS to HRS (red) switch. Model curves are scaled to fit the experimental ones (see details in the text). "Shade" around a model curve reflects its standard deviation.

HRS [Fig. 5(b)] reproduce well the trends of the experimentally measured dependencies [cf. Fig. 4(b)]. For scaling the simulated curves we perform linear fitting (see Supplemental Material [24]) between real and dimensionless parameters (I, V, and T).

C. Temperature effect on a spiking circuit

One of the most promising applications of diffusive memristors is using them as a core element in spiking and switching neuromorphic devices [7–9]. Therefore, next we investigate how the change of memristor temperature T_0 affects the spiking regimes of an artificial neuron, whose principal electrical scheme is depicted in Fig. 6(a). Here, R_{ext} is a load resistor and C_{ext} describes internal or/and externally added capacitance of the memristor. According to Kirchhoff's law, in this case, the voltage drop over the memristor, V, obeys the equation

$$\tau \dot{V} = V_{\text{ext}} - \left(1 + \frac{R_{\text{ext}}}{R(x)}\right) V, \tag{3}$$

where V_{ext} is the externally applied constant voltage and $\tau = R_{\text{ext}} C_{\text{ext}}$. Numerical simulation of Eqs. (1)–(3) reveals that change of T_0 can regulate the residual time the system spends in HRS and LRS during spiking cycles. Figures 6(b) and 6(c) present the time realization of V for $T_0 = 1.1$ and $T_0 = 2.1$, respectively, at the same $V_{\text{ext}} = 37$. It is clearly seen that for $T_0 = 1.1$ [Fig. 6(b)], the state where the memristor spends more time corresponds to LRS (low voltage background), and the spike manifests itself as a sharp surge of V towards its higher values followed by a swift return to LRS. An opposite picture is observed for larger temperature $T_0 = 2.1$ [Fig. 6(c)], where the V spikes are associated with sharp drop of the voltage over the memristor followed by the return to higher voltage values related to HRS. We note that changing the state, where the system spends more time, from LRS to HRS with variation of T_0 relates to changing the stability properties of the equilibrium points of the dynamical system (1)–(3), whose analysis is reported elsewhere.

To check our numerical findings in experiment, we connect an external resistor R_{ext} in series to the memristor discussed in Sec. IV A, assuming the presence of an internal memristor capacitance. The voltage across the device is measured using an oscilloscope at different voltage amplitudes. The value of R_{ext} is fixed at 55 kΩ, which produced spiking in a wide range of voltages. The dynamics of the voltage drop over the memristor for two different temperatures is illustrated by Figs. 6(d) and 6(e).

It is worthwhile to emphasize that the device under investigation can generate spikes with constant voltage (V_{ext}) applied, which is not the case in some other studies (e.g., Refs. [23,38]), where spikes follow some periodic pulsation of an external source. Spiking rates of our diffusive memristors are high enough to consider them as base elements for neuromorphic computational devices. In Fig. 6(d) the rate can be estimated as high as hundreds of spikes per second, which is much faster than firing of living neurons (about ten spikes per second [39]).

For the room temperature and $V_{\text{ext}} = 0.6$ V, the circuit demonstrated spiking [Fig. 6(d)] similar to one presented in Fig. 6(b), i.e., where spikes are associated with sharp increase of V. However, as the temperature is set at 200 °C, the spiking regime occurred for higher voltages. Moreover, as Fig. 6(e) evidences for $V_{\text{ext}} = 1$ V, the spiking is inverted similarly to our numerical simulations [see Fig. 6(c)]. The possibility to control time the system spends in HRS or LRS by setting the appropriate temperature

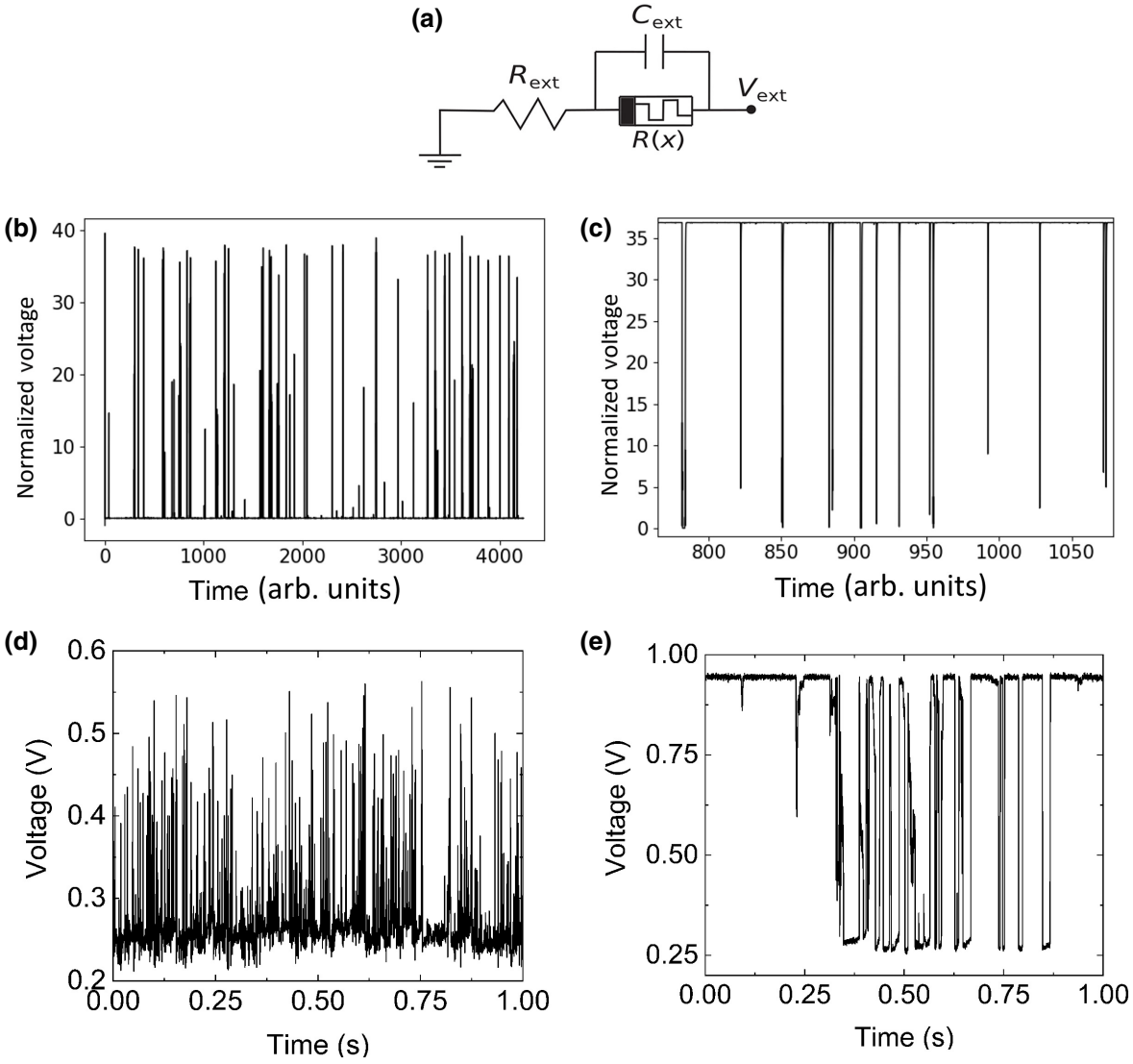

FIG. 6. (a) Artificial neuron circuit. (b) Simulated bottom-up voltage spikes of (a) at low temperature ($T_0 = 1.1$) for the parameters and potential as in Fig. 5. The voltage is mainly at the low level, which corresponds to LRS of the memristor. (c) Simulated top-down voltage spikes at higher temperature ($T_0 = 2.1$), that is, the memristor is mostly in HRS, for the parameters and potential as in Fig. 5. (d) Experimental voltage spikes for the diffusive memristor, when the SiO_x matrix is set to room temperature and (e) the temperature of 200 °C.

offers another degree of freedom in controlling artificial neuron dynamics.

D. Device structural damage at higher temperatures

Having proposed temperature as a mean to control the functioning of the diffusive memristors, it is useful to find a proper range of the temperature tuning. In our experiments we observe that a long-time exposure of diffusive memristors to high temperature can cause a permanent structural damage. The relevant TEM and SEM images of a prolonged heat-treated sample are taken and are shown in Fig. S3 within the Supplemental Material [24]. It is revealed that with extended heating time the nanoparticles coalesce together and surface out of the sample. This property is very similar to Ag sintering properties and can be attributed to Ostwald ripening of Ag nanoparticles [32,40,41].

V. SUMMARY AND CONCLUSIONS

In this work we experimentally and theoretically demonstrate that tuning of the temperature of the dielectric matrix of a diffusive memristor can be used as an efficient tool to control hysteretic properties of the device and spiking regimes in the memristor-based artificial neuron circuit. In particular, we show that appropriate temperature tuning can restore the hysteresis in I-V characteristics of a

diffusive memristor, which gets stuck in LRS after a number of operating cycles. This provides a way to increasing the life time or endurance of the diffusive memristor devices. On the other hand, the temperature reset offers an approach to switch between hysteretic and nonhysteretic behavior of the memristor resistance.

Another finding shows the possibility to employ the dielectric matrix temperature in order to regulate the voltage thresholds for switching between HRS and LRS. We find out that while the voltage threshold for switching to LRS strongly depends on the temperature, the threshold for switching to HRS is less sensitive to the temperature change. These results suggest using the temperature for tuning the hysteresis width, which is beneficial both for resistive switches and for spiking generating circuits, since the hysteresis properties also define the negative differential resistance of memristive devices.

We propose a theoretical model that qualitatively describes the electric properties of the experimental devices. The model is able to predict a possibility for the temperature reset from a permanent LRS, later confirmed in experiment. Analysis of the dynamics of the proposed model for varying device temperature T_0 allows us to reveal phenomena associated with the change of residual time the system spends in LRS and HRS, which are also verified experimentally.

Our results thus open another direction in the efficient control of devices and circuits involving the diffusive memristors, which is key for design and development of future neuromorphic computing and AI systems.

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APPENDIX A

The temperature-dependent potential $U(x, T_0)$ can be justified as follows: a complex multiparticle system has been reported [28,42] to consist of multiple wells. Our guess is there are additional deep wells near $x = -1$ and $x = 0$ in our model (see an example in Fig. 7). At moderate temperatures and external voltages the particle will move between the wells 2 and 3. However, at higher T_0 the particle can move to a deeper well 1 due to more intense fluctuations. Hence, the switching voltage to remove the particle from the well 1 will be higher.

For the presented case of the three-well potential, we measure the following values in simulations:

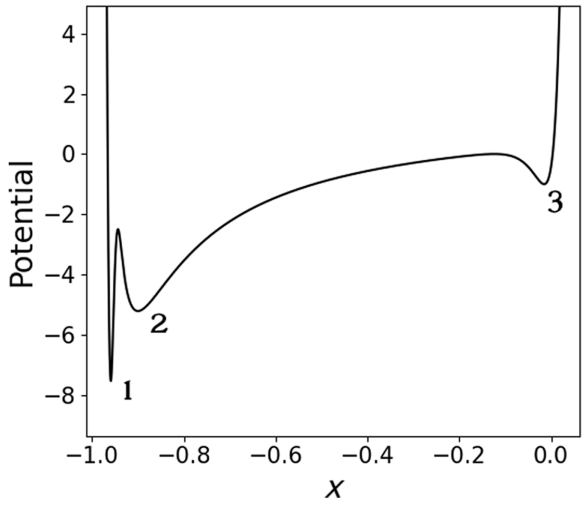

FIG. 7. Normalized model potential to explain the temperature dependence as a function of the nanoparticle position (x). Due to higher temperature T_0 a model particle can occur in the left-most well 1, so, the higher external voltage will be necessary to move it out of there.

(a) at $T_0 = 0.9$ the average switching threshold is $V_{\text{th}} = 16.2$,

(b) at $T_0 = 1.9$ the average switching threshold is $V_{\text{th}} = 25.6$,

i.e., the higher temperature, the higher the switching threshold.

It total, we assume that there are many more similar narrow wells on the left and on the right of $U(x)$, which explain the gradual temperature dependency of the switching threshold voltage in Figs. 5(c) and 5(d).

It is also noteworthy that in Fig. 5(a) the experimental points corresponding to HRS (low current) lie on several levels. A similar picture is observable at the top (high current) except that the current limiter compresses the distinctive levels into the single one for higher voltages. This is exactly what happens in simulations, if there are many narrow wells in the potential $U(x)$.

APPENDIX B

A previous study [12] demonstrated that electrical current through the diffusive memristor is determined by a sequence of charges tunneling between moving NPs and CFs formed near the memristor electrodes, see Figs. 8(a) and 8(b). Another research [29] into the same phenomena suggested that in most cases it is sufficient to consider only one NP in the gap between CFs. In this case, local temperature $T(t)$, governed by Joule heating law, controls diffusion of NP, and the dynamics of NP could be considered as motion in a potential field $U(x)$, which has a local minimum near the tip of CF. The origin of this

minimum reflects a van der Waals character of the interaction of the neutral NPs. If energy of the particle exceeds the potential barrier due to thermal or/and electric field activation, then NP starts to wander between CFs. The applied voltage V stimulates tunneling of a charge from the filament to NP. As a result, NP detached from CF gets ionized and therefore subjected to the electromotive force proportional to V. Thus, the momentum rate of NP within the potential $U(x)$ has a diffusion component proportional to $\sqrt{T}$ and a drift component proportional to V. In Fig. 8(a) one can see the illustration of such a picture with electrical field, **E**, directed from left to right. The particle, bearing induced positive charge, detaches from the left CF and drifts towards the right one. The potential barrier near $x = 0$ is introduced phenomenologically to accord with the studies [27,28] where preventing the model particle from moving further provided good qualitative agreement between simulations and experiments. This key idea is used successfully in the presented study as well. The charge-transport mechanisms assume realization of LRS when NP is in the middle of the gap between CFs, since it maximizes the tunneling rate.

In the case of the opposite direction of the electrical field, one can assume that NP detaches from the right CF, see Fig. 8(b). This can be accommodated in the model, if we assume that either charge of the particle changes sign or the potential seen by a particle is inverted. Indeed, in the former case, we can expect that the induced charge is proportional to voltage ($q = CV$) at low voltages. With increasing voltage the accumulated charge should saturate due to strong repulsion of electrons and holes. The simplest way to reflect these processes is to use the equation $q = q_{\max} \times \tanh(\alpha V)$, with constant $q_{\max}$ and $\alpha = C/q_{\max}$ [Fig. 8(c)]. For our dimensionless Eq. (1) we just write the second right-hand side term as $\tanh(V) \times V/2$ to obtain the double-sided hysteresis loop shown in Fig. 8(d).

The second option is to use two noninteracting particles on each side of the gap. The left one will be moving within the original potential $U(x)$ as the detached particle in Fig. 8(a). This will describe the resistance switching in the case of the left-to-right direction of the electric field [positive V in Eq. (1)]. The second NP, on the right-hand side, will be moving within the reflected potential $U(-x)$ as depicted in Fig. 8(b). That NP will get stuck near $x = 1$, when V is positive, and will describe the system when V is negative. Such dynamics allows explanation of the symmetric I-V loops as well.

To elaborate on the physical origin of the potential barrier at $x = 0$, we can think of tunneling charge through the nanoparticle. Tunneling rate should be a reciprocal of $t_L + t_R$, where t_L is the tunneling time from NP to the left CF shoulder, and t_R is the tunneling time from the right CF shoulder to NP (assuming $V > 0$). If $x < 0$, then $t_L < t_R$, so NP is positive most of the time even though negative

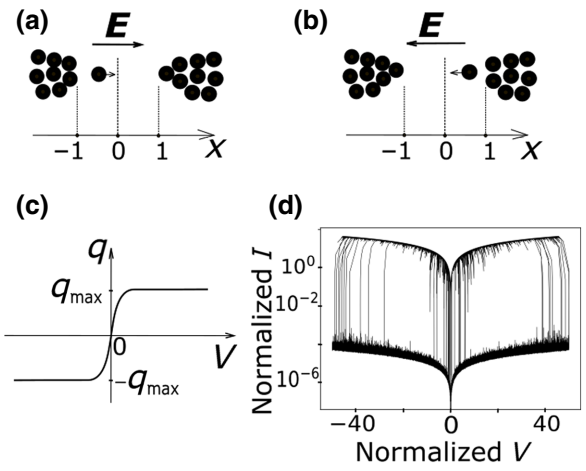

FIG. 8. Model explanation. (a) Single NP in a gap of CF in case of left-to-right electrical field **E** direction [the potential $U(x)$ from Fig. 2(a) corresponds to this situation]; (b) single NP in the gap in case of right-to-left **E** direction [the corresponding potential will be $U(-x)$ in this case]; (c) suggested $q(V)$ dependence to model the double-sided hysteresis loop without changing $U(x)$; (d) double-sided hysteresis loop obtained with the suggested $q(V)$.

electrons jump on it at random instants of time. It is positive, because the incoming rate of electrons is lower than the outgoing rate. However, if $x > 0$, then $t_L > t_R$ on average, so NP can become neutral or even negative, which forces it to move in the direction opposite to **E**. Thus, $x = 0$ will work effectively as a reflecting boundary.

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