# Ultrasensitive Strain Sensor Based on a Tunnel Junction with an AlN/GaN Core-Shell Nanowire

Gongwei Hu<sup>®</sup>,<sup>1,\*</sup> Fobao Huang,<sup>2</sup> and Jun-Feng Liu<sup>1,†</sup>

<sup>1</sup>School of Physics and Materials Science, Guangzhou University, Guangzhou 510006, China <sup>2</sup>School of Microelectronics, Northwestern Polytechnical University, Xi'an 710072, China

(Received 1 September 2022; revised 26 November 2022; accepted 3 January 2023; published 25 January 2023)

Piezotronic transistor operating in the quantum tunneling regime has recently roused wide interest for developing ultrasensitive strain sensing with applications in wearable electronics and human-machine interfaces. However, the lack of a strict theoretical demonstration from a quantum perspective renders the development of such an emerging area particularly slow due to their complex fabrication process and vulnerable experimental interference. Here, by combining third-dimensional self-consistent calculation with a nonequilibrium Green's function framework, we study the intrinsic device properties of piezotronic tunneling transistor (PTT) based on AlN/GaN core-shell nanowire. The results show that strain-induced piezoelectric polarization can remarkably tune tunneling barrier height and width, both of which are increased by tensile strain and decreased by compressive strain. At a moderate strain amplitude of 1.0% and bias of 2.0 V, the strain-induced change in effective barrier height and width can reach as high as 0.5 eV and 4.0 nm, respectively. This remarkable tunability in the barrier allows for an ultrahigh on/off current ratio  $10^{17}$ , and giant gauge factor  $1.2 \times 10^8$  in current and  $1.1 \times 10^{13}$  in resistance. The performance can be further optimized by properly tailoring device architectures, including insulator thickness, nanowire length, or core-shell size. Our demonstration of the PTT with combined quantum tunneling and piezotronic effect opens a window for designing highly sensitive, large on/off ratio and low-power strain sensing.

DOI: 10.1103/PhysRevApplied.19.014066

## I. INTRODUCTION

The tunneling transistors (TTs) have been regarded as one of the most promising candidates for developing postcomplementary metal-oxide semiconductor (post-CMOS) technology in ultralow power-integrated circuit applications [1–3]. The working mechanism of the TT is based on a fascinating physical phenomenon that the charge carriers have the capability to penetrate an energy barrier. Therefore, the operation of the TT relies on the tunability of tunneling barrier height and width [4], and both of which are inherently suitable for the electrical modulation. In this regard, various TT's derivatives have been demonstrated, including molecular TT [5], dopingless TT [6], reconfigurable TT [7], vertical TT [8], energy-efficient TT [9], and resonant TT [10].

Mechanical stimuli that are ubiquitous and abundant in environment, are an alternative way to tune quantum tunneling by virtue of piezoresistive effect where straininduced deformation potential modifies electronic band structure to realize a macroscopically electrical regulation [11–15]. This motivates a wide interest for applications in strain sensing with high sensitivity and low power consumption. However, in terms of a quantum perspective, a deformation potential is a pure perturbation quantity compared with an intrinsic barrier formed by material features [16], including the electron effective mass, lattice constant, and band gap. For example, the confined electrons would feel a high barrier at the interface if the hosting material has a large effective mass such that the sub-band level is lowered down to the bottom of the potential well. The mismatch of lattice constants in heterostructure can cause a strain at the interface to induce a deformation potential modifying the band gap as well as the barrier height [17]. A considerable variation in tunneling barrier (or tunneling current), hence, requires the provided external mechanical strain large enough in order for sufficient device operation [11,12,15]. For instance, tensile stress of 500 MPa can only obtain a 4% enhancement in sourcedrain current in a double-gated silicon tunneling fieldeffect transistor [12]. Nevertheless, large strain inevitably brings in high density of defects and dislocations inside materials [18,19], leading to a tunneling device with high off current leakage and low on current due to brokengap band alignment [20,21]. Moreover, third-generation

<sup>\*</sup>gwhu@std.uestc.edu.cn

<sup>&</sup>lt;sup>†</sup>phjfliu@gzhu.edu.cn

semiconductor systems enduring a large strain remain technically challenged due to their large Young's modulus (ZnO  $\sim$  200 GPa, GaN  $\sim$  400 GPa, AlN  $\sim$  400 GPa) [22], which hampers their tunneling device applications. To address these issues, tunneling junctions modulated by strain-induced piezoelectric polarization have recently been proposed based on *p*-doped GaN heterostructures and n-doped ZnO nanowires [23-25]. Piezoelectric modulation inherently is a combination of electrical (piezoelectric potential) and mechanical (deformation potential) means, and thus can trigger a higher gauge factor in tunneling junction  $(7 \times 10^4 \text{ in MgO/ZnO [23]}, 2.6 \times 10^8)$ in Pt/Al<sub>2</sub>O<sub>3</sub>/p-GaN [24],  $4.8 \times 10^5$  in Ag/HfO<sub>2</sub>/n-ZnO [25]). However, the overestimated gauge factor due to nonideal experimental platforms [24], together with the difficulty in the growth of high-quality tunneling junction [23,25], requires a strict theoretical demonstration not only for an in-depth understanding of combined tunneling mechanism and piezoelectric modulation, but also for a guidance of next performance optimization.

In this work, we theoretically demonstrate a piezotronic tunneling transistor (PTT) based on AlN/GaN core-shell nanowire by a strict quantum transport simulation. A nonpiezoelectric insulator layer sandwiched between the source and core-shell nanowire is constructed as a high potential barrier to drive tunneling current. By regulating barrier height and width of the PTT, strain-induced interfacial polarization charges can effectively tune device performance. The results suggest that tensile strain significantly increases gauge factor in the current, and compressive strain raises gauge factor in the resistance. At a moderate strain amplitude 1.0%, the PTT exhibits giant gauge factor  $1.2 \times 10^8$  in current and  $1.1 \times 10^{13}$  in resistance, and ultrahigh *on/off* current ratio  $10^{17}$ . The performance can be further optimized by engineering device architectures including insulator thickness, nanowire length, or core-shell size.

# II. QUANTUM TRANSPORT IN AIN/GaN CORE-SHELL NANOWIRE

More recently, III-nitride core-shell nanowires have stimulated tremendous research interest in electronics and optoelectronics applications, such as high-efficiency lightemitting diodes [26,27], ultraviolet laser [28], and highmobility transistors [29]. In comparison with single-crystal bare nanowires, the core-shell structural nanowires support many favorable attributes in strain engineering [30], bandgap tunability [31], electron mobility [32], and structural diversity [33].

The basic configuration of our PTT consists of sourcedrain electrodes, AlN/GaN core-shell nanowire, and a nonpiezoelectric insulator layer sandwiched between the source and nanowire. A high potential barrier formed in insulator layer enables the electrons to tunnel instead of directly traveling. The tunneling current is controllable either by modifying barrier height or by altering barrier width, and both of them can be accommodated by strain-induced piezoelectric polarization. This is the case no matter there is or not a bias (see Appendix A). When a tensile strain is applied, positive piezoelectric polarization charges are induced at the interface between the insulator layer and AlN/GaN core-shell nanowire. These positive polarization charges attract the electrons tunneling



FIG. 1. Schematic diagrams of the PTT based on the AlN/GaN core-shell nanowire under (a) tensile strain and (b) compressive strain. The device structures are shown in the left and the conduction-band potential profiles are displayed in the right.

from the source to insulator-nanowire interface by reducing barrier height and width, as seen in Fig. 1(a). When a bias is supplied, these tunneled electrons start to flow and produce a larger tunneling current. By contrast, negative polarization charges induced by compressive strain will repel the electrons access to insulator-nanowire interface. In this case, the electron is difficult to tunnel due to the raised barrier height and width, leading to a low current, as shown in Fig. 1(b). It should be noted that although piezoelectric polarization charges also exist at the drain-nanowire interface, its impact on tunneling transport is negligible because they mainly affect drain-to-source tunnelling, which is much weaker than source-to-drain tunneling under a positive bias (we do not consider reverse bias).

The electronic properties in low-dimensional nanodevices can be captured by the Schrödinger equation  $H\Psi = E\Psi$  with Hamiltonian *H*, wave function  $\Psi$ , and energy level *E*. In AlN and GaN, their wide-gap feature allows for a parabolic effective-mass Hamiltonian for the electron, which is solved as

$$\begin{bmatrix} -\frac{\hbar^2}{2m_{xy}} \left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2}\right) - \frac{\hbar^2}{2m_z}\frac{\partial^2}{\partial z^2} + U(x, y, z) \end{bmatrix} \Psi(x, y, z)$$
  
=  $E\Psi(x, y, z),$  (1)

where  $\hbar$  is the reduced Planck constant,  $m_{xy}$  and  $m_z$  are the effective mass parallel and perpendicular to the *c* axis in wurtzite crystal, respectively. The conduction-band potential profile is given by  $U(x, y, z) = E_C(x, y, z) - qV(x, y, z)$  with offset energy  $E_C$ , electron charge *q*, and electrostatic potential *V*.

Three-dimensional (3D) Schrödinger Eq. (1) can be uncoupled into the case in two-dimensional (2D) crosssection plane and one-dimensional (1D) transport for wave function with form  $\Psi(x, y, z) = \sum_i \varphi_i(z)\psi_i(x, y; z)$  [34, 35], where  $\psi_i(x, y; z)$  is *i*th 2D sub-band wave function at each core-shell cross-section slice, and  $\varphi_i$  is its 1D transport wave function. In each cross-section slice, the 2D sub-band can be obtained as

$$\begin{bmatrix} -\frac{\hbar^2}{2m_{xy}} \left( \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} \right) + U(x,y;z) \end{bmatrix} \psi_i(x,y;z)$$
  
=  $E_i \psi_i(x,y;z),$  (2)

where  $E_i$  is *i*th 2D subband energy. In the uncoupled mode space [35], 1D transport is solved as  $(-(\hbar^2/2m_z)(\partial^2/\partial z^2) + E_i)\varphi_i(x,y;z) = E\varphi_i(x,y;z)$  with open boundary condition. Here, the 1D transport problem is solved by the nonequilibrium Green's function (NEGF) approach in the presence of an applied bias. The 1D Green's function for the *k*th 2D sub-band is written as

$$G_{i} = \frac{1}{E - H_{i}^{1D} - \sum_{i}^{S} - \sum_{i}^{D}},$$
 (3)

where  $H_i^{1D} = -(\hbar^2/2m_z)(\partial^2/\partial z^2) + E_i$ ,  $\sum_i^S$  and  $\sum_i^D$  are self-energy of the *i*th subband in the source and drain electrode. For the NEGF, the 1D electron density in each subband can be obtained as

$$n_i^{\rm 1D} = \frac{1}{\pi \Delta z} \int (f_S G_i \Gamma_i^S G_i^+ + f_D G_i \Gamma_i^D G_i^+) dE, \quad (4)$$

where  $\Delta z$  is the discrete spacing,  $f_{S(D)} = (1 + \exp(E - E_{F,S(D)}/kT))^{-1}$  is Fermi function,  $E_{F,S(D)}$  is Fermi level relevant with the bias  $V_{DS}$  via  $E_{F,S} - E_{F,D} = qV_{DS}$ . The broadening matrices in source and drain are given by  $\Gamma_i^S = i\left(\sum_i^S - \sum_i^{S+}\right)$  and  $\Gamma_i^D = i\left(\sum_i^D - \sum_i^{D+}\right)$ . Symbol "+" denotes complex conjugate operation. Here, spin degeneracy is accounted for. Once the 1D and 2D Schrödinger equations are solved, the 3D electron concentration can be calculated as

$$n^{3D}(x, y, z) = \sum_{i} n_{i}^{1D}(z) |\psi_{i}(x, y; z)|^{2}.$$
 (5)

The above equations are solved under the known materials parameters and device structure except for the electrostatic potential V that should be solved from Poisson's equation

$$\nabla \cdot \left[-\varepsilon_r \nabla V(x, y, z) + \mathbf{P}(x, y, z)\right]$$
  
=  $q[N_D - N_A - n^{3D}(x, y, z)],$  (6)

where  $\varepsilon_r$  is the dielectric constant,  $N_D$  and  $N_A$  are the donor and acceptor doping concentration, **P** is the electrical polarization. In piezoelectric semiconductor AlN and GaN, the electrical polarization  $\mathbf{P} = \mathbf{P}_{sp} + \mathbf{P}_{piezo}$  comes from spontaneous  $\mathbf{P}_{sp}$  and piezoelectric segment  $\mathbf{P}_{piezo} =$  $\mathbf{e} \cdot \mathbf{s}$  with piezoelectric tensor  $\mathbf{e}$  and strain  $\mathbf{s}$ . When an external stress is supplied, the material endures strain  $\mathbf{s} = \mathbf{C}^{-1} \cdot \boldsymbol{\sigma}$  with elastic coefficient tensor  $\mathbf{C}$  and applied stress  $\boldsymbol{\sigma}$ . In experiment, stress is usually applied along growth direction of nanowire *c* axis, which is the case of this study.

In Poisson Eq. (6), Neumann boundary condition, i.e.,  $\mathbf{n} \cdot \nabla V = 0$  is used in the source and drain electrode in order to ensure space-charge neutrality and float sourcedrain voltage relative to Fermi level [34]. Here,  $\mathbf{n}$  denotes the direction normal to the boundary. For other boundaries, the same zero electric field condition is imposed. To accelerate Schrödinger-Poisson convergence, the linear Poisson Eq. (6) is altered to a nonlinear one by introducing a quasi-Fermi-level [34,35]

$$n^{\rm 3D}(x,y,z) = N_{\rm 3D}F_{1/2} \left[ \frac{F_n(x,y,z) + qV(x,y,z)}{kT} \right], \quad (7)$$

where  $N_{3D}$  is the effective density of states for the electrons,  $F_{1/2}$  is the Fermi-Dirac integral of order 1/2,

 $F_n(x, y, z)$  is quasi-Fermi-level, *k* is Boltzmann's constant, and *T* is temperature. This nonlinear Poisson equation provides a feedback mechanism to accelerate iterative convergence process [36]. Additionally, Newton-Raphson iteration and Gaussian elimination method are employed to solve 3D nonlinear Poisson Eqs. (6) and (7). All calculations are based on the finite-difference method. Once the Schrödinger-Poisson equation gets convergence, we can calculate transmission coefficient and current

$$T_i = \operatorname{Tr}(\Gamma_i^S G_i \Gamma_i^D G_i^{\dagger}), J = \frac{2q}{h} \sum_i \int T_i(E)(f_S - f_D) dE,$$
(8)

where Tr stands for matrix trace operator, h is Planck's constant.

There are two possibilities to select insulator barrier: piezoelectric and nonpiezoelectric. For the piezoelectric insulator, a good candidate is AlN(Al<sub>2</sub>O<sub>3</sub>) because it has a larger conduction-band offset energy approximately 2.0 eV in terms of GaN. This large offset energy can significantly restrict the electron propagating in transport direction, and thus form quantum tunneling. Nevertheless, the common piezoelectric property of the AlN insulator and AlN/GaN nanowire renders strain-induced polarization charges relatively lower. As a result, device performance modulated by strain becomes inferior [23,24]. An alternative is to select a nonpiezoelectric insulator, such as HfO<sub>2</sub> [25]. In this case, piezoelectric polarization charges come solely from the polarization in the AlN/GaN nanowire rather than polarization difference between the piezoelectric insulator and nanowire. Therefore, polarization charges induced by strain will obtain a remarkable variation, allowing for a noticeable improvement in device performance. In this context, we mainly focus on the nonpiezoelectric insulator case, whereas the piezoelectric case will be involved in our next work. Due to the lack of relevant band parameters in HfO<sub>2</sub>, we replace it with AlN but cancel its piezoelectric property. To some extent, this treatment is reasonable because the main role of HfO<sub>2</sub> in the PTT is to serve as an insulator barrier.

The piezoelectric charges can simultaneously exist at two terminations of core-shell nanowire due to the polarization discontinuity. Given that the insulator layer is formed at the source side, we take into account only the piezoelectric charges of insulator-nanowire interface throughout this work. The tunneling transport is controlled by the barrier formed at the dielectric layer. Hence, the height and width of this barrier is predominated by the piezoelectric charges at dielectric-nanowire interface instead of those charges at drain-nanowire interface. Particularly, the latter impact on the barrier (or tunneling current) will be greatly reduced with increasing the nanowire length [see Appendix B]. Additionally, owing to the presence of dielectric layer, the piezoelectric charges of dielectric termination would be difficult to be screened by the carriers in source electrode. This dielectric layer can sufficiently prevent the carrier directly transferring from the electrodes to affect interfacial piezoelectric charges.

We fix the doping of the PTT within an experimental accessible value:  $10^{16}$  cm<sup>-3</sup> intrinsic *n* doping,  $5 \times 10^{18}$  cm<sup>-3</sup> *n* doping in the GaN core, and heavy *n* doping  $2 \times 10^{20}$  cm<sup>-3</sup> in source-drain extension. Without special statements, the PTT is comprised of 11.0 nm AlN/GaN core-shell nanowire, L = 1.0 nm insulator layer, 4.0 nm source-drain extension. The sides of hexagon core and shell is  $a_{core} = 2.0$  nm and  $a_{shell} = 3.0$  nm, respectively. The Fermi level in the source is fixed at  $E_F^S = 0.5$  eV. The device is operated at room temperature 300 K. All material parameters in AlN and GaN are used from Refs. [37,38].

#### **III. QUANTUM TUNNELING IN THE PTT**

Figure 2(a) shows the conduction-band potential profile along *c*-axis direction at the center of core-shell hexagon. Here, the bias is set at  $V_{DS} = 2.0$  V. It is clear that at the insulator-nanowire interface the potential is pushed up by compressive strain but down by tensile strain, which is the result of piezoelectric polarization charges. In addition, insulator layer is rather thin (1.0 nm), and thus cannot completely screen the influence of polarization charges on Schottky barrier height (SBH) at the sourceinsulator interface. It leads to a remarkable change in the SBH, which is analogous to a metal-semiconductor contact transistor controlled by the piezotronic effect where interfacial polarization charges modify the SBH to tune device performance [39]. By combining the SBH with the insulator-nanowire potential, the entire barrier height and width become particularly sensitive to strain, which is demonstrated subsequently.

Distinguished from many quantum transport devices with integer plateaus in transmission coefficient T (related directly with conductance by  $T \times q^2/h$ , the PTT has much lower transmission coefficient because the electrons permeate barrier region in an evanescent fashion. This can be seen in Fig. 2(b) under a bias  $V_{DS} = 2.0$  V. The effective barrier height is 1.5-3.0 eV [see Fig. 4(c)] higher than the highest electron energy  $E_{F,S} = 0.5$  eV. Hence, we can unambiguously confirm that transmission coefficient and corresponding current comes from quantum tunneling effect. With the increasing of electron energy, the transmission coefficient gradually increases but its overall amplitude is lower than 1.0%. According to the Fermi-Dirac distribution function, only those electrons with energy less or slightly larger (temperature broadening) than Fermi level  $E_{F,S} = 0.5$  eV contribute to the tunneling current. Hence, the tunneling current is usually weak. Moreover, it also shows that increasing strain can considerably increase transmission probability due to reduced barrier height and width.



FIG. 2. (a) Potential profile of the PTT. (b) Transmission coefficient *T* as a function of electron energy *E*. (c) 1D electron density in the PTT under strain of  $\varepsilon = 1.0\%$  (upper), 0 (middle), and -1.0% (lower). (d) The current-voltage characteristics under different strains. The source and drain Fermi level in (a) are  $E_{F,S} = 0.5$  eV and  $E_{F,D} = -1.5$  eV, respectively. The inserts in (b),(d) are the semilogarithmic *T*-*E*, and *J*-*V*<sub>DS</sub> curve, respectively. The bias used in (a)–(c) is fixed at  $V_{DS} = 2.0$  V.

It is instructive to present 1D electron density distribution in order for intuitively showing the electron tunneling process in the PTT, as displayed in Fig. 2(c) under strains of -1.0%, 0, and 1.0%. The bias is still  $V_{DS} = 2.0$  V. The black solid line is the first sub-band profile. Although there are several sub-bands participating in tunneling transport, only the first one predominates due to strong quantum confinement effect in the core-shell cross section. It shows that in all cases the electrons are mainly resided at source and drain extension region. When strain is -1.0%, the barrier width is wide enough, leading to the electrons being almost completely blocked in source and drain. Barrier width shrinks sharply for strain increased to 0, and thus a tiny amount of electrons can pass through it. Moreover, a clear tunneling process can be observed where 1D electron density is rapidly attenuated with source electrons access to the barrier region. As strain is further increased to 1.0%, barrier width is almost shortened to the insulator thickness 1.0 nm. In this case, the electrons with energy close to Fermi level  $E_{F,S} = 0.5$  eV can tunnel through the insulator, giving rise to a high transmission probability and current.

Owing to the piezoresistive effect, strain sensors based on silicon or graphene have a linear dependence of the current or resistance on strain [11,12,40,41]. The piezoresistive effect is to use strain-induced deformation potential to slightly modify the band structure and then affect the resistance, and thereby the tunability of sensing device is weak due to the deformation potential having a tiny contribution to band structure. This leads to a small gauge factor or low sensitivity in these piezoresistive devices. However, by combining the deformation potential with polarization electric field, our proposed piezoelectric regulation can cause a notable strain-induced change in band structure or tunnel barrier. As is well known, the conductance in tunneling junction is exponentially dependent on tunnel barrier [42]. Therefore, the current or resistance in the proposed tunneling junction sensor can exhibit a highly nonlinear and exponential strain dependence.

Figure 2(d) shows the tunneling current against bias under different strains. When the bias is increased to be higher than a cut-off value, tunneling current is switched on. The current-voltage characteristic is very similar to traditional semiconductor devices based on p-n junctions or metal-semiconductor contacts [39,43], whereas the difference is the PTT with a relatively low on current. We also can see in the insert of Fig. 2(d) that tunneling current can be markedly increased by tensile strain and decreased by compressive strain. At bias  $V_{DS} = 2.0$  V, the on/off current ratio for  $\varepsilon = \pm 1.0\%$  can reach as high as  $10^8$ , which is much larger than experimental measurements approximately 500 in Ref. [25]. Such a huge difference may stem from several factors, including the limitation of current accuracy (approximately 10<sup>-3</sup> nA) in experimental measurement, strain magnitudes ( $\varepsilon = \pm 0.1\%$  in Ref. [25]), nanowire length and cross-section size, or material and structure difference.

First of all, the on/off current ratio significantly relies on the defined on current that is increased exponentially with increasing strain. Therefore, the on/off ratio obtained at strain of 0.1% in Ref. [25] will be much lower than the case of strain 1.0% presented here. A further calculation shows an *on/off* ratio approximately 200 at strain of 0.1%[see Appendix B], which is much closer to the experimental value. Secondly, there are two dielectric layers in ZnO nanowire tunneling junction in the experiment but only one in our core-shell nanowire. This may be a useful ingredient because the traveling electrons will tunnel twice: one is the tunneling from source to nanowire, and the other is the case from nanowire to drain. The two tunneling processes will influence the *on* and *off* current. Additionally, the size of realistic nanowire including the cross section and length is also a relevant factor to affect the on current. To be more specific, the on current would be decreased by reducing quantum confinement for a large cross section, whereas it is increased for a long nanowire. Their combined effects will cause a decreasing current. A 3D simulation of real nanowire is unrealistic and out of our calculation scope due to its large size with length approximately 300 µm and cross section approximately 1.0  $\mu$ m<sup>2</sup> in Ref. [25]. A simplified 1D model may be accessible by neglecting the quantum confinement in the cross-section direction, which will be involved in our future work.

The tunneling effect is a pure quantum phenomenon, examining which will be useful to understand the PTT. Figure 3(a) displays wave functions  $\psi_1 \sim \psi_4$  in the first four sub-bands confined within AlN/GaN core-shell cross section. Our calculation suggests that only these four subbands are occupied in the source and drain, and thus make a contribution to tunneling current. In the core-shell plane, the presence of a high barrier in the shell layer makes wave functions spatially confined inside the core layer. Hence, the tunneling electrons are transported along the GaN layer rather than the AlN layer. In this regard, the GaN core acts mainly as a conductive channel, which is protected by the shell layer. Compared with bare single-crystal nanowire, such a core-shell heterostructure can sufficiently lower current leakage [44], and interface scattering [45].

Figure 3(b) shows the conduction-band offset energy  $E_C$ (left) and electrostatic potential V (right) in the PTT under a bias  $V_{DS} = 2.0$  V and no strain. It shows a high offset energy in the shell layer and the insulator layer, where the former brings in quantum confinement and the latter leads to quantum tunneling. Considering that the source-drain electrodes are experimentally fabricated by surrounding nanowire with a metal film, the source-drain extension regions are treated as a core-shell structure in our simulation. The right of Fig. 3(b) shows the electrostatic potential that is linearly increased from source to drain. Owing to the presence of polarization charges, the electrostatic potential near the insulator-nanowire interface undergoes a first decrease and then increase, giving rise to an energy barrier. It is this energy barrier that allows for the high tunability of tunneling current by strain.

The essence of tunneling transport is the electrons flowing inside the device with a barrier. This process can be clearly illustrated by plotting the 3D electron concentration distributed in the PTT operated at a bias, as shown in Fig. 3(c). Here, the bias is still fixed at  $V_{DS} = 2.0$  V. The piezoelectric charges in the core (red) and shell (blue) layer are also shown at the insulator-nanowire interface. Different from the ionic charge or doping carrier, the piezoelectric charges have an areal density due to the polarization discontinuity  $\Delta P$ . It shows that the piezoelectric charges decrease with increasing strain  $\varepsilon$ . The nonzero piezoelectric charges at  $\varepsilon = 0$  comes from the pure spontaneous polarization  $P_{\rm sp} = -0.029 \text{ C/m}^2$ . Hence, the total polarization charges are reduced by positive piezoelectric polarization  $P_{\text{piezo}} > 0$  at tensile strain but raised by  $P_{\text{piezo}} < 0$  at compressive strain.

In natural state  $\varepsilon = 0$ , a few electrons can tunnel through the insulator layer along a conductive channel that is formed in the GaN core layer. When a smaller compressive strain  $\varepsilon = -0.5\%$  is applied, the conductive channel is switched off due to a higher barrier in insulator layer where the electron concentration decays rapidly. Such a decay becomes more notable if further increasing compressive strain to  $\varepsilon = -1.0\%$ . In this case, tunneling current is much lower approximately  $10^{-8} \mu A/\mu m$ , indicating a good switching-off state. By contrast, for a small tensile strain  $\varepsilon = 0.5\%$ , more electrons can tunnel through insulator layer access to the core-shell nanowire channel due to barrier height that is decreased by positive polarization charges. Increasing strain to  $\varepsilon = 1.0\%$  brings in a further reduction in barrier height, and thus a large number of electrons can enter the channel. Tunneling current can reach as high as approximately 1 µA/µm, demonstrating an excellent switching-on state for the PTT. Notice that due to the quantum mechanics tunneling effect, the tunneling-based



FIG. 3. (a) Wave functions of the first four sub-bands in the core-shell cross-section plane. (b) Offset energy (left) and electrostatic potential (right) in the PTT under a fixed bias  $V_{DS} = 2.0$  V. (c) The 3D electron concentration in the PTT under strain varying from -1.0% to 1.0% (from left to right). The piezoelectric charges (unit C/m<sup>2</sup>) of the core (red) and shell (blue) layer are displayed at the insulator-nanowire interface.

devices usually suffer from low *on* current, which limits its operating speed and ambipolar behavior [46,47]. Nevertheless, the *on* current in our PTT is higher and superior to those in group-IV and III–V, InAs/Si, and carbon-nanotube-based tunnel FETs [48].

## IV. EFFECTIVE BARRIER HEIGHT AND WIDTH IN THE PTT

The above results demonstrate that barrier height and width play a decisive role on the PTT. In order to estimate them, it is necessary to define effective barrier height  $\Phi_B$  and width  $W_B$ . Similar to Ref. [25], the effective barrier height  $\Phi_B$  is defined as the energy difference between the Fermi level and half of the potential in the insulator layer. The effective barrier width  $W_B$  is assumed as space width in the sub-band profile with energy higher than the Fermi level. According to these two definitions, we can intuitively see in Fig. 4(a) that both  $\Phi_B$  and  $W_B$  decrease with increasing strain. Their simultaneous reduction leads to a sharp increase in tunneling current.

Figure 4(b) shows tunneling current as a function of strain under different biases. When strain is higher than a critical value, the PTT is switched *on* and its current increases exponentially. The critical strain depends highly on the bias because the bias can also regulate barrier height and width [4]. In order to estimate strain sensitivity, we plot a semilogarithmic  $J-\varepsilon$  curve in the insert of Fig. 4(b). The semilogarithmic current is almost proportional to strain  $\varepsilon$  for each bias, and the slope



FIG. 4. (a) Potential profile of the first sub-band under bias  $V_{DS} = 2.0$  V. The  $\Phi_B$  and  $W_B$  donate the effective barrier height and width, respectively. (b) The current versus strain under different biases. The insert is the semilogarithmic J- $\varepsilon$  curve. (c) The effective barrier height  $\Phi_B$  (dash lines) and its change  $\Delta \Phi_B$  (solid lines) as a function of strain. (d) The effective barrier width  $W_B$  (dash lines) and its change  $\Delta W_B$  (solid lines) as a function of strain.

decreases with increasing bias. Therefore, the PTT operated at small bias has a higher strain sensitivity. However, small bias corresponds to low *on* current, undesirable in practical device operation. In this regard, it is necessary to select a proper bias compatible with high *on* current as well as large sensitivity, such as  $V_{DS} = 2.0$  V (*on* current approximately 1  $\mu$ A/ $\mu$ m and gauge factor approximately 10<sup>5</sup> at  $\varepsilon = 1.0\%$ ).

Figure 4(c) shows the effective barrier height  $\Phi_B$ (dashed lines) and its change  $\Delta \Phi_B = \Phi_B(\varepsilon) - \Phi_B(0)$ (solid lines) as a function of strain under different biases. The case without bias can be seen as a comparison in Appendix A. The  $\Phi_B$  varying linearly from 3.0 to 1.5 eV as strain increases, is much higher to produce tunneling current. Such a giant variation in barrier width sufficiently demonstrates the superior piezoelectric tunability of tunneling devices, which is almost inaccessible for the general piezoresistive or magnetoresistive modulation [12–14]. Moreover, for a fixed strain, the  $\Phi_B$  decreases with increasing bias, indicating a common nature between bias and strain manipulation in tunneling transistors. The barrier change  $\Delta \Phi_B$  is useful to estimate the sole impact of strain on barrier height, and has been illustrated in Ref. [25]. Figure 4(c) shows that the  $\Delta \Phi_B$  is also linearly decreased with strain, in an agreement with ZnO-based PTT [25]. Moreover, strain-induced barrier change is almost independent on the bias, implying a weak coupling of strain and bias in the modulation of barrier height. However, this is not the case in the modulation of barrier width, as demonstrated subsequently.

The effective barrier width  $W_B$  is another factor to control tunneling current. Figure 4(d) shows the  $W_B$  (dashed lines) and its change  $\Delta W_B = W_B(\varepsilon) - W_B(0)$  (solid lines) against strain under different biases. Similar to the  $\Phi_B$  and  $\Delta \Phi_B$ , the  $W_B$  and  $\Delta W_B$  also decrease with strain. The  $W_B$  has a minima value corresponding to insulator thickness 1.0 nm. These barrier widths higher than 1.0 nm are the results of the potential in insulator-nanowire interface, which can be regulated by polarization charges. This is analogous to the situation where polarization charges act as a bias (or piezopotential) supplied at the insulatornanowire interface [see Fig. 4(a)]. Additionally, Fig. 4(d) also shows that the barrier width  $W_B$  shrinks quickly with increasing bias. Different from  $\Delta \Phi_B$ , the  $\Delta W_B$  relies on bias particularly at low bias. For instance, at  $V_{DS} =$ 1.0 V (2.5 V), the variation in  $\Delta W_B$  can reach 7.1 nm (4.0 nm) over strain range -1.0%-1.0%. It is this remarkable bias dependence of barrier width that directly leads to high current on/off ratio and larger gauge factor in low bias.

As strain approaches  $\varepsilon = 1.0\%$  at bias  $V_{DS} = 2.5$  V, the  $W_B$  reaches its minima 1.0 nm and will remain unchanged, as seen in Fig. 4(d). This does not mean that the influence of barrier width on tunneling transport reaches saturation if strains or bias are further increases. This is because in terms of all occupied electrons, our defined effective barrier width corresponds only to the electron with highest energy, i.e., the Fermi level. Usually, the occupied electrons with low energy will feel a larger barrier width, which can be further reduced even at an unchanged  $W_B = 1.0$  nm.

### V. GAUGE FACTOR AND PERFORMANCE OPTIMIZATION

Gauge factor is a useful indicator to estimate the ability of using strain to control the device, and is usually defined as  $g_C = \Delta J/(J_0\varepsilon)$  for the current, and  $g_R = \Delta R/(R_0\varepsilon)$ for the resistance. Here,  $\Delta J = J(\varepsilon) - J(0)$ ,  $J_0 = J(0)$ ,  $\Delta R = R(\varepsilon) - R(0)$ ,  $R_0 = R(0)$ . Considering that tensile strain enhances the current and compressive strain raises the resistance, we calculate the  $g_C$  at  $\varepsilon > 0$  and the  $g_R$  at  $\varepsilon < 0$  in order for a larger gauge factor [25], as shown in Fig. 5.

In realistic device applications, the large gauge factor indicates a high sensitivity and thus good signal detection. This enables the nanowire tunneling junction to detect tensile (compressive) strain using current (resistance) signal. Additionally, the tunneling junction is also not expected to detect current signal at compressive strain where the device is usually switched *off* with an extremely low current that is beyond the measurement accuracy  $10^{-3}$  nA [25]. In this case, the current signal will become inaccurate. Instead, the resistance signal will become distinct and can be treated as the signal to measure compressive strain.

Figure 5(a) plots two gauge factors as a function of strain under different biases. The current gauge factor  $g_C$ (solid lines) is much high and improved by increasing tensile strain or reducing bias. At strain  $\varepsilon = 1.0\%$ , the  $g_C$ is  $6.2 \times 10^7$ ,  $1.8 \times 10^6$ ,  $1.4 \times 10^5$ ,  $2.7 \times 10^4$ , at the biases  $V_{DS} = 1.0, 1.5, 2.0, 2.5$  V, respectively. However, as mentioned above, small bias has a low on current, and thus a moderate bias  $V_{DS} = 2.0$  V is proper in order for a sufficient device operation. The resistance gauge  $g_R$  (dashed lines) evaluates the capability of restricting electron flowing within the device via strain. As we can see, the  $g_R$ increases with compressive strain, and its amplitude at  $\varepsilon = -1.0\%$  is as high as  $3.9 \times 10^8$ ,  $3.2 \times 10^7$ ,  $4.1 \times 10^6$ ,  $5.5 \times 10^5$ , at the biases  $V_{DS} = 1.0, 1.5, 2.0, 2.5$  V, respectively. Gauge factor in the resistance is usually greater than that in the current, implying that strain-induced piezoelectric polarization is more effective to control electron blockage compared with electron conduction. The combination of high  $g_R$  with  $g_C$  not only reflects good electromechanical performance of the PTT, but also demonstrates its excellent switching behavior.

Owing to the tunneling transistor working under principles of quantum mechanics, the structure and size of the PTT will affect device performance. We examine in Fig. 5(b) the influence of insulator thickness  $W_i$  on gauge





factor. Here, insulator thickness varies from 1.0 to 2.5 nm, which is much closer to the experimental thickness 1.8 nm [25]. Other parameters are the same as Fig. 5(a). The increased  $W_i$  widens barrier width in the PTT, leading to a reduction in tunneling current [49]. In this case, we do not see a decrease in  $g_C$  and  $g_R$  but an increase as the  $W_i$  grows. This is similar to bias modulation case where the decreased current gives rise to an increased gauge factor. The increased gauge factor is due to effective barrier width that becomes more sensitive to strain variation under a thicker insulator layer.

Realistic nanowires grown in experiments are usually much longer in µm level [25–27,29,31,32], and thus difficult to establish simulation model in a quantum perspective due to heavy computation burden. Actually, it is unnecessary to model a long nanowire in the PTT because its electric property will tend to saturation, as plotted in Fig. 5(c). Here, the bias is  $V_{DS} = 2.0$  V and insulator thickness is  $W_i = 1.0$  nm. Other parameters are the same as Fig. 5(a). When core-shell nanowire length L increases from 20 to 30 nm, both  $g_C$  and  $g_R$  obtain a significant enhancement. However, such an enhancement becomes weak and eventually saturated as the L approaches 50 nm. The saturation in gauge factor comes from the effective barrier height and width (not shown here) that are unchanged as nanowire length further increases. This is due to the fact that barrier modulation in the PTT is determined simultaneously by electron transport in the source and drain [34]. When nanowire length is long enough, strain-induced polarization charges at the source side are spatially far away from the drain region, and thus bring in a negligible impact on its electron transport. In this case, the potential barrier depends only on source electron transport that is unchanged if polarization charges and bias are fixed. The saturated  $g_C$  and  $g_R$  are  $1.2 \times 10^8$  $(\varepsilon = 1.0\%)$  and  $1.1 \times 10^{13}$  ( $\varepsilon = -1.0\%$ ), respectively. Such a large gauge factor enables on/off current ratio to be as high as  $10^{17}$  at strain amplitude of 1.0%. More notably, long nanowire allows for a high current (approximately 0.2  $\mu$ A/ $\mu$ m at  $\varepsilon = 1.0\%$  and L = 50 nm), which is distinct from the modulation via bias and insulator thickness where an increase in gauge factor accompanies a considerable decrease in on current. This demonstrates that the realistic longer nanowire is feasible for designing an ultrahighly sensitive strain sensor.

Owing to the quantum confinement effect related with core-shell size, it is necessary to examine its influence on device performance. Figure 5(d) plots gauge factor as a function of strain under different sides lengths of core layer  $a_{core}$ . Here, we fix  $V_{DS} = 2.0$  V,  $W_i = 1.0$  nm, and L = 20 nm. At strain  $\varepsilon = 1.0\%$  (-1.0%), the  $g_C$  ( $g_R$ ) is  $1.4 \times 10^5$  ( $4.1 \times 10^6$ ),  $3.1 \times 10^3$  ( $1.5 \times 10^4$ ),  $9.7 \times 10^2$ ( $1.9 \times 10^3$ ) for  $a_{core} = 2.0$ , 3.0, and 4.0 nm, respectively. It is interesting that unlike the case in Figs. 5(a)–5(c), increasing core size seriously reduces gauge factor but raises tunneling current. This can be well understood from quantum confinement effect where the increased  $a_{core}$ allows for more sub-bands contributing to tunneling transport and thus leads to high conductance. In this case, these sub-bands with low energy still dominate tunneling transport, whereas their electron concentration has to suffer from a significant reduction in source and drain for a fixed heavy doping. Hence, we can see an inferior device performance of the PTT if quantum confinement is reduced by a growing size. In this regard, it is quantum effect that plays a significant role to improve the performance of tunneling transistors.

#### VI. CONCLUSION

In this context, a piezotronic tunneling device based on the AlN/GaN core-shell nanowire is investigated from pure quantum perspective. By jointly controlling barrier height and width of the tunneling transistor, strain-induced polarization charge enables the devices to exhibit high performance with *on/off* current ratio  $10^{17}$ , current gauge factor  $1.2 \times 10^8$ , resistance gauge factor  $1.1 \times 10^{13}$  at strain of 1.0%. The device performance can be further tailored by increasing insulator thickness, nanowire length, and coreshell structure. This study provides an avenue to design high-performance, giant-sensitivity, and low-power strain sensing by extending piezotronic transistor to the level of quantum mechanics.

#### ACKNOWLEDGMENTS

The work is supported by the Natural Science Foundation of China (Grant No. 12174077), National Natural Science Foundation of Guangdong Province (Grant No. 2021A1515012363), the National Natural Science Foundation of China (Grant No. 62004169), and the Basic Research Programs of Taicang, 2021 (Grant No. TC2021JC20).

## APPENDIX A: THE COMPARISON OF BARRIER WITH AND WITHOUT BIAS

In order to compare the results for  $V_{DS} = 2.0$  V, we calculate the sub-band potential profile and barrier height and width for the tunneling junction device without bias, as shown in Fig. 6. Here, the structural parameters of the core-shell nanowire are the same as those in Fig. 4.

The potential profile shows in Fig. 6(a) that the straininduced piezoelectric charges can also bring a notable change in the barrier height. Similar to the case of  $V_{DS} =$ 2.0 V, the effective barrier height  $\Phi_B$  in Fig. 6(b) is linearly dependent on the strain  $\varepsilon$ . However, the potential of the entire nanowire is higher than the Fermi level  $E_F = 0.5$  eV at zero bias [see Fig. 6(a)], leading to a large effective barrier width. When the bias is supplied, this barrier width will become tunable by strain-induced piezoelectric charges.



FIG. 6. The results of no source-drain bias. (a) Potential profile of the first sub-band, and (b) effective barrier width  $W_B$  and height  $\Phi_B$  versus strain. All the structural parameters are the same as those in Fig. 4.

Therefore, different from the barrier height, the tunability of barrier width is the combined effect of bias and strain.

# APPENDIX B: PIEZOELECTRIC CHARGES AT DRAIN-NANOWIRE INTERFACE

Generally speaking, piezoelectric charges are simultaneously present at two ends of nanowire due to the polarization discontinuity. In our tunneling device, we take into account only the piezoelectric charges at the insulatornanowire interface due to the dielectric layer located at the source electrode. For comparison, we calculate the tunneling current as a function of strain in Fig. 7 with (dashed lines) and without (solid lines) drain-nanowire piezoelectric charges. Here, the piezoelectric charges at the



FIG. 7. The tunneling current as a function of strain under the core-shell nanowire length L = 20, 50, and 100 nm. The dashed and solid lines correspond to the case with and without drain-nanowire piezoelectric charges, respectively. The insert is the enlargement of current. Other parameters are  $W_i = 1.0$  nm,  $a_{core} = 2.0$  nm,  $V_{DS} = 2.0$  V.

insulator-nanowire layer are already taken into account in both cases. The tunneling device has insulator thickness  $W_i = 1.0$  nm, the sides of hexagonal core  $a_{core} = 2.0$  nm, and source-drain bias  $V_{DS} = 2.0$  V.

As we can see, the drain-nanowire piezoelectric charges have a significant influence on the tunneling current when the core-shell nanowire length is short L = 20 nm. This is because the piezoelectric charges of drain side are very close to source side and thus can notably affect the barrier formed at insulator layer. This affect can be decreased by increasing nanowire length. At L = 100 nm, the drainnanowire piezoelectric charges would cause only a tiny difference on the tunneling current. The insert of Fig. 7 further shows this tiny difference existing not only in the switching *on* (high current) case but also in the switching *off* (low current) case.

An interesting result shown here is that the slope of current versus strain becomes large with increasing coreshell nanowire length. This indicates the *on/off* current ratio will be further enhanced. The specific calculation shows that at strain  $\varepsilon = \pm 0.1\%$ , the *on/off* ratio is approximately 200, which is much closer to the experimental measurement value approximately 500 [25].

- J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors, Phys. Rev. Lett. 93, 196805 (2004).
- [2] P.-F. Wang, K. Hilsenbeck, T. Nirschl, M. Oswald, C. Stepper, M. Weis, D. Schmitt-Landsiedel, and W. Hansch, Complementary tunneling transistor for low power application, Solid-State Electron. 48, 2281 (2004).
- [3] A. Seabaugh, The tunneling transistor, IEEE Spectrum **50**, 35 (2013).
- [4] R. Tsu and L. Esaki, Tunneling in a finite superlattice, Appl. Phys. Lett. 22, 562 (1973).
- [5] C. Jia, M. Famili, M. Carlotti, Y. Liu, P. Wang, I. M. Grace, Z. Feng, Y. Wang, Z. Zhao, and M. Ding, Quantum

interference mediated vertical molecular tunneling transistors, Sci. Adv. 4, eaat8237 (2018).

- [6] W. Li, H. Liu, S. Wang, S. Chen, T. Han, and K. Yang, Design and investigation of dopingless dual-gate tunneling transistor based on line tunneling, AIP Adv. 9, 045109 (2019).
- [7] G. Lu, Y. Wei, X. Li, G. Zhang, G. Wang, L. Liang, Q. Li, S. Fan, and Y. Zhang, Reconfigurable tunneling transistors heterostructured by an individual carbon nanotube and MoS<sub>2</sub>, Nano Lett. **21**, 6843 (2021).
- [8] Y. Liu, J. Sheng, H. Wu, Q. He, H. C. Cheng, M. I. Shakir, Y. Huang, and X. Duan, High-current-density verticaltunneling transistors from graphene/highly doped silicon heterostructures, Adv. Mater. 28, 4120 (2016).
- [9] G. Nazir, A. Rehman, and S.-J. Park, Energy-efficient tunneling field-effect transistors for low-power device applications: challenges and opportunities, ACS Appl. Mater. Interfaces 12, 47127 (2020).
- [10] L. L. Chang, L. Esaki, and R. Tsu, Resonant tunneling in semiconductor double barriers, Appl. Phys. Lett. 24, 593 (1974).
- [11] X. Yang, J. Lim, G. Sun, K. Wu, T. Nishida, and S. Thompson, Strain-induced changes in the gate tunneling currents in p-channel metal-oxide-semiconductor field-effect transistors, Appl. Phys. Lett. 88, 052108 (2006).
- [12] P.-F. Guo, L.-T. Yang, Y. Yang, L. Fan, G.-Q. Han, G. S. Samudra, and Y.-C. Yeo, Tunneling field-effect transistor: Effect of strain and temperature on tunneling current, IEEE Electron Device Lett. 30, 981 (2009).
- [13] L. M. Loong, X. Qiu, Z. P. Neo, P. Deorani, Y. Wu, C. S. Bhatia, M. Saeys, and H. Yang, Strain-enhanced tunneling magnetoresistance in MgO magnetic tunnel junctions, Sci. Rep. 4, 1 (2014).
- [14] T. Shen, A. V. Penumatcha, and J. Appenzeller, Strain engineering for transition metal dichalcogenides based field effect transistors, ACS Nano 10, 4712 (2016).
- [15] P. K. Dubey, N. Yogeswaran, F. Liu, A. Vilouras, B. K. Kaushik, and R. Dahiya, Monolayer MoSeâĆĆ-based tunneling field effect transistor for ultrasensitive strain sensing, IEEE Trans. Electron Devices 67, 2140 (2020).
- [16] L. C. L. Y. Voon and M. Willatzen, *The k-p Method: Electronic Properties of Semiconductors* (Springer, Berlin, 2009).
- [17] H. Dong, J. Sun, S. Ma, J. Liang, T. Lu, Z. Jia, X. Liu, and B. Xu, Effect of potential barrier height on the carrier transport in InGaAs/GaAsP multi-quantum wells and photoelectric properties of laser diode, Phys. Chem. Chem. Phys. 18, 6901 (2016).
- [18] B. Monemar and B. Sernelius, Defect related issues in the "current roll-off" in InGaN based light emitting diodes, Appl. Phys. Lett. 91, 181103 (2007).
- [19] S. A. Fortuna and X. Li, Metal-catalyzed semiconductor nanowires: a review on the control of growth directions, Semicond, Sci. Tech. 25, 024005 (2010).
- [20] Y. Zhu, N. Jain, S. Vijayaraghavan, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, N. Monsegue, and M. K. Hudait, Defect assistant band alignment transition from staggered to broken gap in mixed As/Sb tunnel field effect transistor heterostructure, J. Appl. Phys. **112**, 094312 (2012).

- [21] Y. Zhu, M. K. Hudait, D. K. Mohata, B. Rajamohanan, S. Datta, D. Lubyshev, J. M. Fastenau, and A. K. Liu, Structural, morphological, and defect properties of metamorphic In<sub>0.7</sub>Ga<sub>0.3</sub>As/GaAs<sub>0.35</sub>Sb<sub>0.65</sub> p-type tunnel field effect transistor structure grown by molecular beam epitaxy, J. Vac. Sci. Technol., B **31**, 041203 (2013).
- [22] T. Hanada, Basic properties of ZnO, GaN, and related materials, Adv. Mater. Res. **19**, 1 (2009).
- [23] X. Liao, X. Yan, P. Lin, S. Lu, Y. Tian, and Y. Zhang, Enhanced performance of ZnO piezotronic pressure sensor through electron-tunneling modulation of MgO nanolayer, ACS Appl. Mater. Interfaces 7, 1602 (2015).
- [24] S. Liu, L. Wang, X. Feng, J. Liu, Y. Qin, and Z. L. Wang, Piezotronic tunneling junction gated by mechanical stimuli, Adv. Mater. 31, 1905436 (2019).
- [25] Q. Yu, R. Ge, J. Wen, T. Du, J. Zhai, S. Liu, L. Wang, and Y. Qin, Highly sensitive strain sensors based on piezotronic tunneling junction, Nat. Commun. 13, 1 (2022).
- [26] Y. H. Ra, S. Kang, and C. R. Lee, Ultraviolet lightemitting diode using nonpolar AlGaN core-shell nanowire heterostructures, Adv. Opt. Mater. 6, 1701391 (2018).
- [27] Y.-H. Ra and C.-R. Lee, Core-shell tunnel junction nanowire white-light-emitting diode, Nano Lett. 20, 4162 (2020).
- [28] K. Li, X. Liu, Q. Wang, S. Zhao, and Z. Mi, Ultralowthreshold electrically injected AlGaN nanowire ultraviolet lasers on Si operating at low temperature, Nat. Nanotechnol. 10, 140 (2015).
- [29] W. Song, R. Wang, X. Wang, D. Guo, H. Chen, Y. Zhu, L. Liu, Y. Zhou, Q. Sun, and L. Wang, a-axis GaN/AlN/AlGaN core–shell heterojunction microwires as normally off high electron mobility transistors, ACS Appl. Mater. Interfaces 9, 41435 (2017).
- [30] F. Glas, Strain in nanowires and nanowire heterostructures, Semicond. Semimetals **93**, 79 (2015).
- [31] L. Balaghi, G. Bussone, R. Grifone, R. Hübner, J. Grenzer, M. Ghorbani-Asl, A. V. Krasheninnikov, H. Schneider, M. Helm, and E. Dimakis, Widely tunable GaAs bandgap via strain engineering in core/shell nanowires with large lattice mismatch, Nat. Commun. 10, 1 (2019).
- [32] L. Balaghi, S. Shan, I. Fotev, F. Moebus, R. Rana, T. Venanzi, R. Hübner, T. Mikolajick, H. Schneider, and M. Helm, High electron mobility in strained GaAs nanowires, Nat. Commun. 12, 1 (2021).
- [33] L. J. Lauhon, M. S. Gudiksen, D. Wang, and C. M. Lieber, Epitaxial core-shell and core-multishell nanowire heterostructures, Nature 420, 57 (2002).
- [34] Z. Ren, R. Venugopal, S. Goasguen, S. Datta, and M. S. Lundstrom, nanoMOS 2.5: A two-dimensional simulator for quantum transport in double-gate MOSFETs, IEEE Trans. Electron Devices 50, 1914 (2003).
- [35] J. Wang, E. Polizzi, and M. Lundstrom, A threedimensional quantum simulation of silicon nanowire transistors with the effective-mass approximation, J. Appl. Phys. 96, 2192 (2004).
- [36] Z. Ren, Nanoscale MOSFETs: Physics, Simulation and Design (Purdue University, West Lafayette, 2001).
- [37] I. Vurgaftman, J.á. Meyer, and L.á. Ram-Mohan, Band parameters for III–V compound semiconductors and their alloys, J. Appl. Phys. 89, 5815 (2001).

- [38] V. Litvinov, Electron spin splitting in polarization-doped group-III nitrides, Phys. Rev. B 68, 155314 (2003).
- [39] J. Zhou, Y. Gu, P. Fei, W. Mai, Y. Gao, R. Yang, G. Bao, and Z. L. Wang, Flexible piezotronic strain sensor, Nano Lett. 8, 3035 (2008).
- [40] T. Toriyama, Y. Tanimoto, and S. Sugiyama, Single crystal silicon nano-wire piezoresistors for mechanical sensors, J. Microelectromech. Syst. 11, 605 (2002).
- [41] S.-H. Bae, Y. Lee, B. K. Sharma, H.-J. Lee, J.-H. Kim, and J.-H. Ahn, Graphene-based transparent strain sensor, Carbon 51, 236 (2013).
- [42] W. Brinkman, R. Dynes, and J. Rowell, Tunneling conductance of asymmetrical barriers, J. Appl. Phys. 41, 1915 (1970).
- [43] Y. Liu, Y. Zhang, Q. Yang, S. Niu, and Z. L. Wang, Fundamental theories of piezotronics and piezo-phototronics, Nano Energy 14, 257 (2015).
- [44] S. Sahay and M. J. Kumar, Controlling L-BTBT and volume depletion in nanowire JLFETs using core-shell architecture, IEEE Trans. Electron Devices 63, 3790 (2016).

- [45] H. J. Joyce, S. A. Baig, P. Parkinson, C. L. Davies, J. L. Boland, H. H. Tan, C. Jagadish, L. M. Herz, and M. B. Johnston, The influence of surfaces on the transient terahertz conductivity and electron mobility of GaAs nanowires, J. Phys. D: Appl. Phys. 50, 224001 (2017).
- [46] J. Appenzeller, Y.-M. Lin, J. Knoch, Z. Chen, and P. Avouris, Comparing carbon nanotube transistors-the ideal choice: a novel tunneling device design, IEEE Trans. Electron Devices 52, 2568 (2005).
- [47] O. M. Nayfeh, C. N. Chleirigh, J. Hennessy, L. Gomez, J. L. Hoyt, and D. A. Antoniadis, Design of tunneling field-effect transistors using strained-silicon/strained-germanium type-II staggered heterojunctions, IEEE Electron Device Lett. 29, 1074 (2008).
- [48] C. Convertino, C. Zota, H. Schmid, A. M. Ionescu, and K. Moselund, III–V heterostructure tunnel field-effect transistor, J. Phys.: Condens. Matter 30, 264005 (2018).
- [49] X. Yang, Y. Gu, M. A. Migliorato, and Y. Zhang, Impact of insulator layer thickness on the performance of metal–MgO–ZnO tunneling diodes, Nano Res. 9, 1290 (2016).