Polarization-Dominated Internal Timing Mechanism in a Ferroelectric Second-Order Memristor

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Second-order memristors are considered as ideal synaptic emulators for their capability of exhibiting Ca^{2+}-like dynamics. Recently, ferroelectric second-order memristors were developed, but whether their temporal conductance evolution is related to polarization dynamics remains unclear owing to the difficulty in directly measuring polarization in these devices. This issue is addressed here by using a ferroelectric diode (FD) that shows both second-order memristive behavior and well-shaped polarization-voltage hysteresis loops. It is demonstrated that the resistance-state change in the FD is triggered by polarization switching, arising from polarization-controlled Schottky emission. Moreover, concurrent conductance decay and polarization relaxation are observed, and their correlation is quantitatively evidenced, suggesting that conductance decay is caused by the polarization-relaxation-induced increase in the Schottky barrier height. Using polarization relaxation as an internal timing mechanism, our FD-based second-order memristor faithfully emulates various synaptic functions, where short-term plasticity is indispensable, including excitatory postsynaptic current, paired-pulse facilitation, the transition from short-term plasticity to long-term plasticity, learning experience, and associative learning. Our study not only reveals a polarization-dominated internal timing mechanism in the FD-based second-order memristor, but also demonstrates that such a device is a promising building block for biorealistic neuromorphic systems.

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I. INTRODUCTION

Conventional digital computers are inefficient at handling data-intensive tasks, such as image recognition and natural language processing, due to the memory wall existing in the von Neumann architecture [1,2]. This has triggered a surge in research into alternative computing technologies. Neuromorphic computing, as inspired by the architecture and operation principle of the human brain, has recently emerged as a promising computing paradigm with in-memory computation capability, massive parallelism, and ultralow power consumption [3]. A neuromorphic computing system is constructed by artificial neurons and synapses. In particular, artificial synapses with reconfigurable connection strengths (i.e., weights) are the key units to realize memory and learning functions. Most previous artificial synapses were based on first-order memristors, the conductances of which are controlled solely by external stimuli [4,5]. However, there is a lack of mechanism for the spontaneous decay of conductance, making these devices unable to emulate the short-term plasticity (STP) of a biological synapse (notably, STP refers to a temporal change in synaptic weight that can recover to its initial value in a short period, typically ranging from tens of milliseconds to a few minutes).

Unlike their first-order counterparts, second-order memristors exhibit tunable conductances, which are modulated by both external stimuli and internal state variables with

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short-term dynamics [6,7]. In such a memristor, the temporal evolution of its internal state variable is analogous to the Ca^{2+} dynamics in a biological synapse, thus allowing a biorealistic implementation of synaptic plasticity. Previously reported second-order memristors were mainly based on filament-forming oxides, which utilized rich ionic dynamics, including the thermal dissipation of oxygen vacancies [6], decay of the oxygen-vacancy mobility [7], and diffusion of metal species [8], as the internal timing mechanisms. These devices successfully emulate typical synaptic functions, such as spike-frequency- and -timing-dependent plasticity, using simple spike signals [6–8]. However, they still suffer from relatively large cycle-to-cycle and device-to-device variations due to the stochastic nature of ionic drift and diffusion processes [3].

Compared with ionic dynamics, ferroelectric polarization dynamics are inherently more deterministic [9]. Great attention has thus been paid to ferroelectric memristors, including the ferroelectric tunnel junction (FTJ) [10,11], ferroelectric diode (FD) [12–15], and ferroelectric field-effect transistor (FEFET) [16,17], which use polarization to modulate the tunneling barrier, interfacial Schottky barrier, and carrier accumulation or depletion, respectively. Notably, in most previous ferroelectric memristors, polarization and its associated conductance were modulated solely by an external field [9,13,18–23], restricting these devices to the level of first-order memristors. Only recently were ferroelectric second-order memristors successfully developed [14,15,24–27], by mainly using the depolarization effect. However, the polarization dynamics (particularly polarization relaxation in the absence of an external field) remain largely unexplored in the reported ferroelectric second-order memristors, probably due to the difficulty in directly measuring polarization in these devices (see detailed reasons in the next paragraph). A critical question thus remains about whether the temporal conductance evolution in these devices is truly related to the polarization dynamics. Answering this question is important not only for understanding the internal timing mechanism in these devices, but also for manipulating the temporal behaviors of polarization and conductance towards the biorealistic implementation of synaptic functions.

To address the above question, a ferroelectric memristor not only exhibiting second-order memristive behavior but also allowing direct polarization measurement is required. The FTJ typically suffers from a large leakage current because the ferroelectric layer is ultrathin [24]. The FEFET typically undergoes insufficient charge compensation due to the poor conductivity of the semiconducting channel [28]. These factors make it very difficult or even impractical to directly measure polarization in the FTJ and FEFET. By contrast, the FD can exhibit a small leakage current due to the relatively large ferroelectric layer thickness and the reverse-bias Schottky barrier at one of the ferroelectric-metal interfaces. In addition, the FD uses two metal electrodes with high conductivities, which can ensure good charge compensation. As a result, the FD allows direct polarization measurement, and moreover, it can exhibit well-shaped polarization-voltage (*P*-*V*) hysteresis loops [29,30]. A ferroelectric second-order memristor based on a FD is therefore an ideal platform not only for verifying whether the internal timing mechanism is polarization dominated, but also for faithful emulation of the STP.

Here, we develop a ferroelectric second-order memristor based on a $Pt/BiFeO_3$ (BFO)/$SrRuO_3$ (SRO) FD. Combining the polarization and current measurements, we show that the transition from the high-resistance state (HRS) to the low-resistance state (LRS) is induced by down-to-up polarization switching, revealing the correlation between polarization and conductance. Furthermore, we show that the conductance decay in the LRS is accompanied by relaxation of the upward polarization driven by a downward imprint field (E_{imp}), and their quantitative correlation indicates that the conductance decay is caused by the polarization-relaxation-induced increase in Schottky barrier height. Using polarization relaxation as an internal timing mechanism, the FD-based second-order memristor faithfully emulates various synaptic functions where STP is indispensable, including excitatory postsynaptic current (EPSC), paired-pulse facilitation (PPF), the transition from STP to long-term plasticity (LTP), learning experience, and associative learning. This study therefore demonstrates that the FD-based second-order memristor with a robust polarization-dominated internal timing mechanism is a well-functioning synaptic emulator, highlighting its potential as a building block for biorealistic neuromorphic systems.

II. SAMPLE PREPARATION AND CHARACTERIZATION

About 110-nm BFO epitaxial thin films are grown on $SrTiO_3$ (STO) (001) substrates with about 40-nm SRO buffer layers using pulsed laser deposition (PLD) (KrF excimer laser with $\lambda = 248$ nm). Laser energy fluences of about 1.0 and 1.1 J/cm^2 are used for the deposition of SRO and BFO films, respectively, while the repetition rates for both films are kept the same, i.e., 5 Hz. The SRO films are first deposited on STO substrates at 680 °C under an oxygen pressure of 15 Pa. Subsequently, the BFO films are deposited on top of the SRO films at 690 °C under an oxygen pressure of 19 Pa. After deposition, the BFO/SRO films are cooled to room temperature at a rate of 10 °C/min under 1000-Pa oxygen atmosphere. To construct the devices, circular Pt electrodes (diameter, ∼100 μm; thickness, ∼10 nm) are *ex situ* deposited on the BFO films by PLD through a shadow mask at room temperature under vacuum.

The crystalline structures and epitaxial qualities of the BFO/SRO films are examined using x-ray diffraction (XRD) and reciprocal space mapping (RSM) (PANalytical X'Pert PRO). The surface morphologies and domain structures are characterized by atomic force microscopy (AFM) and piezoresponse force microscopy (PFM), respectively, on a commercial scanning probe microscope (Asylum Research MFP-3D) with Pt-coated silicon tips (Nanoworld EFM Arrow). Both PFM imaging and loop measurements are conducted in the dual ac resonance tracking mode with an ac driving voltage of 0.8 V. The macroscopic P-V hysteresis loops and I-V characteristics of the Pt/BFO/SRO devices are measured with a ferroelectric workstation (Radiant Precision Multiferroic) and a source meter (Keithley 6430), respectively.

Figure S1(a) within the Supplemental Material [31] shows the XRD θ-2θ scan of the BFO/SRO epitaxial film grown on the STO substrate. Only (00l) diffraction peaks from BFO, SRO, and STO are observed, evidencing the phase purity of both BFO and SRO layers. Moreover, the epitaxial character of the BFO/SRO heterostructure on the STO substrate is confirmed by the (103) and (113) RSMs [Figs. S1(b) and S1(c) within the Supplemental Material [31]]. Figure S2(a) within the Supplemental Material [31] shows the AFM topography image of the BFO film. The surface is relatively flat (root-mean-square roughness, ∼750 pm) with bunched steps, which is a typical morphological feature of a relatively thick BFO film [32]. Our BFO film is self-polarized, where most domains are oriented downward in the as-grown state, as revealed by the PFM phase images [Figs. S2(c) and S2(d) within the Supplemental Material [31]]. Moreover, the combined PFM phase images and hysteresis loops [Fig. S2(e) within the Supplemental Material [31]] further show that up-to-down domain switching is easier than the reverse switching, suggesting the existence of a downward E_{imp} in our BFO film.

III. RESULTS AND DISCUSSION

A. Polarization switching and relaxation

The macroscopic ferroelectric properties of the Pt/BFO/SRO devices (device size, ∼100 μm in diameter) are investigated by measuring polarization-voltage (P-V) hysteresis loops. The voltage is applied to the Pt electrode, while the SRO electrode is grounded. Bipolar P-V loops are first measured by using the pulse scheme shown in the inset of Fig. 1(a). The first pair of positive and negative triangular pulses are used to preset the device to a polarization-up (P_{up}) state, followed by a delay period during which no voltage is applied. Then, two pairs of positive and negative triangular pulses (cycles 1 and 2, respectively) are applied consecutively to measure the P-V loops. Figure 1(a) shows the P-V loops measured in cycles 1 and 2 (pulse amplitude, ±4 V; pulse width, 0.15 ms; delay period, 1 min). Both cycles of P-V loops show a large remanent polarization (P_r) of about 65 μC/cm^2, which is consistent with those reported for the BFO (001) epitaxial films [30,33,34]. In addition, it is observed that the negative coercive voltage (∼−2.8 V for both cycles) is at least about 0.5 V larger than the positive one (∼2.3 and ∼1.9 V for cycles 1 and 2, respectively), evidencing again the presence of a downward E_{imp}.

By further inspecting Fig. 1(a), one can find that there is a gap between the starting $-P_r$ and ending $-P_r$ in the loop of cycle 1, while it is absent in the loop of cycle 2. Note that the starting $-P_r$ and ending $-P_r$ reflect the polarization states at the beginning of the positive triangular pulse and the end of the negative triangular pulse, respectively [see schematic illustration in the inset of Fig. 1(a)]. The ending $-P_r$ is large (∼−64.4 μC/cm^2) and close to $+P_r$ (∼64.3 μC/cm^2) in magnitude, because polarization is fully switched upward right after application of the negative triangular pulse. However, the starting $-P_r$ is observed to be smaller (∼−56.9 μC/cm^2), suggesting that the P_{up} state (corresponding to $-P_r$) is unstable. This can be well correlated with the downward E_{imp}. More specifically, the downward E_{imp} may cause the back-switching of some upward polarization during the delay period, thus reducing the starting $-P_r$ and giving rise to the gap in the loop of cycle 1. By contrast, the loop of cycle 2 shows the absence of the gap, which is well attributed to the zero delay period between cycles 1 and 2, disallowing the occurrence of polarization relaxation.

The polarization-relaxation behavior in the P_{up} state is further characterized by measuring the monopolar P-V loops. As shown in the inset of Fig. 1(b), a negative preset pulse is first applied, followed by a delay period and a positive measurement pulse. Figure 1(b) shows the monopolar P-V loops with different delay periods (pulse amplitude, +4 V; pulse width, 0.15 ms). As the delay period becomes longer, the starting $-P_r$ becomes smaller, indicating that more polarization is back-switched to the downward direction. To further support this, the polarization state after the delay period is double-checked by applying a negative measurement pulse [see the pulse scheme in the inset of Fig. 1(c)]. The monopolar P-V loops with different delay periods (pulse amplitude, −4 V; pulse width, 0.15 ms) are presented in Fig. 1(c). It is clearly seen that the starting $-P_r$ becomes smaller with a prolonged delay period, consistent with the results in Fig. 1(b). Moreover, all the loops in Fig. 1(c) exhibit an "S" shape as the voltage increases from 0 to −4 V, which is a fingerprint of polarization switching. Because the polarization that is switched during the loop measurement can only come from the previously relaxed polarization, it is thus confirmed that polarization in the P_{up} state gradually relaxes during the delay period.

As a comparison, the stability of the polarization-down (P_{down}) state is also investigated. As shown in the inset of Fig. 1(d), the P_{down} state is obtained by applying a positive

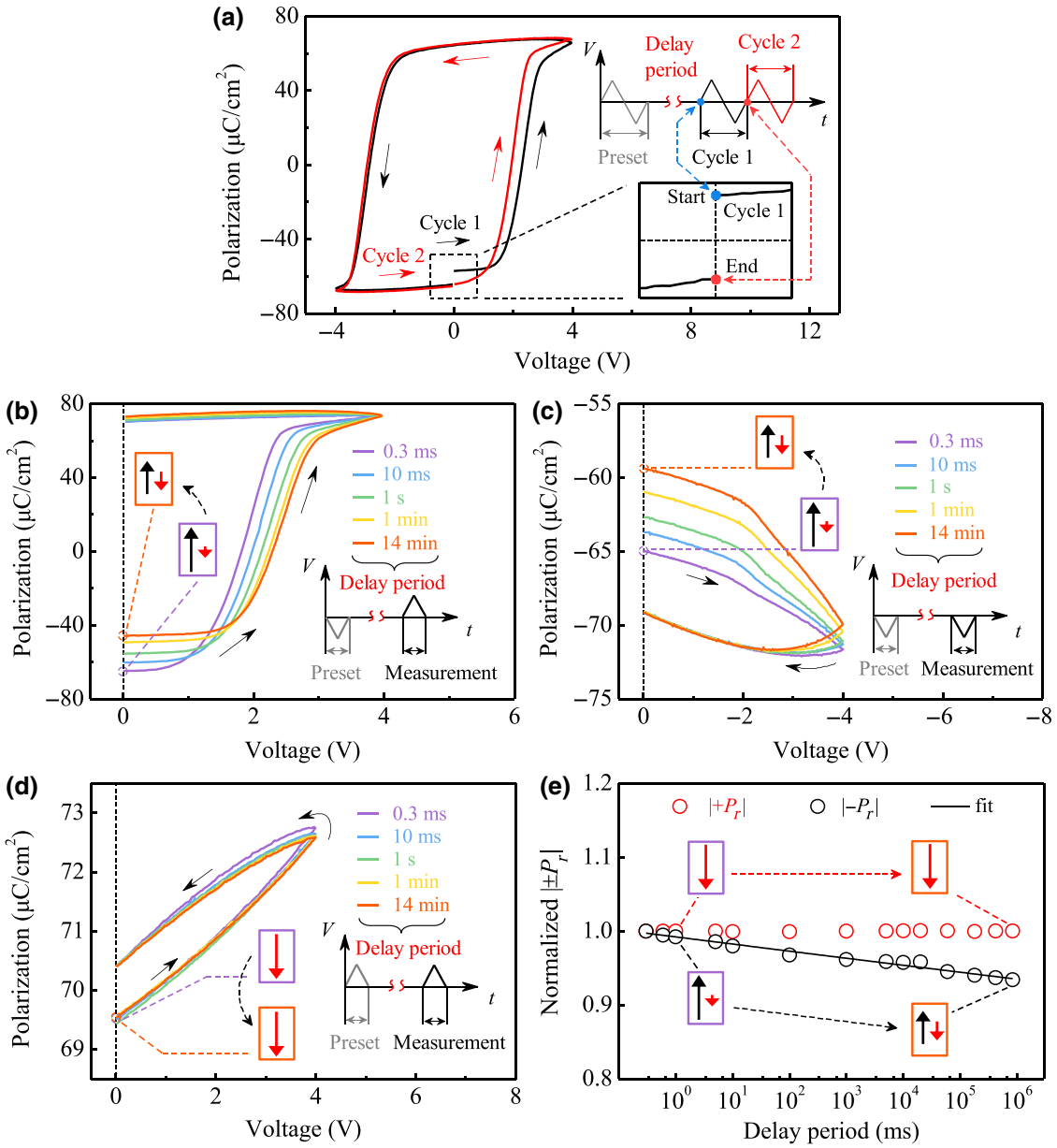

FIG. 1. Polarization switching and relaxation in the Pt/BFO/SRO device. (a) Two cycles of bipolar *P*-*V* hysteresis loops. Upper inset shows the schematics of the pulses applied in the bipolar loop measurement, while the lower inset shows an enlarged part of the *P*-*V* loop of cycle 1 near $-P_r$. Monopolar *P*-*V* hysteresis loops measured by applying (b) positive and (c) negative measurement pulses with different delay periods after negative preset pulses, and (d) those measured by applying positive measurement pulses with different delay periods after positive preset pulses. Insets in (b)–(d) show the schematics of the pulses applied in the monopolar loop measurements. (e) Normalized $|\pm P_r|$ as a function of the delay period. In (b)–(e), black and red solid arrows represent upward and downward polarizations, respectively.

preset pulse, and the polarization state after a certain delay period is probed by applying a positive measurement pulse. Figure 1(d) shows the monopolar *P*-*V* loops with different delay periods (pulse amplitude, +4 V; pulse width, 0.15 ms). These loops almost overlap and they all exhibit very small hysteresis windows, suggesting that negligible polarization relaxation occurs in the P_{down} state. This is not unexpected because E_{imp} is pointing in the downward direction, which would not cause the back-switching of the downward polarization.

To better show the stability difference between the P_{up} and P_{down} states, the corresponding remanent polarizations (i.e., $-P_r$ and $+P_r$, respectively) are plotted against the delay period, as shown in Fig. 1(e). There is almost no change in $+P_r$ with prolonged delay period, while $-P_r$ decreases by about 6.6% as the delay period increases to

840 s. This unambiguously confirms the existence of the downward E_{imp}, which causes polarization relaxation only in the P_{up} state. This also excludes the depolarization field (E_{DP}) as the major driving force for polarization relaxation, because E_{DP} would induce polarization relaxation in both P_{up} and P_{down} states.

To gain a deeper insight, the polarization decay behavior in the P_{up} state is fitted using a power-law relationship [35]:

$$\frac{|-P_r(t=0)| - |-P_r(t)|}{|-P_r(t=0)|} \sim t^{-n}, \tag{1}$$

where $-P_r(t)$ is the remanent polarization at moment t, and n is the decay exponent. Figure 1(e) shows good agreement between the fitting curve and experimental data, demonstrating that polarization decay follows the power law. Based on the theory in Ref. [35], such power-law-type polarization relaxation at room temperature typically originates from an internal-field-induced lowering of the domain nucleation energy to a level comparable to the thermal energy. The internal field in our Pt/BFO/SRO device is just the downward E_{imp}. Therefore, the downward E_{imp} may induce the back-switching of upward polarization via reducing the nucleation energy of downward domains.

The E_{imp}-induced polarization relaxation provides an internal timing mechanism, which may enable our Pt/BFO/SRO device to function as a second-order memristor. To demonstrate this, the resistive-switching (RS) behavior of the device is investigated, as detailed in the next section.

B. One-side diode-type resistive switching

Figure 2(a) shows the typical current-voltage (I-V) characteristics of the Pt/BFO/SRO device measured with a voltage sweep of $-3\ \text{V} \rightarrow 0 \rightarrow +3\ \text{V} \rightarrow 0 \rightarrow -3\ \text{V}$ (sweep rate, 0.14 V/s). It is observed that the resistance state changes from HRS to LRS in the negative voltage region, but it always remains HRS in the positive voltage region. Such RS behavior is called the one-side diode effect, which was reported previously [30,36]. To understand its origin, there are two questions to be answered: what causes HRS $\rightarrow$ LRS switching in the negative voltage region and why is the HRS persistent in the positive voltage region.

We first focus on the origin of HRS $\rightarrow$ LRS switching in the negative voltage region. The I-V characteristics are measured with voltage sweeps of $0 \rightarrow -V_{max} \rightarrow 0$, where $-V_{max}$ is varied from -0.8 to -2.8 V. Before each negative voltage sweep, a positive voltage sweep of $0 \rightarrow +3\ \text{V} \rightarrow 0$ is applied to preset the device to an initial HRS. As shown in Fig. 2(b), the hysteresis window becomes wider as $-V_{max}$ increases. Figure 2(c) plots the *on*:*off* ratio read at -0.8 V as a function of $-V_{max}$. A relatively abrupt increase in *on*:*off* ratio is observed at about -2.0 V, which is regarded as the critical voltage for RS. Moreover, this critical voltage for RS corresponds well to the low-frequency coercive voltage for polarization switching (~ -2.2 V; see Fig. S3 within the Supplemental Material [31] for a more detailed discussion). This reveals that HRS $\rightarrow$ LRS switching in the negative voltage region is induced by down-to-up polarization switching. In addition, the hysteretic I-V characteristics show a weak dependence on the voltage sweep rate (Fig. S4 within the Supplemental Material [31]), thus excluding ion migration or charge trapping as the major origin of HRS $\rightarrow$ LRS switching in the negative voltage region.

In the positive voltage region, however, the persistence of HRS suggests that conduction is dominated by factors other than polarization. Lee *et al.* [30] proposed that an interfacial defective layer capable of trapping charge carriers might be responsible for the persistence of HRS. Our BFO film grown on the SRO bottom electrode is self-poled downward [Fig. S2(c) within the Supplemental Material [31]]. The negative polarization charge at the BFO surface may induce the accumulation of positively charged oxygen vacancies (O-V) during high-temperature film deposition, leading to an O-V-rich defective layer near the surface (see Fig. S5 within the Supplemental Material [31] for evidence). This layer in the Pt/BFO/SRO device can suppress carrier injection, and thus, preserve the HRS. In addition, because of its positive charge, the O-V-rich defective layer is likely to be the origin of the downward E_{imp} (see Fig. S6 within the Supplemental Material [31] for a schematic illustration). To verify that the O-V-rich defective layer is responsible for the persistence of HRS and the presence of E_{imp}, we attempt to move this layer to the bottom interface to modify the RS and ferroelectric switching behaviors. To realize this goal, the device is set to the P_{up} state and then annealed at 250 °C for 60 min in air. After this treatment, the device remains largely in HRS in the negative voltage region, while it exhibits noticeable HRS $\rightarrow$ LRS switching in the positive voltage region [see Fig. S7(a) within the Supplemental Material [31]]. In addition, the P-V hysteresis loop exhibits an apparent positive voltage offset [Fig. S7(b) within the Supplemental Material [31]], suggesting that the direction of E_{imp} is reversed. These results can be well explained by the movement of O-V toward the bottom interface in the P_{up} state at high temperature (notably, O-V can become more mobile at high temperature [30,37]).

Taking into account the abovementioned polarization and defective layer, the energy-band diagrams can be established and used to illustrate the mechanism for the observed one-side diode-type RS behavior. Figure S8 within the Supplemental Material [31] reveals that our BFO film is a p-type semiconductor, probably owing to Bi loss [30]. Note that, although O-V can induce electron doping in the BFO film, O-V may accumulate mainly near the film surface, while the bulk region may still be dominated by Bi vacancies. Therefore, the BFO film can

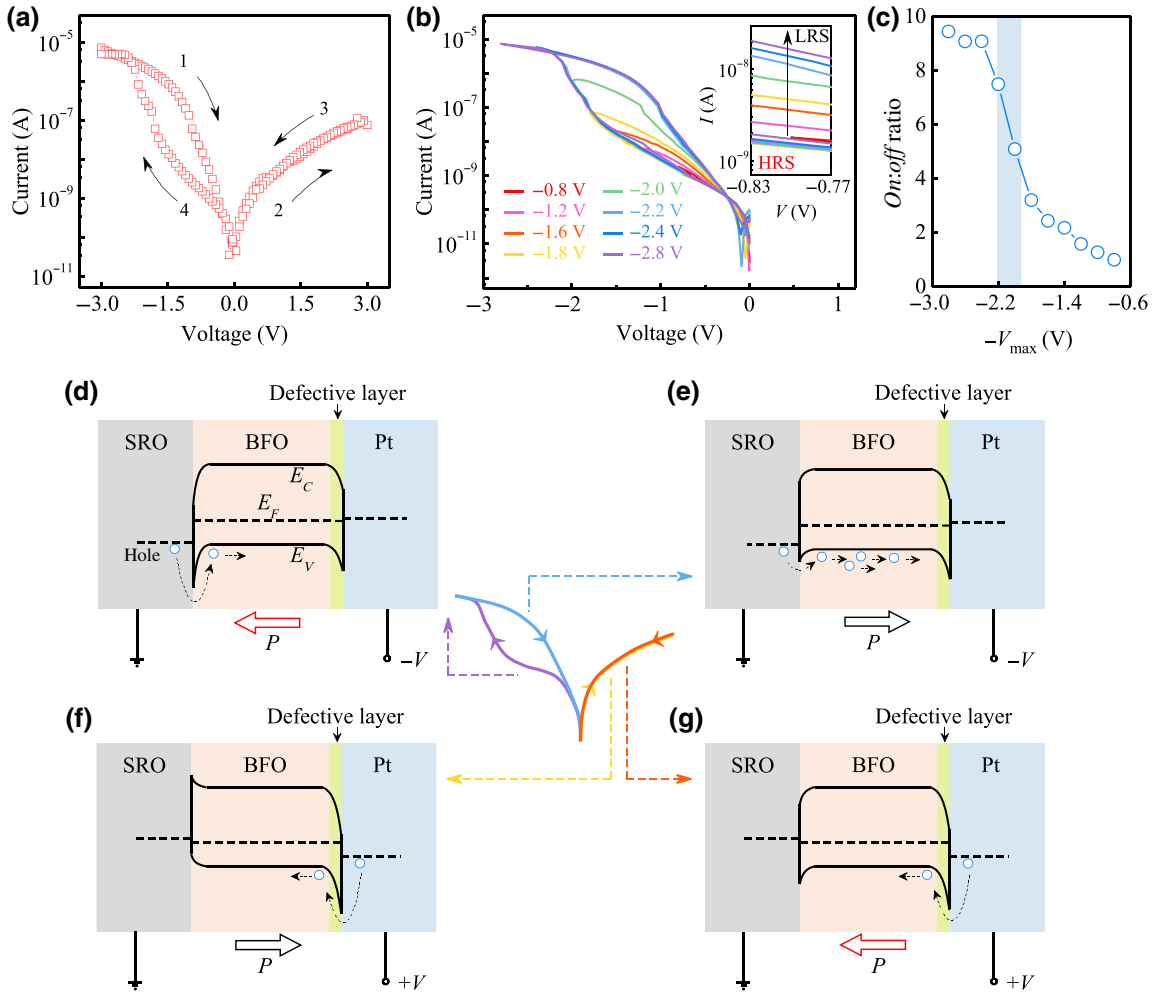

FIG. 2. RS behavior in the Pt/BFO/SRO device. (a) Typical I-V characteristics measured with a voltage sweep of $-3\ \text{V} \rightarrow 0 \rightarrow +3\ \text{V} \rightarrow 0 \rightarrow -3\ \text{V}$. (b) Different I-V curves measured by applying voltage sweeps of $0 \rightarrow -V_{\text{max}} \rightarrow 0$ ($-V_{\text{max}}$ varies from -0.8 to -2.8 V) to the device in the initial HRS. (c) *On*:*off* ratio as a function of $-V_{\text{max}}$. Schematic diagrams showing the energy-band diagrams and conduction processes of the device (d) under a small negative voltage in the P_{down} state, (e) under a small negative voltage in the P_{up} state, (f) under a small positive voltage in the P_{up} state, and (g) under a small positive voltage in the P_{down} state. (d)–(g) correspond to steps 4, 1, 2, and 3 in (a), respectively.

exhibit p-type characteristics, despite the existence of O-V. In addition, BFO typically has an electron affinity of about 3.3 eV and a band gap of about 2.7 eV [29,38], while Pt and SRO have work functions of about 5.3 and 5.2 eV, respectively. Based on these parameters, p-type Schottky barriers may be formed at both Pt/BFO and BFO/SRO interfaces. The barrier height (Φ_B) can be further tuned by polarization, i.e., Φ_B can be increased (reduced) when the polarization is pointed to (away from) this barrier. However, the polarization charge may be screened by the charges in the defective layer [39]; hence, polarization may be unable to modulate Φ_B at the interface where a defective layer is located.

When the device in the initial P_{down} state is subjected to a small negative voltage, the reverse-bias barrier at the BFO/SRO interface limits hole injection [Fig. 2(d)]. The high Φ_B caused by the positive polarization charge at this interface results in a low current, accounting for the observed HRS [Fig. 2(a)]. When the negative voltage becomes sufficiently large, polarization switching occurs [Fig. 2(e)]. The negative polarization charge at the BFO/SRO interface lowers Φ_B, thus leading to HRS $\rightarrow$ LRS switching [Fig. 2(a)]. The proposed RS mechanism is validated by the good agreement between the critical voltages for RS and polarization switching [Figs. 2(c) and S3(b) within the Supplemental Material [31]], and it can be further supported by fitting of the conduction behavior. Figure S9 within the Supplemental Material [31] shows that the I-V curves in the P_{down} and P_{up} states can be fitted to the interfacial Schottky emission model, and the fitted Φ_B value at the BFO/SRO interface is reduced by 0.12 eV when down-to-up polarization

switching occurs. The fitting results support that RS in the negative voltage region originates from the polarization modulation of Φ_B.

As the applied voltage changes to positive, hole injection occurs at the Pt/BFO barrier, which is reversely biased. Due to the defective layer, Φ_B at the Pt/BFO interface remains high, regardless of the polarization direction [Figs. 2(f) and 2(g)], as mentioned earlier. In addition, the defective layer may trap holes, further suppressing hole transport. Therefore, the device remains HRS in the positive voltage region and no RS occurs [Fig. 2(a)].

C. Conductance decay

The previous section shows the one-side diode-type RS behavior in the Pt/BFO/SRO device and reveals its mechanism, i.e., polarization modulation of Φ_B induces HRS $\rightarrow$ LRS switching in the negative voltage region, while the defective layer causes the persistence of HRS in the positive voltage region. Also recall from Sec. III A that there is polarization relaxation in the P_{up} state. Combining polarization-controlled RS and polarization relaxation, it is expected that the device in the P_{up} state (i.e., LRS in the negative voltage region) can exhibit spontaneous conductance decay.

To demonstrate this, repeated voltage sweeps of $0 \rightarrow -3\ \text{V} \rightarrow 0$ with different delay periods between two sweeps [inset in Fig. 3(a)] are applied to the device in the initial P_{down} state, and the resulting I-V characteristics are recorded. Immediately after application of the $0 \rightarrow -3$ V sweep, the device is set to the P_{up} state (see evidence in Fig. S10 within the Supplemental Material [31]). Figures 3(a) and 3(b) show that the I-V curve measured during the $-3\ \text{V} \rightarrow 0$ sweep remains almost unchanged for different cycles, confirming that almost the same P_{up} state and LRS are realized before each $-3\ \text{V} \rightarrow 0$ sweep through the application of the $0 \rightarrow -3$ V sweep. However, the $0 \rightarrow -3$ V sweep produces an I-V curve with a lower current level than that measured during the previous $-3\ \text{V} \rightarrow 0$ sweep, even for the zero delay period between these two sweeps. This suggests that conductance decay occurs during the $-3\ \text{V} \rightarrow 0$ sweep and/or the delay period. Moreover, the I-V curve measured during the $0 \rightarrow -3$ V sweep gradually shifts to a lower current level as the delay period becomes longer [see Fig. 3(b)]. This demonstrates that conductance decay becomes more significant with a prolonged delay period. Recall that the device in the P_{up} state also exhibits polarization relaxation [Fig. 1(e)]. It is thus natural to correlate conductance decay with polarization relaxation.

To further confirm this correlation, the retention behavior of the Pt/BFO/SRO device is directly investigated. The device is preset in an intermediate state close to LRS by applying a $0 \rightarrow -3\ \text{V} \rightarrow 0$ sweep followed by a waiting time of 3 min. It is then written by the -3-V (50-ms) pulse, so that the back-switched polarization can be aligned upward again and the resistance state can be brought closer to LRS. Right after this, the conductance of the device is monitored with a small read voltage of -1 V (notably, all the read voltages mentioned hereafter are around -1 V, unless otherwise specified). This small read voltage is unable to cause any RS [Fig. 2(b)], and it is only applied when needed. Figure 3(c) shows that the conductance decays from 26.1 to 16.4 nS during the retention time of 840 s. Because our device exhibits polarization-controlled Schottky emission in the negative voltage region (Fig. S9 in the Supplemental Material [31]), conductance decay is likely to originate from polarization relaxation, which increases the barrier height (Φ_B) over time. More specifically, when the device is read in the negative voltage region, the barrier at the BFO/SRO interface limits conduction. In the initial P_{up} state, the negative polarization charge at the BFO/SRO interface causes a low Φ_B at this interface and, consequently, a high conductance [Fig. 3(e)]. However, as time goes by, some upward polarization gets relaxed under the effect of the downward E_{imp}. Therefore, Φ_B at the BFO/SRO interface gradually increases [Fig. 3(f)], leading to conductance decay. If the proposed mechanism was true, the following relationship between the time-dependent polarization [$P(t)$], barrier height [$\Phi_B(t)$], and conductance [$G(t)$] should be obeyed, according to the polarization-controlled Schottky emission model [40,41]:

$$\ln(G(t)) \sim -\,\Phi_B(t) \sim P(t)^{1/2}. \tag{2}$$

Figure 3(d) shows the plot of $\ln(G(t))$ versus $P(t)^{1/2}$, where $G(t)$ and $P(t)$ data are taken from Figs. 3(c) and 1(e), respectively. It is seen that the $\ln(G(t))$-$P(t)^{1/2}$ relationship exhibits good linearity, thus validating the proposed mechanism, i.e., the polarization-relaxation-induced increase in Φ_B causes conductance decay.

Although several previous studies on ferroelectric second-order memristors already observed conductance decay and attributed its origin to polarization relaxation, the correlation between conductance decay and polarization relaxation was not rigorously demonstrated because of the lack of polarization data (see detailed reasons in Sec. I). However, our Pt/BFO/SRO FD allows direct polarization measurement (Fig. 1). Combining $G(t)$ and $P(t)$ data, we demonstrate that conductance decay is quantitatively correlated with polarization relaxation [Fig. 3(d)]. Our study therefore unambiguously identifies polarization relaxation as the origin of conductance decay.

Note that polarization relaxation itself can generate a capacitive current. However, such a capacitive current is estimated to be only about 1.5 pA, which is 4 orders of magnitude lower than the average current measured in the retention test [$\sim$20 nA, as deducible from Fig. 3(c)]. This confirms that the current measured in the retention test is

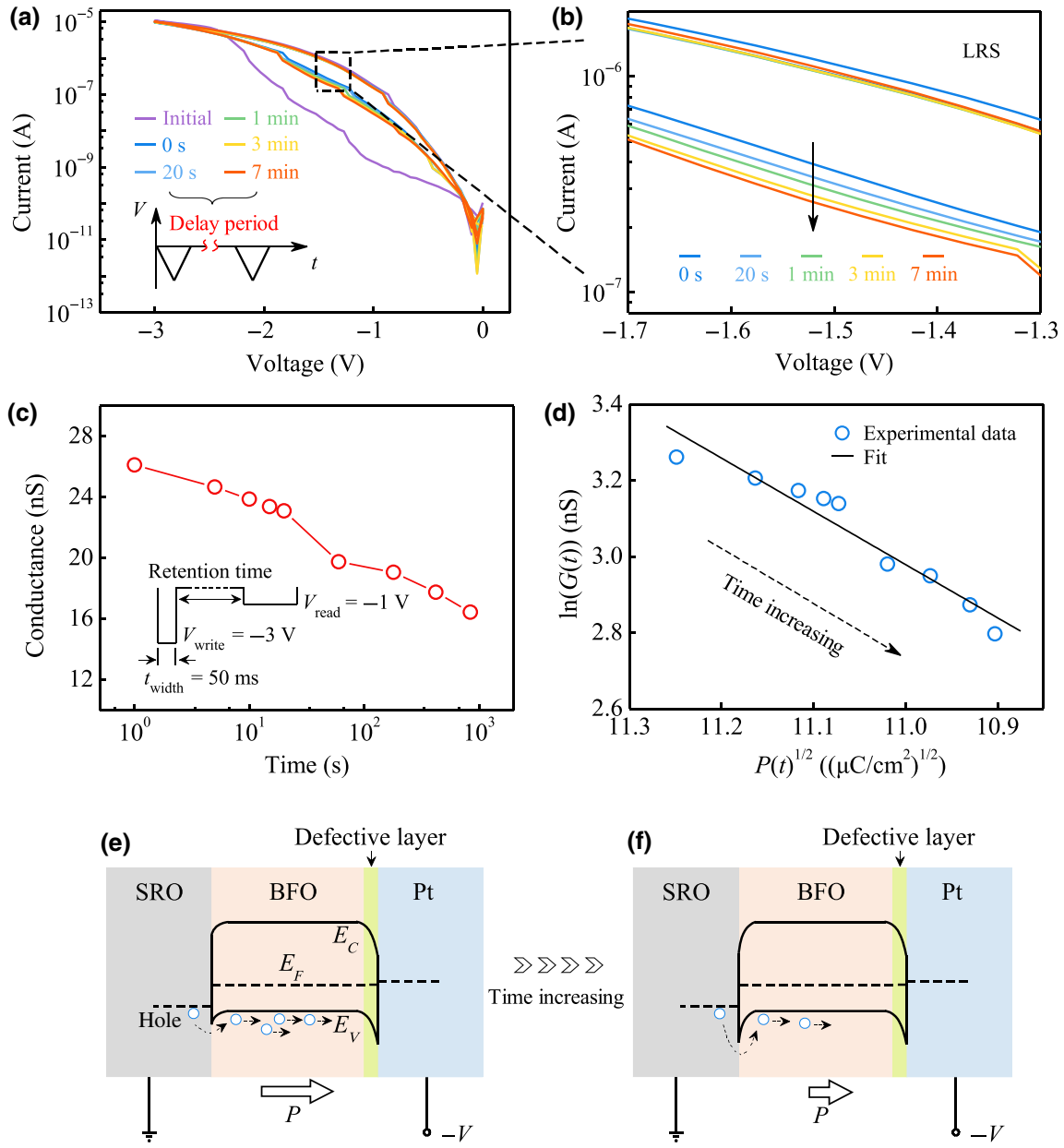

FIG. 3. Conductance decay behavior in the Pt/BFO/SRO device. (a) Different *I*-*V* curves measured for the device in the initial P_{down} state by applying repeated voltage sweeps of $0 \rightarrow -3\ V \rightarrow 0$ with different delay periods between two sweeps. Inset shows the schematics of the voltage waveform applied in the *I*-*V* measurement. (b) Enlarged view of the *I*-*V* curves in (a), except the one measured with the initial $0 \rightarrow -3\ V \rightarrow 0$ sweep [labeled as "Initial" in (a)]. (c) Conductance decay behavior of the device in the P_{up} state. (d) Plot of the $\ln(G(t))$-$P(t)^{1/2}$ relationship and its fit using Eq. (2). Schematic diagrams showing the energy-band diagrams and conduction processes of the device in the P_{up} state (e) before and (f) after relaxation.

mainly the conductive current, which can reflect the conductance appropriately. Also note that ion migration can be excluded as the major origin of conductance decay, as demonstrated in Fig. S11 within the Supplemental Material [31].

D. Emulation of synaptic functions

The polarization-relaxation-induced conductance decay, as demonstrated in the previous section, qualifies our Pt/BFO/SRO FD as a second-order memristor and enables it to emulate various synaptic functions. For a biological synapse, the synaptic weight is modified by the Ca^{2+} concentration rather than directly by the spike [6]. When a spike arrives at the presynaptic terminal, the Ca^{2+} influx is activated, which causes the release of neurotransmitters and thereby enhances the synaptic weight. After the spike, the Ca^{2+} concentration spontaneously decays over time, allowing the synaptic weight to return to its

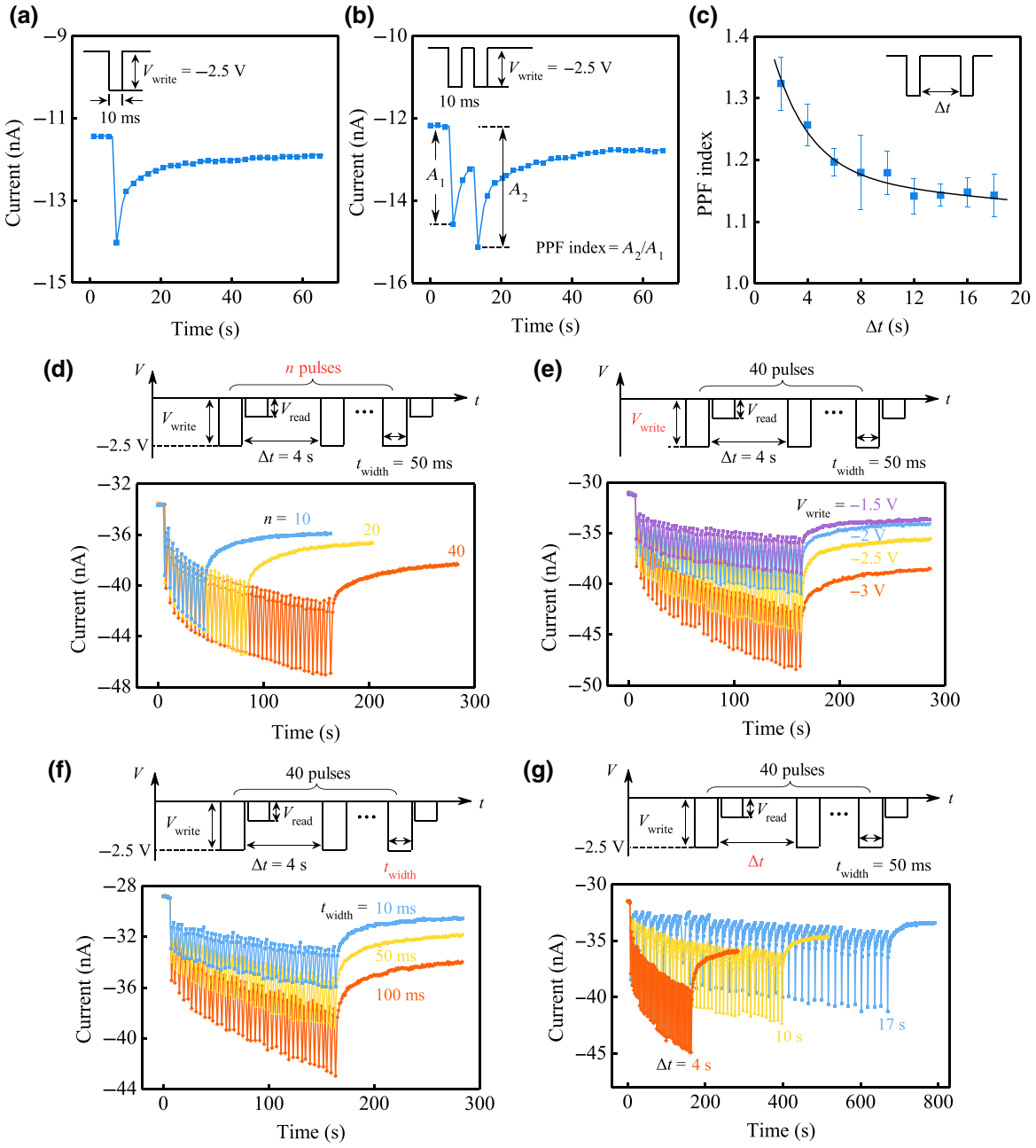

FIG. 4. Emulation of EPSC, PPF, and STP-to-LTP transition. (a) EPSC in response to a −2.5 V (10 ms) pulse. (b) PPF characteristics stimulated by a pair of −2.5 V (10 ms) pulses. (c) PPF index (η) as a function of pulse interval (Δt). EPSCs under repeated pulses with different (d) numbers, (e) amplitudes, (f) widths, and (g) frequencies (i.e., the reciprocal of Δt). Insets in (a)–(c) and upper panels in (d)–(g) show the schematics of the applied pulses.

initial value. This provides an internal timing mechanism for the biological synapse, which is key to the realization of STP. Similar to the Ca^{2+} concentration in the biological synapse, polarization in our Pt/BFO/SRO FD exhibits short-term dynamics and it directly influences the conductance (i.e., the synaptic weight). Therefore, our FD is promising for the emulation of various synaptic functions in which STP is indispensable.

The first STP-based function to be implemented with our FD is the EPSC, which depicts a transient current flow into the postsynaptic neuron upon spike stimulation. The device is preset in an intermediate state close to LRS by applying a $0 \rightarrow -3\ \text{V} \rightarrow 0$ sweep followed by a waiting time of 3 min (notably, hereafter in all the synaptic measurements, the device is always preset in this intermediate state, unless otherwise specified. This intermediate state is relatively stable, as demonstrated in Fig. S12 within the

Supplemental Material [31]). Then, a voltage pulse (amplitude, −2.5 V; width, 10 ms) is applied to the device and its current response is read out. Figure 4(a) shows that the current rises abruptly to a peak right after the pulse and then decays over time, mimicking the EPSC in a biological excitatory synapse. As revealed in Sec. III C, the current rise and decay can be attributed to barrier-height modulations by polarization switching and relaxation, respectively. Figure S13 within the Supplemental Material [31] further shows that the current peak becomes higher as the pulse amplitude and width increase. This is explained by the fact that more back-switched polarization is aligned upward again upon the application of a negative pulse with larger amplitude and width, causing a more significant lowering of the barrier height and, consequently, a higher current peak.

PPF is a STP-based function that is important for decoding temporal information, such as visual and auditory signals [42,43]. It refers to a phenomenon where the second spike evokes a higher EPSC than the first spike when these two spikes are applied in close succession. Moreover, the EPSC enhancement depends on the interval between the two spikes. The PPF behavior is investigated in the Pt/BFO/SRO FD by applying two successive identical pulses at different intervals. Figure 4(b) shows the EPSCs triggered by two –2.5-V (10-ms) pulses with an interval of 6 s. It is clearly seen that the second EPSC is higher than the first one. To quantify the EPSC enhancement, the ratio between the relative peak height of the second EPSC (A_2) and that of the first one (A_1) is defined as the PPF index (η). Figure 4(c) presents a plot of η against the pulse interval (Δt), revealing that η decreases with increasing Δt. At shorter Δt, less polarization is back-switched during the interval, while more upward polarization is attained right after the second pulse, thereby causing a lower barrier height and, consequently, a higher A_2. Moreover, as shown in Fig. 4(c), decay of η with Δt follows a double-exponential function:

$$\eta = 1 + C_1 \exp\left(-\frac{\Delta t}{\tau_1}\right) + C_2 \exp\left(-\frac{\Delta t}{\tau_2}\right), \qquad (3)$$

where C_i and τ_i are the initial facilitation magnitude and time constant, respectively, and $i = 1$ and 2 correspond to the rapid and slow relaxation processes, respectively. The fitted value of τ_2 (i.e., 72.2 s) is at least 1 order of magnitude larger than that of τ_1 (i.e., 2.8 s), consistent with the rule found in biological synapses [44].

When stimulating a biological synapse repeatedly, the temporary change in synaptic weight (i.e., STP) can be transformed into a more persistent one (i.e., LTP). Such a STP-to-LTP transition in a biological synapse originates from Ca^{2+} remaining inside the postsynaptic membrane [8,45]. To emulate the STP-to-LTP transition, repeated pulses with different numbers, amplitudes, widths, and frequencies are applied to the Pt/BFO/SRO FD, and the temporal current responses are read out. As shown in Figs. 4(d)–4(g), although the current decays after pulse stimulation, it gradually becomes stabilized at a certain intermediate level. Moreover, the stabilized current level becomes higher with increasing pulse number, amplitude, width, and frequency, indicative of the transition from STP to LTP. The STP-to-LTP transition in our device may be attributed to the following two effects under repeated negative pulses: (i) more back-switched polarization is aligned upward again, and the domain walls may be moved to more energetically favorable sites [46]; and (ii) more electrons may be injected and trapped at the Pt/BFO interface, reducing E_{imp} originating from the positively charged O-V [47]. Both effects lead to enhanced stability of upward polarization, and the stability enhancement becomes more significant with increasing pulse number, amplitude, width, and frequency. Consequently, the conductance in LRS becomes more persistent and the STP-to-LTP transition is thus realized.

With the capability of exhibiting the STP-to-LTP transition, the Pt/BFO/SRO FD can further emulate the learning experience of a biological brain. As illustrated in Fig. 5(a), the device is first stimulated with 35 identical pulses (amplitude, –2.5 V; width, 50 ms) and then undergoes a 240-s period without any pulse stimulation. The read current gradually increases to a peak value of about –44.3 nA and then decays to about –35.6 nA, originating from barrier-height modulations by polarization switching and relaxation, respectively. Such a current rise and decay correspond well with the learning and forgetting processes, respectively. Afterward, the device is stimulated with –2.5-V (50-ms) pulses again. It is seen that recovering the current to its peak value needs only 4 pulses, much fewer than those used to reach the same current level in the first learning stage. This resembles the phenomenon that relearning is much easier than learning something for the first time [48]. Why this can be realized by our device may be because down-to-up polarization switching is easier during the relearning stage due to the domain walls moving to more energetically favorable locations and a reduced E_{imp} (see explanations of the STP-to-LTP transition for details). Moreover, the stabilized current level in the second decay stage becomes higher than that in the first decay stage, which can be explained by the enhanced stability of upward polarization, as described earlier for the STP-to-LTP transition. The enhancement in the stabilized current level is analogous to the phenomenon that memory stability is strengthened by relearning. These results demonstrate that the learning experience of a biological brain is successfully imitated by the Pt/BFO/SRO FD.

Associative learning is a more complex type of learning, where the biological brain learns to associate things together. One of the most representative examples of

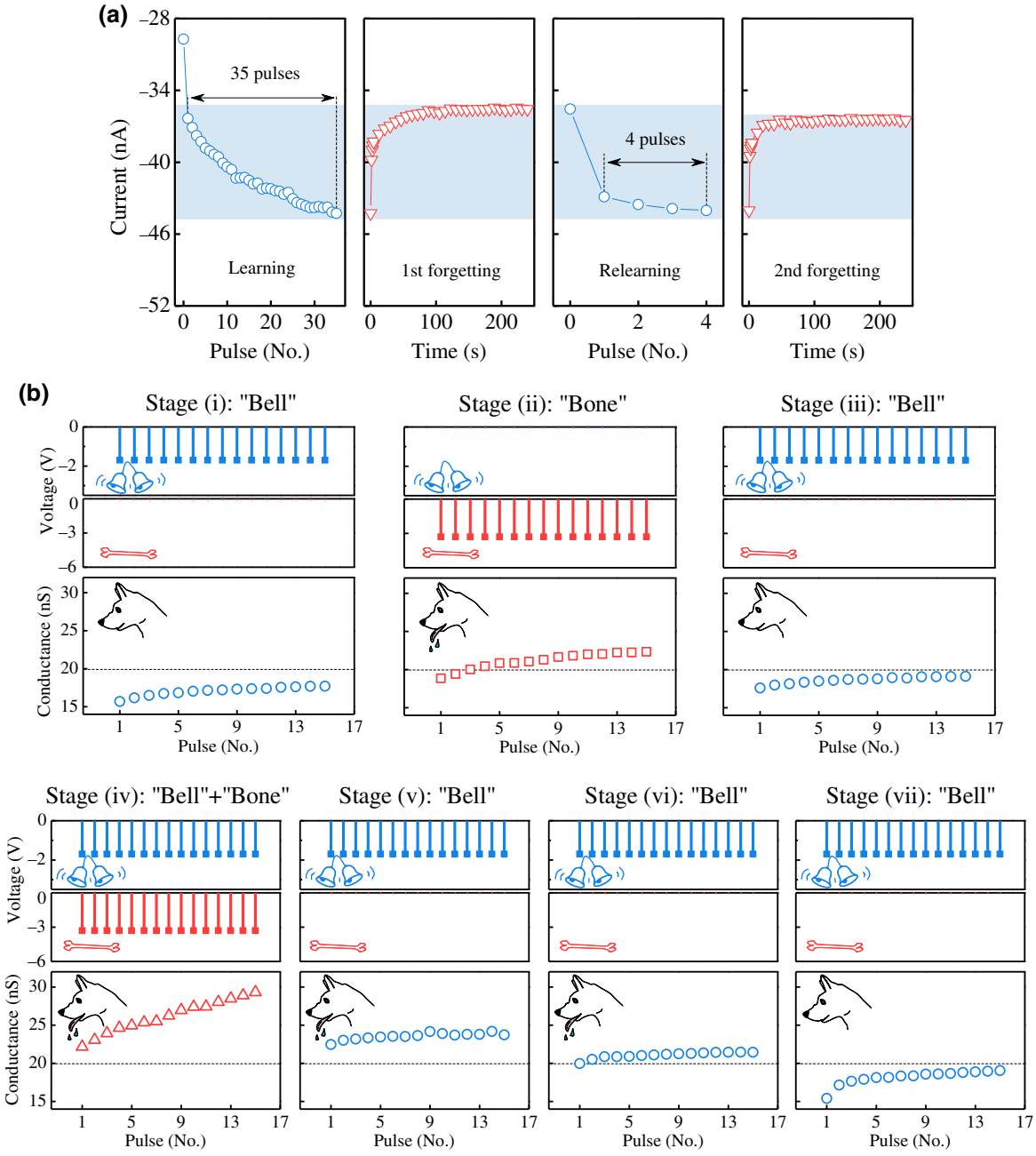

FIG. 5. Emulation of learning experience and associative learning. (a) Learning-experience characteristics consisting of four stages: learning [under 35 −2.5-V (50-ms) pulses], forgetting (without pulse stimulation), relearning [under 4 −2.5-V (50-ms) pulses], and forgetting (without pulse stimulation). (b) Associative learning demonstrated with Pavlov's dog experiment, where the "bone" and "bell" stimuli are simulated by −3.3- (50-) and −1.7-V (50-ms) pulses, respectively.

associative learning is the Pavlov dog experiment, which can be implemented with our Pt/BFO/SRO FD. Here, an unconditioned stimulus ("feeding with a bone") is simulated by a –3.3-V (50-ms) pulse, while a conditioned stimulus ("ringing the bell") is simulated by a –1.7-V (50-ms) pulse. When the device's read current exceeds a threshold value of 20 nA, the dog's salivation is considered to occur. As seen from Fig. 5(b), when the "bell" stimuli are applied alone [stage (i)], the current is well below the threshold value. By contrast, applying only the "bone" stimuli can enhance the current to above the threshold value, thus triggering "salivation" [stage (ii)]. After the bone stimuli, the bell stimuli are applied again, which are still insufficient to allow the current to reach the threshold value [stage (iii)]. Then, both bone and bell stimuli are applied simultaneously to simulate the training

process, during which the "dog" is conditioned to associate the bone and bell stimuli [stage (iv)]. Shortly after training, salivation can be induced by the bell stimuli alone [stage (v)]. The reason for this is because the overlapping pulses during training have large amplitudes and can thus result in a LRS with high stability, enabling subsequent low-amplitude pulses to trigger relatively high currents. However, the conditioned response becomes weaker gradually [stage (vi)] and eventually the bell stimuli alone cannot induce salivation [stage (vii)]. This is analogous to forgetting the association, which is attributed to polarization relaxation and associated conductance decay. These results demonstrate that our device successfully emulates the associative learning exemplified by the Pavlov dog experiment.

As seen above, polarization relaxation plays an important role in the emulation of all the above synaptic functions. Specifically, the STP and the forgetting effect are realized by polarization relaxation. Modulating polarization relaxation along with polarization switching by applying repeated pulses can realize the STP-to-LTP transition and enhanced memory stability. This also suggests that more complex synaptic functions, such as spike-timing-dependent plasticity, can be implemented with the FD (see Fig. S14 within the Supplemental Material [31]). Therefore, our Pt/BFO/SRO FD is capable of faithfully emulating biological synaptic behavior.

IV. CONCLUSION

We develop a Pt/BFO/SRO FD that shows not only RS behavior but also allows direct polarization measurement. The device exhibits well-shaped P-V hysteresis loops with a negative voltage offset, suggesting the existence of a downward E_{imp}. Additionally, polarization relaxation is observed in the P_{up} state, which is attributed to the downward E_{imp} that induces back-switching of upward polarization. On the other hand, the device exhibits one-diode-type RS behavior, where HRS $\rightarrow$ LRS switching occurs in the negative voltage region, while the HRS is persistent in the positive voltage region. It is revealed that HRS $\rightarrow$ LRS switching may originate from down-to-up polarization switching that reduces the barrier height at the BFO/SRO interface, while the persistence of HRS may be caused by a O-V-rich defective layer (this layer may also be the origin of downward E_{imp}). Moreover, the device exhibits a conductance decay in LRS, and its correlation with polarization relaxation is quantitatively evidenced. It is thus confirmed that polarization relaxation induces conductance decay. Using polarization relaxation as an internal timing mechanism, our device functions as a second-order memristor and emulates various synaptic functions where STP is indispensable, including EPSC, PPF, the STP-to-LTP transition, learning experience, and associative learning. This study reveals not only a polarization-dominated internal timing mechanism in the FD-based second-order memristor, but also demonstrates that such a device is promising for mimicking biological synapses.

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