Performance Limit of Gate-All-Around Si Nanowire Field-Effect Transistors: An *Ab Initio* Quantum Transport Simulation

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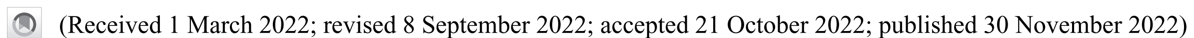

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The gate-all-around (GAA) Si nanowire (NW) field-effect transistor (FET) is considered one of the most promising successors of the current mainstream Si fin FET (FinFET) owing to its better electrostatic gate control. Experimentally, the diameter of Si NWs has been scaled down to 1 nm. In this paper, the performance limit of the GAA Si NWFET with a 1-nm diameter is investigated by utilizing *ab initio* quantum transport simulations. We prove that the electrical conduction is concentrated in the core of the ultranarrow wire channel. The minimum gate length (L_g) at which the *n*- and *p*-type GAA Si NWFET can satisfy the high-performance application requirements (*on*-state current, gate capacitance, delay time, and power dissipation) of the International Technology Roadmap for Semiconductors is 3 nm. The best-performing 5-nm-L_g *n*-type GAA Si NWFET exhibits an energy-delay product comparable with typical monolayer two-dimensional FETs. Compared with the similar-sized trigate Si NW FinFET, an approximately 200% increase in the *on*-state current and about 15% decrease in the subthreshold swing are witnessed in GAA Si NWFET at the same 5-nm L_g. Through strain engineering, about an 80% increase of *on*-state current is observed in the 5-nm-L_g *p*-type GAA Si NWFET. Our research demonstrates the vast potential of the GAA Si NWFET in the sub-3-nm gate-length region.

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I. INTRODUCTION

With the current mainstream Si fin field-effect transistor (FinFET) technologies approaching their ultimate size, Si gate-all-around (GAA) nanowire (NW) FETs have received considerable attention recently because of their better electrostatic gate control restraining the short-channel effects and their natural compatibility with the state-of-the-art CMOS fabrication process [1–7]. Moreover, compared with two-dimensional (2D) and three-dimensional semiconductors, ballistic transport can be more easily realized in such a one-dimensional (1D) channel because backscattering happens only in the transport direction [8,9]. Hence 1D semiconductors have a larger mean free path and carrier mobility [10]. For example, the carrier mobility of the room-temperature semiconducting 1D carbon nanotube (CNT) can reach 100 000 cm^2 V^{-1} s^{-1} [11], much higher than those of room-temperature 2D semiconductors [2D black phosphorene (BP) has the highest mobility, about 1000 cm^2 V^{-1} s^{-1}, among the 2D semiconductors] [12].

Experimentally, several sub-10-nm gate-length Si NWFETs have been fabricated. The record high *on*-state current (I_{on}) of 3740 μA/μm (diameter-normalized) is achieved in the GAA Si NWFET with a diameter (D_{NW}) of 10 nm and gate length (L_g) of 8 nm [13,14]. This reported I_{on} dramatically exceeds the required I_{on} (1330 μA/μm) for 8-nm-L_g high-performance (HP) applications, according to the strict International Technology Roadmap for Semiconductors (ITRS) 2013 edition [15]. As L_g scales down to 5 nm, the I_{on} of the fabricated Si NWFET with D_{NW}= 8 nm decreases to 802 μA/μm (diameter-normalized) [16]. This I_{on} value almost touches the required I_{on} (900 μA/μm) for the 5-nm-L_g HP applications of ITRS 2013 [15] and

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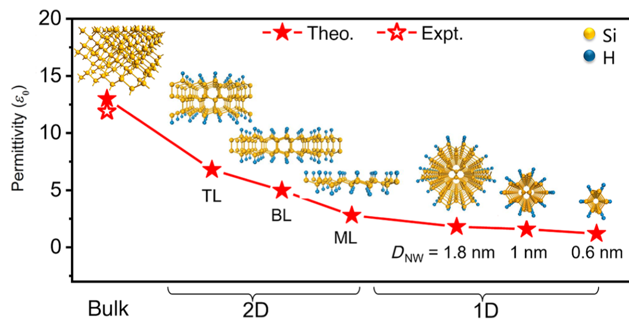

FIG. 1. Permittivity as a function of the dimension of the Si structures, from bulk Si to 2D ML silicane and finally the 1D Si NW (D_{NW} = 1 nm).

is superior to the fabricated 5-nm-L_g Si FinFET, whose I_{on} is 497 μA/μm and normalized by 2 times fin height (H_{fin}) plus fin width (W_{fin}) [17,18]. Natural length λ $\left(\sqrt{\alpha(\varepsilon_{ch}/\varepsilon_{ox})T_{ch}T_{ox}}\right)$ characterizes the penetration depth of the source and drain electrical potential into the channel, where α depicts the gate structure and is equal to 1, 1/2, 1/3, and 1/4 for the single-gate (SG), double-gate (DG), trigate (TG), and GAA devices, respectively. $\varepsilon_{ox}(T_{ox})$ and $\varepsilon_{ch}(T_{ch})$ represent the electrical permittivity (thickness) of the gate dielectric and channel, respectively [19]. A thinner and lower dimension channel gives rise to a smaller ε_{ch} due to the reduced screening of the electron-electron interaction [20–22]. For instance, the calculated ε_{ch} decreases from 13.0ε_0 (the experimental value is 11.9ε_0) to 2.8ε_0 and finally 1.58ε_0 as the structure changes from bulk Si to 2D monolayer (ML) silicane, and finally the 1D Si NW ($D_{NW} \sim 1$ nm), as shown in Fig. 1. Since a smaller T_{ch} and ε_{ch} lead to smaller λ and better gate electrostatics, further improvement of the sub-5-nm-L_g GAA Si NWFET performance is anticipated by reducing the diameter of the NW.

Many efforts have been invested in developing thinner Si NW fabrication [14,23,24]. Remarkably, by adopting HF treatment, Lee *et al.* have successfully produced Si NWs with a diameter approaching 1 nm [25]. Such a Si NW is hydrogen passivated and exhibits a greater antioxidant capacity than regular silicon wafer surfaces and stays stable in the air [25]. Two questions arise naturally: what is the device performance limit for the GAA Si NWFETs with 1-nm D_{NW}, and to what scale will Moore's law continue in such a device design? Several semiempirical simulations about the GAA ultrathin Si NWFET have been reported previously [26–28]. For example, the GAA 5-nm-D_{NW} Si NWFET with $L_g = 10$ nm has been investigated by the **k·p** model and nonequilibrium Green's function (NEGF) method [26]. The device performance of the GAA 2-nm-D_{NW} Si NWFET with $L_g = 10$ nm has been compared with that of the InAs NW counterpart by the semiclassical ballistic transport model [28]. However, the semiclassical model will lead to large errors for the sub-10-nm devices [29–31]. For example, a subthreshold slope of the 9-nm CNT channel calculated by the numerical simulation is almost triple the experimental value [31]. The reason lies in the parameter-dependent transition matrix element [29]. Moreover, the ultrashort channel devices could not be understood by a model that mainly concentrates on the channel segment [31]. The investigation of a sub-5-nm L_g ultrathin Si NWFET with D_{NW}= 1 nm is still absent.

Here, based on accurate *ab initio* quantum transport simulations, the performance limit of the ideal GAA Si NWFET with a 1-nm D_{NW} is predicted. Remarkably, according to the calculated *on*-state current (I_{on}), delay time (τ), power dissipation (PDP), and energy-delay product (EDP), both the *n*- and *p*-type GAA Si NWFETs can satisfy the ITRS 2013 [15] HP applications' requirements even as L_g downscales to 3 nm. The EDP of the 5-nm-L_g GAA Si NWFET is comparable with those of typical monolayer 2D FETs, such as ML tellurene [32], ML Bi_2O_2Se [33], and ML BP FETs [34]. Besides, at $L_g = 5$ nm, the optimized *n*-type GAA Si NWFET outperforms its TG NW FinFET [35] ($W_{fin} \sim 0.8$ nm) and ML silicane MOSFET [29] ($T_{ch} \sim 0.37$ nm) counterparts in terms of a 200% increase in I_{on}. Inspired by the strain-enhanced performance of the planar MOSFET, we also investigate the influence of uniaxial stress [from −1% (compression) to +1% (tension)] on GAA Si NWFET. Regarding the 5-nm-L_g GAA Si NWFET, the *n*-doped device only benefits from the tensile strain, with an increase of nearly 40% in I_{on} at +1% strain, while the *p*-doped device benefits from both compressive and tensile strain, with about 60% and 80% enhancement in I_{on} at −1% and +1% strain, respectively. Hence, in this respect, we show that GAA Si NWFET provides vast potential for future transistors at the sub-3-nm gate length.

II. COMPUTATIONAL DETAILS

As a kind of logic device, the *on-off* switch of a FET is modulated by the gate electrostatics. Driven by the external gate and bias voltage, the carriers flow from the source to drain through the channel, and the device is in a nonequilibrium state. A two-probe device configuration is built to simulate the quantum transport of the GAA Si NWFET, as shown in Fig. 2(a). The Si NW channel has a D_{NW} of 1 nm and direction along ⟨110⟩ [36–38]. The left and right electrodes are semi-infinite and symmetrically doped. The gate dielectric adopts the widely used SiO_2. The underlapped (UL) structures (between the gate and the electrode) are adopted to improve device performance. By weakening the source and drain's influence on the channel, UL structures can help to reduce the leakage current. However, UL also increases the uncovered channel area beyond the gate control. Therefore, there should be a trade-off at the UL length.

The transport properties are calculated via density-functional theory (DFT) coupled with the NEGF method

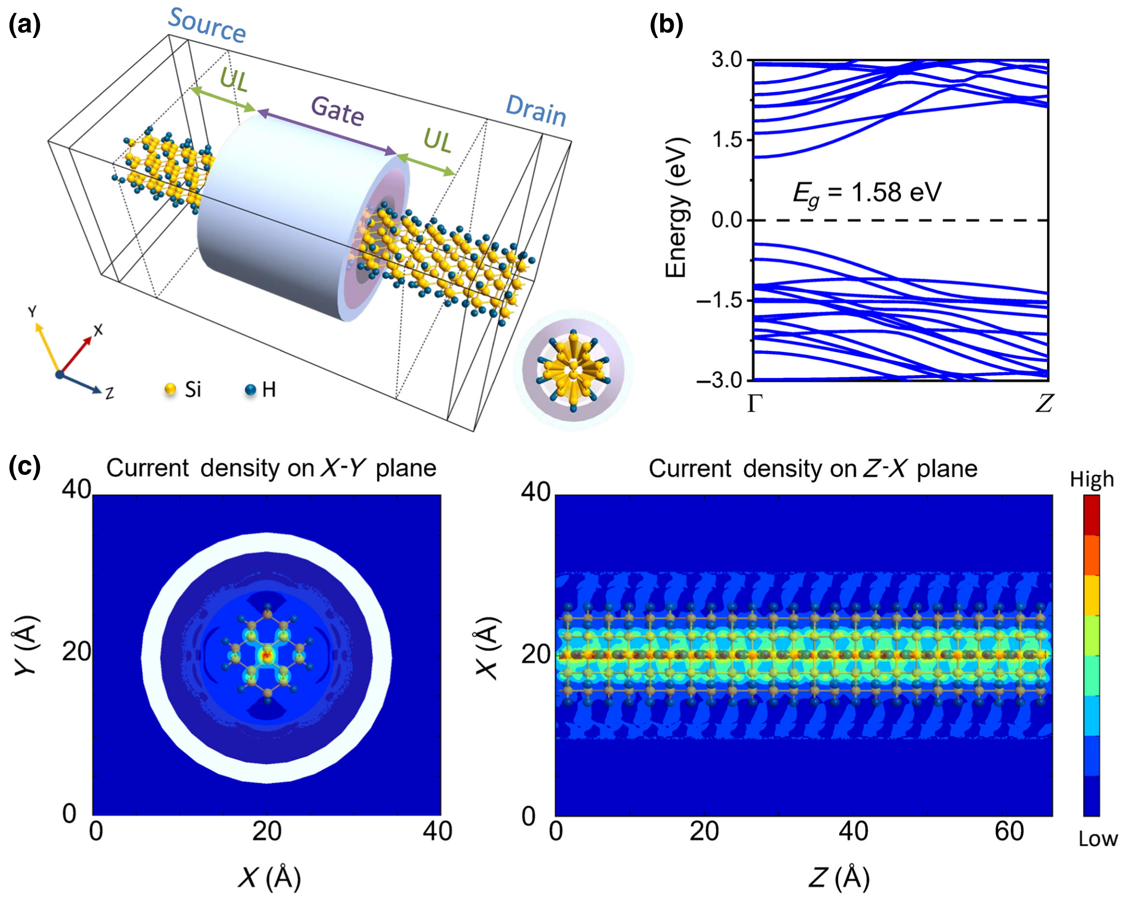

FIG. 2. (a) Perspective view of the GAA Si NWFET with the NW (direction ⟨1 1 0⟩, D_{NW} of 1 nm) passivated by hydrogen. (b) Band structure of the 1D Si NW channel. (c) Current density on the X-Y and Z-X planes.

implemented in the Atomistix ToolKit 2018 package [39, 40]. The X and Y directions of the device take Neumann boundary conditions. The transport Z direction takes a Dirichlet-type boundary condition. During the electron density calculation, the device is separated into the central region (including the extension region) and electrode region. Self-energies $\sum_{l(r),k_{||}}$ depict the influence of the left (right) electrodes on the scattering region, calculated from the electrode Hamiltonians and coupling Hamiltonians [$k_{||}$ is a reciprocal lattice vector point along a surface-parallel direction (orthogonal to the transmission direction) in the irreducible Brillouin zone (IBZ)]. The retarded Green's function matrix for the central region is generated from the central region Hamiltonian matrix H and overlap matrix S with the inclusion of the electrode self-energies,

$$G_{k_{||}}(E) = \left[(E + i\delta_+)S_{k_{||}}(E) - H_{k_{||}}(E) - \sum_{l,k_{||}}(E) - \sum_{r,k_{||}}(E)\right]^{-1}, \tag{1}$$

where δ_+ is an infinitesimal positive number.

The k-dependent and E-dependent transmission coefficient $T_{k_{||}}(E)$ over the IBZ can be obtained by

$$T_{k_{||}}(E) = \text{Tr}[\Gamma^l_{k_{||}}(E)G_{k_{||}}(E)\Gamma^r_{k_{||}}(E)G^\dagger_{k_{||}}(E)], \tag{2}$$

where $G_{k_{||}}(E)$ and $G^\dagger_{k_{||}}(E)$ are the retarded and advanced Green's functions, respectively, obtained from the NEGF method and $\Gamma^{l(r)}_{k_{||}}(E) = i\left(\sum_{l(r),k_{||}}(E) - \sum^\dagger_{l(r),k_{||}}(E)\right)$ is the level broadening originating from the left (right) electrode in the form of self-energy $\sum_{l(r),k_{||}}(E)$. The transmission function $T(E)$ is the average of the transmission coefficient over the IBZ.

The Landauer-Büttiker formula is adopted to calculate the current from source to drain (Ids),

$$I_{\text{ds}} = \frac{2e}{h}\int_{-\infty}^{+\infty}[f(E-\mu_D) - f(E-\mu_S)]T(E)\,dE, \tag{3}$$

where f is the Fermi-Dirac distribution function and $\mu_{S(D)}$ is the Fermi level of the source (drain) electrode. The generalized gradient approximation (GGA) to

the exchange-correlation functional of the Perdew-Burke-Ernzerhof (PBE) form is adopted throughout the device calculation [41,42]. Normconserving PseudoDojo pseudopotentials with a medium basis set, kinetic-energy cutoff energy of 50 Ha, and temperature of 300 K are set. It should be noted that the used approach accounts for ballistic transport. There are two reasons for adopting such a transport method in the considered system. First, the sub-10-nm channel length is much smaller than the mean free path of carriers (hundreds of angstroms) in the channel, which means carriers have a high probability of completing source-drain transport before scattering occurs. For instance, the calculated ballistic transport efficiency of ML MoS_2 FETs is greater than 76% when the channel length is less than 10 nm [43]. Second, the simulated channel has a perfect channel structure, where carriers will not suffer from the scattering of defects and impurities. Thus, the research tends to give the ideal ballistic limit prediction [44,45].

The GGA method always underestimates the band gap of intrinsic 2D and 1D materials, and the *GW* method provides more reliable predictions for the band gap because the many-body effects are considered. However, the band gap of the 2D and 1D materials will be renormalized to the GGA level approximately in the ultrathin FETs due to two factors. First, the dielectric layer in the ultrathin transistors significantly screens the electron-electron interaction in the ultrathin channel [46]. For example, the band gap of ML MoS_2 at the *GW* level is reduced to 1.9 eV in the FET environment with high-κ_E HfO dielectric, consistent with the band gap of 1.76 eV calculated by DFT GGA [47]. Second, when the FETs work, the heavy doping in the channel significantly screens the electron-electron interaction. For example, the band gap of the heavily doped ML $MoSe_2$ is renormalized to 1.59 eV, matching well with 1.52 eV of the GGA PBE method and the value of 1.58 eV measured by angle-resolved photoelectron spectroscopy [48–50]. Therefore, the GGA method is accurate enough to describe the band gap for ultrathin transistors. For example, the measured experimental transport gaps of the ML, bilayer (BL), and trilayer black phosphorene FETs are 0.99, 0.71, and 0.61 eV, respectively, which are consistent with those of 0.79, 0.81, and 0.68 eV at the GGA level, respectively [51–54].

So far, the DFT NEGF method has proved its applicability and feasibility in investigating the quantum transport properties of 1D CNT and 2D WSe_2 FETs. The calculated transfer characteristics, I_{on}, τ, and PDP of the 1D CNT FET ($L_g = 5$ nm) are comparable with the observed ones [55,56]. Besides, the maximum I_{on} of the p-type ML WSe_2 MOSFET with channel length of 9 nm is predicted to be 1500 μA/μm in the ballistic transport limit at $V_{ds} = 0.64$ V [57], in agreement with the measured value of 1360 μA/μm at $V_{ds} = 0.8$ V in the fabricated 20-nm-channel-length BL WSe_2 FET [58].

Compared with the newly updated International Roadmap for Devices and Systems (IRDS) 2020 [59], which has been amended to be less rigorous (the smallest $L_g = 12$ nm) due to slow industrial development, the ITRS 2013 standards [15] (the smallest $L_g = 5$ nm) are stricter and more suitable for our sub-10-nm-L_g GAA Si NWFET performance evaluation. Therefore, the adopted criterion "ITRS" in the following refers specifically to the ITRS 2013 edition.

III. RESULTS

A. *On*-state current

The outermost dangling bonds of the investigated 1-nm diameter Si NW are passivated by hydrogen atoms to avoid carrier mobility degradation deriving from the trap state [60]. This Si NW has a 1.58-eV direct band gap (Γ point) at the DFT GGA PBE level [Fig. 2(b)], matching well with the previous calculation [36,60,61]. The corresponding electron and hole effective masses for the whole Si NW channel are 0.127 and 0.152 m_0, respectively. Based on the ITRS table [15], the supply voltage (V_{dd}) of 0.64 V is adopted for the transfer characteristic's calculation of the sub-5-nm-L_g GAA Si NWFET. There are two current normalization methods for NWFET: the perimeter (peri) normalization and the diameter (dia) normalization of the cross section [27,61]. Generally, peri normalization is adopted for the thicker wire ($D_{NW} > 10$ nm), and dia normalization is adopted for the narrower wire ($D_{NW} < 10$ nm) because the electrical conduction remains at the surface and in the inner core for thick and narrow wires, respectively [62]. Such a diameter-dependent current distribution for the narrow wire can be explained by the simple model of a particle confined in an infinite cylindrical potential well. The standing wave solution is zero at the boundary. The boundary weight rises as D_{NW} decreases. Therefore, the carriers of the narrower wires are less likely to appear on the surface but more concentrated in the core [27,61]. We calculate the current density on the X-Y and Z-X plane of the 1-nm-diameter Si NW and show the result in Fig. 2(c). From this figure, it can be seen the current is concentrated in the core of this ultranarrow Si NW. Thus, dia normalization is adopted for the current of this GAA Si NWFET throughout the paper unless otherwise specified [37].

The *off*-state current (I_{off}) for the HP and low-power (LP) applications is set to 0.1 μA/μm (I_{off}^{HP}) and 5×10^{-5} μA/μm (I_{off}^{LP}), respectively, according to the ITRS [15]. The gate voltage where the I_{off} occurs is defined as the *off*-state gate voltage ($V_{off}^{HP\ (LP)}$). The *on*-state gate voltage ($V_{on}^{HP\ (LP)}$) is generated by $V_{on}^{HP\ (LP)} = V_{off}^{HP\ (LP)} + V_{dd}$, and then the *on*-state current ($I_{on}^{HP\ (LP)}$) can be evaluated. The doping method in the atomistic model is the atomic compensation charge method [21,29,63], and the optimal

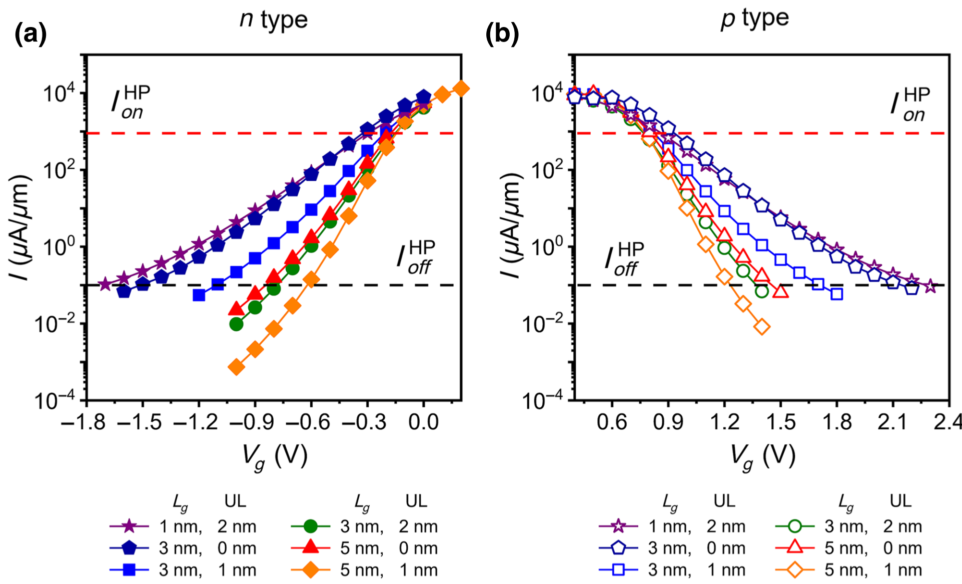

FIG. 3. (a),(b) Transfer characteristics for the n- and p-type GAA Si NWFETs at different L_g and L_{UL}, respectively, under $V_{bias}=0.64$ V. The red and blue dashed lines represent I_{on} and I_{off} required by the ITRS 2013 for HP devices, respectively.

electron and hole concentration of 3×10^{19} cm^{-3} is chosen for the n- and p-type source and drain doping (see Fig. S2 in the Supplemental Material for details [64]). The effective mass m^* of the Si NWs remains unchanged after being heavily doped because the shape of band structures is almost unchanged by the doping concentration and doping type (see Fig. S1 in the Supplemental Material for details [64]). It is a pity that all the simulated GAA Si NWFETs struggle to achieve the ITRS [15] LP *off* state (5×10^{-5} μA/μm) within the investigated gate voltage range. Therefore, Si NW is not suitable for LP devices, and only HP standards are considered in this paper.

The transfer characteristics of the sub-5-nm-L_g GAA Si NWFET are shown in Figs. 3(a) (n-type) and 3(b) (p-type), respectively. I_{on} can be extracted from the transfer characteristics. I_{on} is significant for judging the device's performance. A high I_{on} benefits from a distinguished *on*:*off* ratio and a fast *on*-*off* switch, thus is especially favored by HP devices. The standard I_{on} of the ITRS [15] HP goal is 900 μA/μm at $L_g=5$ nm. Among all the devices on display, the GAA Si NWFET with $L_g=1$ nm performs the worst; the n- and p-type devices show an I_{on} of only 3 μA/μm even with UL = 2 nm. At $L_g=3$ nm without UL, there is no significant improvement in I_{on} (8.3 and 5 μA/μm for the n- and p-type, respectively). After introducing the 1-nm UL, I_{on} values of 54 and 56 μA/μm are obtained for the n- and p-type devices, respectively. Although the I_{on} at this level is still far from the HP goal of 900 μA/μm, the nearly an order of magnitude increase in I_{on} compared with a UL = 0 device indicates a promising improvement plan by increasing UL length. Subsequent results have confirmed this plan. The device performance boosts the n- and p-type I_{on} up to 1239 and 1642 μA/μm at $L_g=3$ nm and UL = 2 nm, exceeding the HP requirement. At $L_g=5$ nm, UL's effect on promoting I_{on} is more significant. As UL increases from 0 to 1 nm, the I_{on} of the n-type (p-type) device rises from 666 (973) to 5854 (6125) μA/μm. To sum up, the minimum gate length at which the UL-optimized GAA Si NWFET can meet the I_{on} of the ITRS [15] HP standard is 3 nm. Detailed data can be found in Table I.

For comparison, the calculated HP I_{on} of typical UL-optimized sub-5-nm advanced silicon transistors TG Si NW FinFET ($W_{fin}\sim0.8$ nm) [35], DG ML silicane FET ($T_{ch}\sim0.37$ nm) [29], and GAA Si NWFET with both dia and peri normalization are shown in Fig. 4(a) (see Tables II and S1 in the Supplemental Material for detail [64]). The black dashed line in Fig. 4(a) represents the ITRS [15] HP sub-5-nm-L_g standard (900 μA/μm), and devices whose I_{on} exceeds this value are desirable. All the data are obtained from the *ab initio* quantum transport simulations. Here, adopting the same SiO_2 dielectric oxide layer ($T_{ox}=0.4$ nm, $\varepsilon_{ox}=3.9\varepsilon_0$), the TG Si NW FinFET has a calculated $\lambda=0.25$ nm ($\alpha=1/3$, $T_{ch}=W_{fin}=0.8$ nm, $\varepsilon_{ch}=1.44\varepsilon_0$), and its current is normalized by $2\times H_{fin}+W_{fin}$; ML silicane FET, the thinnest silicon-based device, has a calculated $\lambda=0.23$ nm ($\alpha=1/2$, $T_{ch}=0.37$ nm, $\varepsilon_{ch}=2.8\varepsilon_0$) and its current is normalized by width; GAA Si NWFET has a calculated $\lambda=0.20$ nm ($\alpha=1/4$, $T_{ch}=D_{NW}=1$ nm, $\varepsilon_{ch}=1.58\varepsilon_0$). At $L_g=5$ and 3 nm, it is evident that the I_{on} of the GAA Si NWFET is much larger than those of the other two devices, irrespective of the current normalization approach. The calculated ultimate gate lengths to fulfill the ITRS [15] HP I_{on} standard of the TG Si NW FinFET [35] and ML silicane FET [29] are both 5 nm. Remarkably, both the dia- and peri-normalized current approaches reveal an ultimate L_g of 3 nm for the UL-optimized GAA Si NWFET, even though the peri-normalized I_{on} [n-type (p-type), 948 (1136) μA/μm] is slightly smaller than the dia-normalized

TABLE I. Benchmarking the ballistic performance of the n-type and p-type GAA Si NWFETs against the ITRS 2013 requirements for HP transistors of the following decades. L_g, the gate length; L_{UL}, the length of the underlapped area; SS, the subthreshold swing; g_m, the transconductance; I_{on}, the *on*-state current; I_{off}, the *off*-state current; C_t, the total capacitance; τ, the delay time; PDP, the power dissipation.

	L_g (nm)	L_{UL} (nm)	SS (mV/dec)	g_m (mS/μm)	I_{on} (μA/μm)	I_{off} (μA/μm)	C_t (fF/μm)	τ (ps)	PDP (fJ/μm)
n-type	5	0	145	5.2	666	0.1	0.45	0.436	0.186
		1	109	31.3	5854	0.1	0.47	0.051	0.193
	3	0	250	0.1	8.3	0.1	0.32	25.221	0.129
		1	189	0.7	54	0.1	0.19	2.201	0.076
		2	144	12.5	1239	0.1	0.25	0.127	0.100
	1	2	292	0.02	3	0.1	0.13	27.457	0.053
p-type	5	0	138	7.6	973	0.1	0.64	0.423	0.263
		1	104	35.1	6125	0.1	0.54	0.056	0.221
	3	0	240	0.03	5	0.1	0.37	46.902	0.151
		1	177	0.7	56	0.1	0.23	2.671	0.096
		2	134	9.5	1642	0.1	0.26	0.103	0.108
	1	2	277	0.01	3	0.1	0.12	25.316	0.049
ITRS HP 2028 Horizon [15]	5.1				900	0.1	0.60	0.423	0.24

one [n-type (p- type), 1239 (1642) μA/μm]. As L_g downscales to 1 nm, all three devices fall short of the ITRS [15] HP I_{on} standard. Above all, the GAA Si NWFET is superior to the other Si-based devices regarding the *on*:*off* ratio.

The transconductance g_m of the UL-optimized GAA Si NWFET (both dia and peri normalization) is considered. Transconductance shows the gate control on the drain current in the superthreshold region using the equation $g_m = dI_{ds}/dV_g$. The higher g_m always corresponds to a higher I_{on}. When L_g is scaled down from 5 to 1 nm, the UL-optimized g_m of both the dia- and peri-normalized Si NWFETs with D_{NW}= 1 nm generally decreases [Fig. 4(b)]. In particular, the g_m of both the n- and p-type Si NWFETs in the dia normalization are generally higher than those of the peri-normalized counterparts at a given L_g (e.g., 31.3 vs 14.5 mS/μm for the n-type and 35.1 vs 19.7 mS/μm for the p-type when L_g is 5 nm). Moreover, g_m of the n-type dia-normalized GAA Si NWFET with $D_{NW} = 1$ nm is much higher (31.3 mS/μm) than that of the fabricated TG counterpart with $D_{NW} = 8$ nm (3.5 mS/μm) when L_g is 5 nm, as shown in Fig. 4(b) [16]. The main reason is that the GAA Si NWFET with $D_{NW} = 1$ nm has a shorter λ than that of the TG counterpart with $D_{NW} = 8$ nm in terms of the

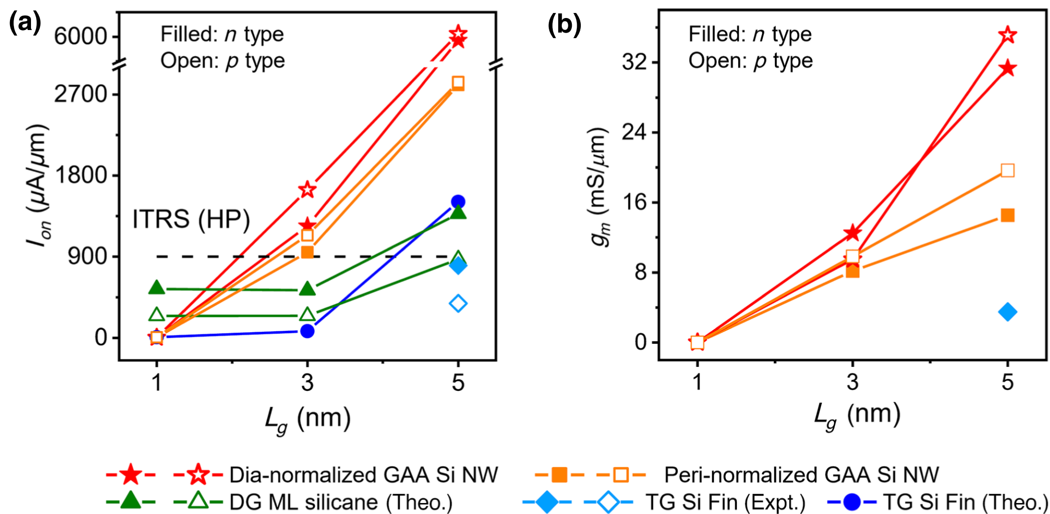

FIG. 4. (a) *On* current comparison among the dia-normalized and peri-normalized GAA Si NWFET, simulated DG ML silicane MOSFET (width normalization), ultrathin ($W_{fin} \sim 0.8$ nm) TG Si NW FinFET (normalized by $2 \times H_{fin} + W_{fin}$) in the simulation, and dia-normalized ($W_{fin} \sim 8$ nm) TG Si NW FinFET in the experiment [16]. The black dashed line represents I_{on} required by the ITRS 2013 for HP devices. (b) Transconductance g_m versus L_g of the UL-optimized GAA Si NWFET (both dia and peri normalization).

TABLE II. Performance comparison among the UL-optimized sub-5-nm-L_g GAA Si NWFETs, DG ML silicane MOSFET, and TG Si NW FinFET. SS, the subthreshold swing; I_{on}, the *on*-state current; C_t, the total capacitance; τ, the delay time; PDP, the power dissipation. The data of the TG Si NW FinFET and DG ML silicane MOSFET are obtained from Refs. [29,35].

L_g (nm)		n- or p-type	SS (mV/dec)	I_{on} (μA/μm)	C_t (fF/μm)	τ (ps)	PDP (fJ/μm)
5 nm	GAA Si NWFET	n-type	109	5854	0.47	0.051	0.193
		p-type	104	6125	0.54	0.056	0.221
	TG Si NW FinFET	n-type	128	1510	0.13	0.055	0.053
	DG ML silicane MOSFET	n-type	65	1374	0.086	0.042	0.037
		p-type	67	871	0.099	0.075	0.043
3 nm	GAA Si NWFET	n-type	144	1239	0.25	0.127	0.1
		p-type	134	1642	0.26	0.103	0.108
	TG Si NW FinFET	n-type	216	74.1	0.06	0.544	0.026
	DG ML silicane MOSFET	n-type	77	527	0.039	0.047	0.016
		p-type	81	244	0.042	0.11	0.017
1 nm	GAA Si NWFET	n-type	292	3	0.13	27.457	0.053
		p-type	277	3	0.12	25.316	0.049
	TG Si NW FinFET	n-type	315	7.8	0.02	1.447	0.007
	DG ML silicane MOSFET	n-type	129	541	0.02	0.024	0.008
		p-type	126	243	0.02	0.051	0.008

equation $\lambda = \sqrt{\alpha(\varepsilon_{ch}/\varepsilon_{ox})T_{ch}T_{ox}}$. The gate structure factor α, T_{ch}, T_{ox}, and ε_{ch} of the former are all smaller than those of the latter (1/4 vs 1/3 for α, 1 vs 8 nm for T_{ch}, 0.4 vs 3.6 nm for T_{ox}, and ε_{ch} becomes smaller with the thinning T_{ch}) [16]. Moreover, the simulated FET has a perfect channel structure, and carriers will not suffer from the scattering of defects and impurities. Therefore, the corresponding g_m represents the theoretical limit value, always higher than that of the experimental counterpart.

B. UL's work mechanism

Note that UL plays a critical role in promoting the I_{on} of the simulated sub-5-nm GAA Si NWFETs. To clarify UL's work mechanism in this system, the local device density of states (LDDOS) and spectrum current density of the n-type 3-nm-L_g GAA Si NWFETs are plotted [Figs. 5(a)–5(c)]. The LDDOS reflects the device's real-space DOS distribution as a function of position along the transport direction. The spectrum current $\tilde{I}$ reflects the energy-distributed current density, which contains two parts: the tunneling spectrum current ($\tilde{I}_{tunnel}$) and thermionic spectrum current ($\tilde{I}_{therm}$). $\tilde{I}_{tunnel}$ and $\tilde{I}_{therm}$ can be distinguished by the activation energy Φ_B on the energy axis. The activation energy Φ_B is the energy difference between the drain and channel. The *off* -state [left panel of Fig. 5(d)] prefers a large Φ_B so that the leakage is suppressed, while the *on*-state [right panel of Fig. 5(d)] prefers a small Φ_B so that I_{on} can be large enough. Gating ability is the ability to regulate Φ_B. According to the ITRS standard [15], V_{dd} of the sub-5-nm device is 0.64 V.

When the n-type GAA Si NWFET with $L_g = 3$ nm is in the *off* -state, all spectrum currents in different UL cases result entirely from the tunneling currents, as shown in Figs. 5(a)–5(c). The tunneling current I_{tunnel} ($\propto e^{-w\sqrt{m^*\Phi_B}}$, where w is the barrier width) is reduced with increasing w, m^*, and Φ_B. In particular, w could be lengthened by the UL structure because the source and drain-to-channel coupling is decreased [45,65]. Therefore, I_{tunnel} could be reduced by the UL structure. The *off* -state current is fixed to 0.1 μA/μm in terms of the ITRS. To realize the same *off* -current when UL and w increase, the Φ_B controlled by the gate is required to be smaller. As shown in Figs. 5(a)–5(c), Φ_B is 0.81, 0.57, and 0.39 eV in the 0-, 1-, and 2-nm-UL cases, respectively. When the FET is in the *on*-state, Φ_B is still getting smaller with the help of the UL. Φ_B in the 0-, 1-, and 2-nm-UL cases are 0.25, 0.06, and –0.30 eV, respectively. However, Φ_B might be increased with the continuously lengthening UL because the overlong UL will weaken the gate control [21,34]. In the *on*-state, $\tilde{I}_{therm}$ is gradually introduced into the current contribution by introducing the UL, and $\tilde{I}_{tunnel}$ is reduced. Finally, $\tilde{I}$ comes entirely from $\tilde{I}_{therm}$, and $\tilde{I}_{tunnel}$ vanishes in the 2-nm-UL case [Fig. 5(c)]. Here, the peak $\tilde{I}$ in the 2-nm-UL case is nearly 70 times larger than that of the device without UL (35 vs 0.5 μA/eV), leading to a higher I_{on} (1239 vs 8.3 μA/μm).

C. Subthreshold swing and total capacitance

Several other figures of merit (FOMs), such as subthreshold swing (SS), total capacitance C_t, delay time τ, and PDP, also need to be considered during the device performance evaluation. These key FOMs for the best-performing sub-5-nm GAA Si NWFETs are listed in Table I and shown in Fig. 6. The FOMs for the sub-5-nm TG Si NW FinFETs [35] and DG ML silicane FETs [29] are also plotted for comparison, and the detailed data can be found in Table II.

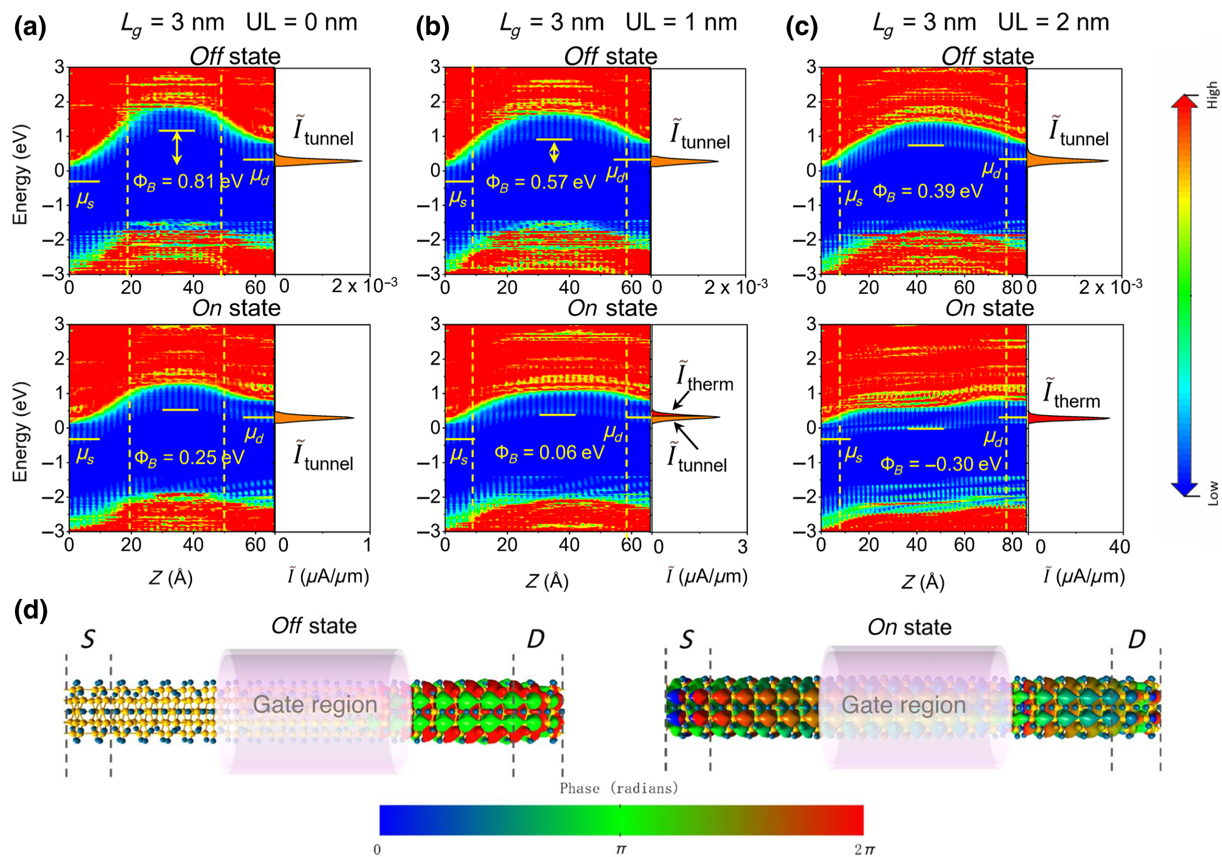

FIG. 5. Local device density of states and spectrum current of the GAA Si NWFET at $L_g = 3$ nm and UL = 0 nm (a), 1 nm (b), and 2 nm (c) under V_{dd}= 0.64 V. The region on the left (right) of the yellow dashed lines represents the source (drain) region, including the scattering region. The Fermi level is set to −0.32 and 0.32 eV for the source (μ_s) and drain (μ_d), respectively. Φ_B is the effective barrier height for electrons of the distribution tail at the conduction-band minimum (CBM) transporting from the drain to the source. $\tilde{I}_{tunnel}$ and $\tilde{I}_{therm}$ represent the tunneling spectrum current and the thermionic spectrum current, respectively. (d) The transmission eigenstates of *on* (left panel) and *off* (right panel) states at $E = 0.32$ eV and $\boldsymbol{k} = (0, 0)$. The iso value is 0.02 au. The phase color scale is shown under the plot.

SS is used to quantitatively describe the gating capability of transistors in the subthreshold region. It is numerically equal to the incremental gate voltage ΔV_g required to change the drain current I_{ds} by one order of magnitude ($SS = \partial V_g/\partial \log I_{ds}$). The smaller the SS, the stronger the gate control and the faster the *on-off* switch. According to the "Boltzmann tyranny," the SS of the conventional MOSFET has a thermionic limit of 60 mV/dec at room temperature [1]. Because of the similar subthreshold swing region, the two normalization methods give the same SS. As shown in Fig. 6(a), SS generally decreases with increasing L_g. The *n*- and *p*-type GAA Si NWFETs share a similar downward trend of SS [*n* (*p*), 292 (277) to 144 (134) to 109 (104) mV/dec] as L_g increases from 1 to 3 to 5 nm, and the *p*-type devices perform slightly better with a slightly smaller SS than the *n*-type devices. At the same L_g, DG ML silicane MOSFETs [29] always perform best due to their better gate regulation (SS in the range of 65–129 mV/dec) from the thinnest channel. In contrast, TG Si NW FinFETs perform worst. The relatively weak gating ability of the TG Si NW FinFET [35] (SS in the range of 128–315 mV/dec) arises from the thicker channel width (about 0.8 nm) than ML silicane (0.37 nm) and insufficient TG wrapping (3/4 of the channel surface) compared with the GAA structure (the whole channel surface).

The total capacitance C_t of the transistor dominates the channel charge and discharge process in an *on-off* switch. The smaller the C_t, the higher the transistor switching frequency. C_t contains two parts: One is gate capacitance C_g, the capacitance of the gate terminal of a FET. C_g can be calculated by $C_g = \partial Q_{ch}/\partial V_g$ in which Q_{ch} is the charge of the channel under the gate. The other is fringing capacitance C_f, caused by the edge effect of the gate electric field. According to the ITRS [15] 5-nm-device standard, C_f equals $2C_g$. As shown in Fig. 6(b) and Table I, the C_t of the sub-5-nm-L_g optimized *n*-type (*p*-type) GAA Si NWFETs is 0.13 (0.12) to 0.47 (0.54) fF/μm by dia normalization, meeting the ITRS [15] HP standard C_t range

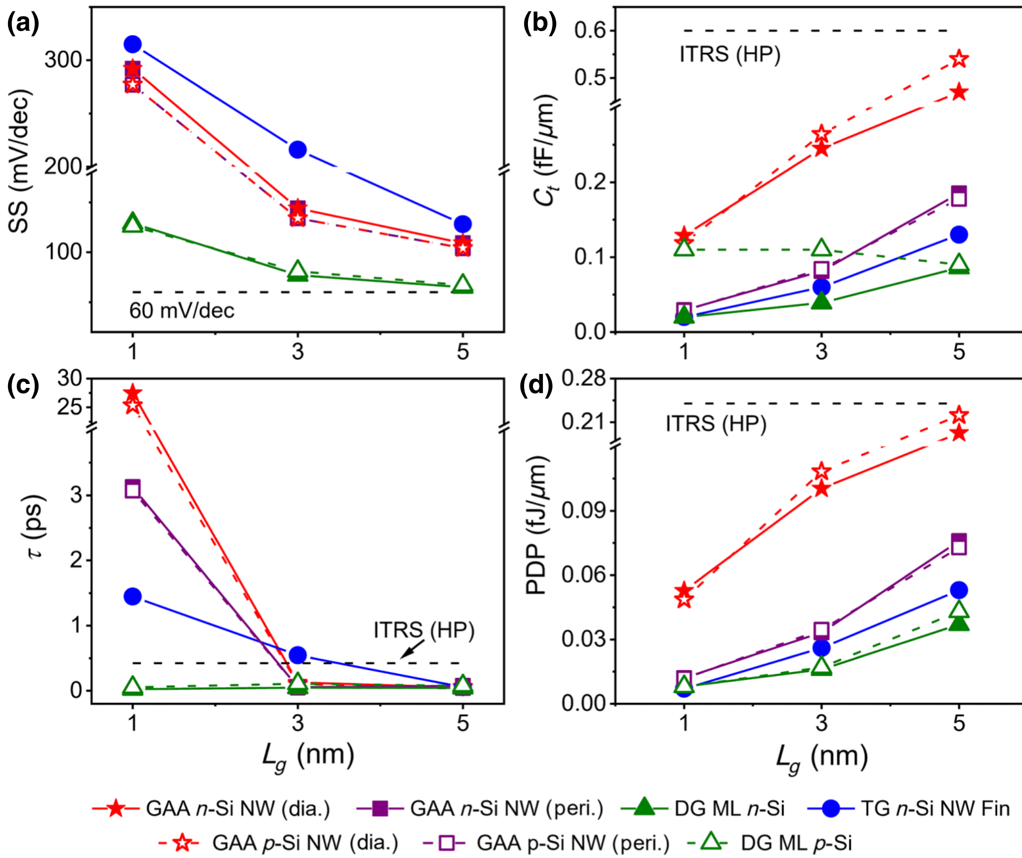

FIG. 6. (a) Calculated subthreshold swing, (b) total gate capacitance, (c) intrinsic delay time, and (d) power dissipation as functions of the gate length in the UL-optimized GAA Si NWFET (dia and peri normalization), TG Si NW FinFET [35], and DG ML silicane MOSFET [29] under $V_{\rm bias} = 0.64$ V. The black dashed lines are the ITRS 2013 HP requirements for corresponding parameters.

(<0.6 fF/μm). When peri normalization is adopted, C_t is significantly decreased to 0.03 (0.03) to 0.19 (0.18) fF/μm for the n-type (p-type) devices, comparable with those of the TG Si NW FinFET [35] (n-type, 0.02–0.13 fF/μm). Because the capacitance of an isolated conductor is only related to its geometric characteristics (size and shape), the comparable C_t between the GAA Si NWFET and TG Si NW FinFET [35] is reasonable as they have similar channel volumes (the cross-section area is around 0.8 nm^2) at the same L_g. The DG ML silicane MOSFET [29] has the smallest C_t [n (p), 0.02 (0.02) to 0.086 (0.099) fF/μm] due to it having the smallest channel volume (the channel cross-section area is around 0.4 nm^2).

D. Delay time and power consumption

The delay time τ is the time for a transistor to complete an *on-off* switch. It can be generated by the precalculated I_{on} and C_t using $\tau = C_t V_{\rm dd}/I_{on}$. C_t and I_{on} are calculated in our work, and $V_{\rm dd}$ is fixed to 0.64 V in terms of the ITRS. A small C_t and a large I_{on} imply a small τ and high-speed switching. $\tau < 0.423$ ps is required for sub-5-nm-L_g devices, according to the ITRS [15] HP application standard. As shown in Fig. 6(c), both the n- and p-type GAA Si NWFETs at $L_g = 5$ nm are desirable, with $\tau = 0.051$ and $\tau = 0.056$ ps, respectively, and comparable with those of the TG Si NW FinFET [35] (n, $\tau = 0.055$ ps) and ML silicane MOSFETs [n (p), $\tau = 0.042$ (0.075) ps] [29]. The fast switch for the GAA Si NWFETs mainly derives from their very large $I_{\rm on}$ even though their C_t is not small enough. At $L_g = 3$ nm, the n-type TG Si NW FinFET [35] ($\tau = 0.544$ ps) fails to meet the τ standard mainly because of a small $I_{\rm on}$, while the τ of the GAA Si NWFETs [n (p), $\tau = 0.127$ (0.103) ps] and ML silicane MOSFETs [29] [n (p), $\tau = 0.047$ (0.11) ps] are still within the ITRS [15] HP range. Downscaling to $L_g = 1$ nm, a drastic decline in $I_{\rm on}$ of the n- and p-type GAA Si NWFETs causes $\tau > 25$ ps, larger than the ITRS [15] standard ($\tau = 0.423$ ps). The DG ML silicane MOSFET [29] is the only one that fulfills the delay time requirement at $L_g = 1$ nm.

As chip integration increases due to the decreased transistor size, the energy cost of a single transistor is more strictly limited to maintain the energy consumption per unit area. PDP is a crucial indicator that reflects the energy consumption of a transistor in an *on-off* switch and can be calculated by PDP $= I_{on} V_{\rm dd}\, \tau = C_t V_{\rm dd}^2$. Note that the $V_{\rm dd}$ is set at 0.64 V. The PDP is dominated by C_t. As shown in Fig. 6(d), due to the relatively large C_t of the sub-5-nm-L_g GAA Si NWFETs compared with those of the DG ML silicane MOSFET [29] and TG Si NW FinFET [35], their PDPs [n (p), 0.053 (0.049) to 0.193 (0.221) fJ/μm by dia normalization] are higher than those

of the DG ML silicane MOSFET [29] [n (p), 0.008 (0.008) to 0.037 (0.043) fJ/μm] and TG Si NW FinFET [35] (n, 0.007–0.053 fJ/μm) but still within the standard range (<0.24 fJ/μm) of the sub-5-nm ITRS [15] HP applications. Considering peri normalization, the PDP of the n-type (p-type) sub-5-nm-L_g GAA Si NWFETs decreases to 0.012 (0.012) to 0.076 (0.073) fJ/μm. It is reasonable that the peri-normalized PDP value is comparable with those of the TG Si NW FinFET [35] because the normalization approaches are approximate.

The ideal transistor should not only switch quickly but also cost less energy. The FOMs that characterize the compromise of τ and PDP is the EDP, calculated by the equation EDP = PDP × τ. Figure 7 compares the EDP of the GAA Si NWFET with those of several other typical FETs (Si NW fin, ML 2D materials, and 1D CNT) at the same 5-nm gate length [35,45,55,67]. Since both the horizontal (τ) and vertical axes (PDP) are logarithmic, the dashed lines can represent the set of (τ, PDP) that correspond to the same EDP. It is easy to find that all the EDPs of the presented FETs (located within the light blue shaded area) can meet the criteria of both ITRS [15] (until 2028 horizon) and IRDS 2020 (until 2031 horizon) except for the ML MoS_2 MOSFET. The ML InSe [67], 1D CNT [55], ML silicane [29], and TG Si NW FinFET [35] occupy the top four places in terms of EDP. The EDP of the GAA Si NWFET is in the second tier, with its value comparable with those of the ML tellurene (Te) [32], ML Bi_2O_2Se [33], and ML BP FETs [34]. By adopting peri-normalization, the EDP of the GAA Si NWFET is improved but still cannot reach the top tier, indicating an overall intermediate performance in terms of EDP. Owing to the relatively large EDP, ML WSe_2 [57] and ML MoS_2 FETs [66] rank in the last two.

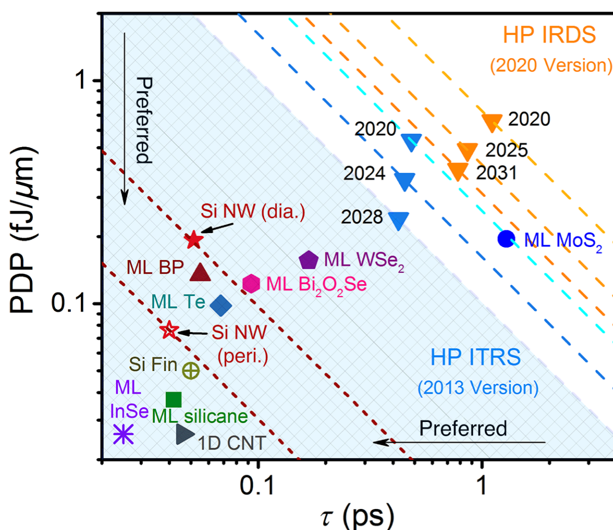

FIG. 7. Power dissipation as a function of delay time for the different HP FETs (GGA Si NW, Si NW fin, ML 2D materials, 1D CNT) at $L_g = 5$ nm [29,35,45,55,57,66]. The criteria of ITRS 2013 (IRDS 2020) are plotted by the blue (orange) dots. The dashed lines represent the equation PDP = EDP/τ.

E. Strain and diameter effects

During the past decades, strain engineering has been adopted as the dominant solution for performance improvements of Si-based devices [27,68–70]. Both experimental and theoretical works have confirmed that strain can drive current enhancement over 4 times in the Si p-MOSFETs and 2 times in the n-MOSFETs [71,72]. The nature of such low-cost and low-risk strain engineering lies in the regulation of band structure and effective mass [36,73]. For example, strain-induced subband splitting and change in DOS can suppress the intervalley scattering; the accompanying carrier repopulation and band warping can lead to the reduction in average conductivity effective mass [74,75]. These all contribute to enhanced mobility. With a deep understanding, the industry shifted the focus from the early biaxial stress to the current uniaxial stress, which has larger mobility enhancements and a smaller shift in threshold voltage [76]. From the 90-nm technology node [77], uniaxial stress was successfully introduced into the industrial MOSFET process flow [78,79]. Encouraged by the strain-enhanced planar MOSFETs, uniaxial stress was also applied to multigate devices as a performance booster [80,81]. Computational studies and experiments both suggested that the 1D Si NWs are very sensitive to strains, with carrier mobility enhanced or reduced over 2 times for moderate strains in the ±2% range, offering unprecedented opportunities to engineer strains in semiconductor devices [27,36,38,62,68,82].

Therefore, we study the uniaxial strain effect, including compressive and tensile strain in the 5-nm-L_g GAA Si NWFET [Fig. 8(a)]. Overall, from the energy band of the 1-nm-diameter Si NW, stress only changes the size of the band gap but does not cause the transformation from a direct to an indirect band gap. As the strain changes from −1% (compression) to +1% (tension), the band gap decreases from 1.6 to 1.55 eV [Fig. 8(b)]; the electron (hole) effective mass decreases from 0.16 (0.13) m_0 to 0.15 (0.12) m_0, as shown in Fig. 8(c). Regarding the 5-nm-L_g GAA Si NWFET, tensile strain has a positive effect on the n-doped device with an increase of nearly 40% in I_{on} at +1% strain, while compressive strain shows a negative effect with about a 20% decrease in I_{on} at −1% strain. Remarkably, both compressive and tensile strains are beneficial to the p-doped device performance, and the effect of tensile strain is more obvious. The I_{on} of the p-doped device performance is increased by 60% and 80% at 1% compressive and tensile strain, respectively [Fig. 8(d)]. Based on the described research, we believe that appropriate uniaxial stress is very promising for boosting the performance of the GAA Si NWFETs,

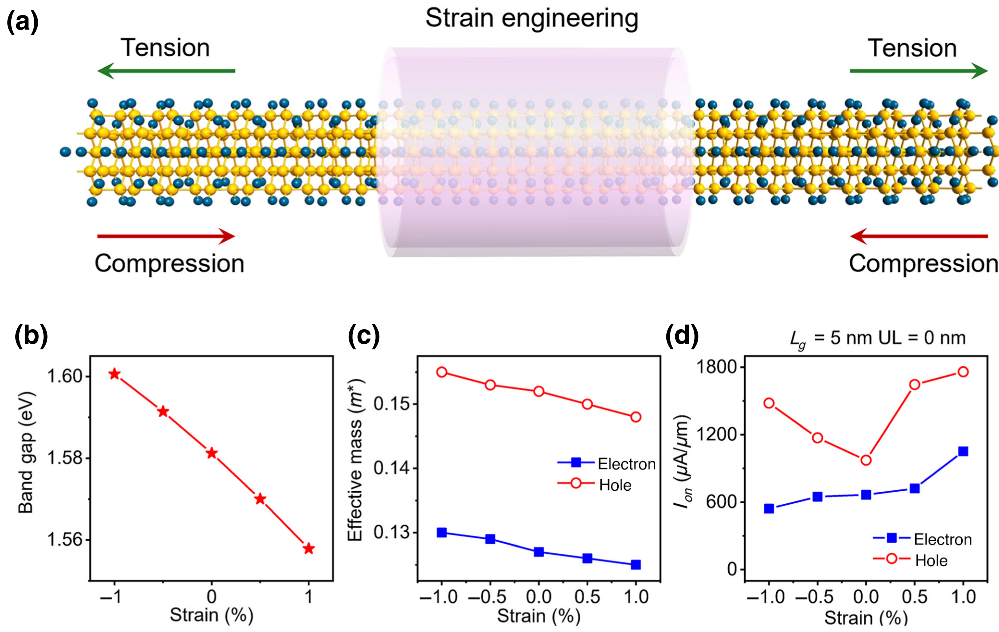

FIG. 8. Strain influence on the GAA Si NWFET under $V_{\text{bias}} = 0.64$ V ($L_g = 5$ nm and $L_{\text{UL}} = 0$ nm). (a) Schematic diagram of the uniaxial tension and compression strain (+1% denotes the tensile strain, and −1% denotes the compressive strain) on the Si NW channel. (b) Band gap, (c) effective mass, and (d) *on*-state current as a function of strain.

implying a long-term vitality for the continuation of industrial Si-based GAA design in the next decades.

IV. DISCUSSION

The previous theoretical works based on the typical low-dimensional FETs with $L_g = 5$ nm only showed the relationship between m^* and I_{on} [45]. The *on*-state current I_{on} will reduce first and then increase as m^* gradually increases, and the valley point is located at 0.8 m_0. The reason is that both a high velocity caused by a small m^* and a high density of states caused by a large m^* could provide a high I_{on}. Both the *n*- and *p*-type GAA Si NWFET with $D_{\text{NW}} = 1$ nm also follow such an I_{on}-m^* relationship

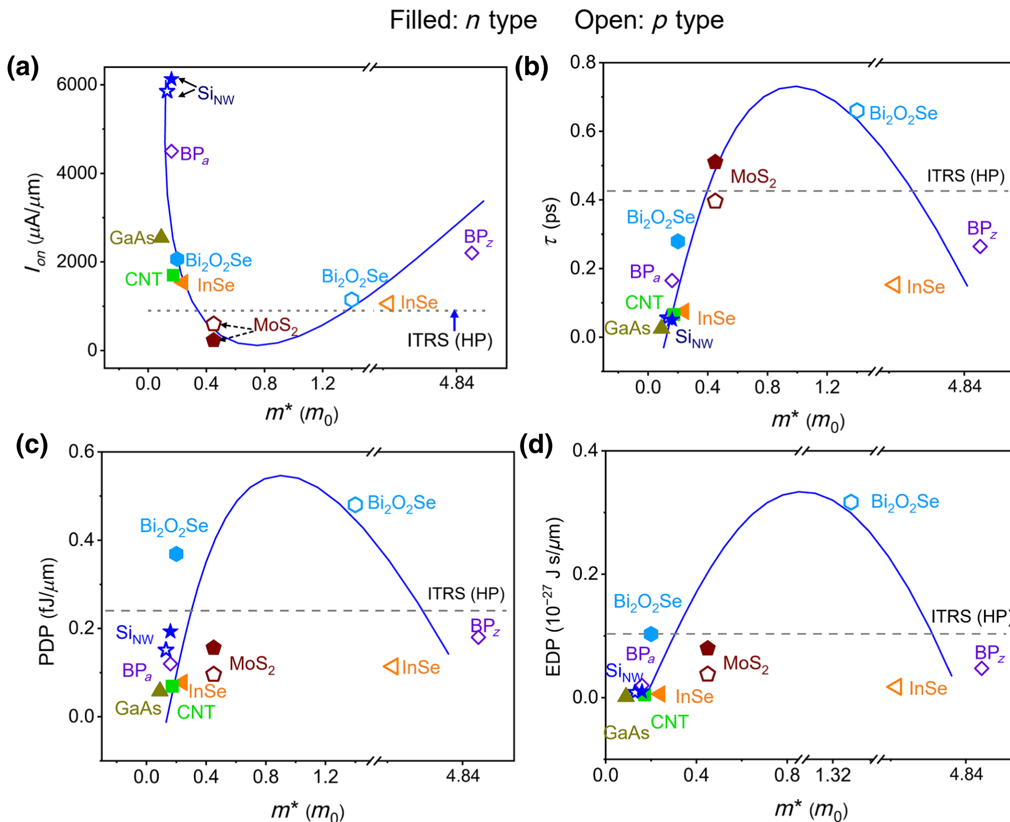

FIG. 9. (a)–(d) C_t, τ, PDP, and the EDPs versus m^* of the 5-nm-L_g MOSFETs based on different low-dimensional materials (CNT [55], ML $GaAsH_2$ [21], ML MoS_2 [66], ML Bi_2O_2Se [33], ML InSe [83], and ML BP along with the armchair and zigzag directions (BPa and BPz, respectively) [34]) for HP applications, respectively.

when L_g is 5 nm (see Fig. S3 in the Supplemental Material for details [64]). However, the relationships between m^* and C_t, τ, PDP, and the EDP have not been studied yet. Herein, we find that C_t, τ, PDP, and the EDP all increase first and then decrease when m^* gradually increases [Figs. 9(a)–9(d)]. τ is in proportion to C_t while in inverse proportion to I_{on}, in terms of the formula $\tau = C_t V_{\text{dd}}/I_{on}$. PDP is entirely dominated by C_t using the equation PDP $= C_t V_{\text{dd}}^2$. The EDP is the product of τ and PDP. Therefore, the trends of all those FOMs with increasing m^* are the same. Interestingly, all their peak points appear at about 0.8 m_0. Those summarized trends of device performance provide more comprehensive guidelines for predicting high-speed low-power transistors.

The effect of the diameter on the device performance of the GAA Si NWFET is also considered. First, the electronic properties of the Si NWs with D_{NW}= 1.8, 1.0, and 0.6 nm are calculated. The band structures of the Si NWs with different D_{NW} are depicted (see Fig. S4 in the Supplemental Material [64]), and the corresponding band gap increases from 1.17 to 1.58 and 2.69 eV when D_{NW} reduces from 1.8 to 1.0 and 0.6 nm [see Fig. S5(a) in the Supplemental Material [64]]. The corresponding hole effective mass also gradually increases from 0.137 to 0.152 and 0.169 m_0 as D_{NW} reduces from 1.8 to 1.0 and 0.6 nm, while the electron effective mass is almost unchanged [see Fig. S5(b) in the Supplemental Material [64]]. Moreover, ε_{ch} for the Si NWs decreases from $1.80\varepsilon_0$ to $1.58\varepsilon_0$ and finally $1.19\varepsilon_0$ as D_{NW} is scaled down from 1.8 to 1.0 and finally 0.6 nm, as shown in Fig. 1. A thinner channel diameter gives rise to a smaller ε_{ch} due to the reduced screening of the electron-electron interaction [20–22]. The calculated λ of the GAA Si NWFETs with D_{NW}= 1.8, 1.0, and 0.6 nm is 0.29, 0.20, and 0.14 nm, respectively. Therefore, the device performance in the 0.6-nm-D_{NW} case is probably the best due to the shorter λ. Herein, the transport properties of the GAA Si NWFET with D_{NW}= 0.6 nm have been studied when L_g is 5 nm and UL is 0 nm. Compared with that in the 1-nm-D_{NW} counterpart, the GAA Si NWFET with D_{NW}= 0.6 nm generally performs better in terms of the FOMs (see Table S2 in the Supplemental Material for details [64]). For example, the I_{on} values of the device in the 0.6-nm-D_{NW} FET are higher than those in the 1-nm-D_{NW} one (1001 vs 666 μA/μm for the *n*-type device and 1339 vs 973 μA/μm for the *p*-type device).

V. CONCLUSION

In conclusion, the ideal GAA Si NWFET with D_{NW}= 1 nm is studied based on *ab initio* quantum transport simulations. The core-distributed electrical conduction is observed in this ultranarrow channel wire. Both the *n*- and *p*-type GAA Si NWFETs show desirable transport properties, with the *on*-state current, delay time, PDP, and EDP satisfying the ITRS [15] HP requirements until the L_g downscales to 3 nm. The optimized 5-nm-L_g *n*-type GAA Si NWFET outperforms its TG NW FinFET and ML silicane counterparts in terms of the enhancement of the *on*-state current and exhibits comparable EDP with those of typical monolayer 2D FETs. Remarkably, by applying a tensile strain up to 1%, about an 80% increase in *on*-state current is observed in the *p*-type 5-nm-gate-length GAA Si NWFET. This study supports that GAA Si NWFET provides good potential for future ultimate short-channel transistors under the 3-nm gate length.

ACKNOWLEDGMENTS

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