Robust Subthermionic Topological Transistor Action via Antiferromagnetic Exchange

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The topological quantum field-effect transition in buckled two-dimensional-Xenes can potentially enable subthermionic transistor operation coupled with a dissipationless *on*-state conduction. We investigate realistic device structures that exploit the quantum field-effect transition between the dissipationless topological phase and the band-insulator phase. We find that the previously considered dual-gate structure is disadvantageous, leading to a near doubling of the subthreshold swing. However, we identify a single-gate strategy capable of overcoming the thermionic limit at the cost of sacrificing the dissipationless *on*-state conduction. By introducing an out-of-plane antiferromagnetic exchange in the material via proximity coupling, we exploit transitions between the quantum spin-valley Hall and the spin quantum anomalous Hall phase, which restore the topological robustness of the *on* state while simultaneously surpassing the thermionic limit. Our work thus outlines a realistic pathway to topological transistors that can overcome Boltzmann's tyranny while preserving topological robustness.

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I. INTRODUCTION

A fundamental challenge today in the evolution of fieldeffect transistors (FETs) is the compulsory power penalty resulting from a fundamental thermionic limit, also known as Boltzmann's tyranny. This relates to the steepness of the transfer characteristics: the subthreshold swing (SS) [1–3], which is conventionally restricted to 60 mV per decade at room temperature. In the context of low-power devices, it is hence paramount to innovate strategies to suppress the SS, thereby ensuring subthermionic operation. Several attempts have been made to overcome this limit, popular ones including tunnel FETs [4–6], impactionization MOSFETs [7], and negative-capacitance FETs (NC FETs) [8–16], to name a few. While the aforementioned paradigms are typically based on transitions between the insulating and the conducting phase, this work aims to investigate realistic device structures that exploit transitions between the dissipationless topologicalinsulator (TI) phase and the trivial band-insulator (BI) phase.

The SS quantifies the corresponding change in drain current I_D due to a change in gate voltage V_G and is given by the expression $(d[\log I_D]/dV_G)^{-1}$. One can further segment the expression into two terms, i.e., $d[\log I_D]/dV_G = (d[\log I_D]/d\psi) \times (d\psi/dV_G)$, by invoking the surface potential ψ , which relates to the position of the channel band structure with respect to the Fermi level. The first term, $d[\log I_D]/d\psi$, depends on the carrier-transport mechanism in the subthreshold regime. The value of this term is limited to $k_B T \ln(10)/q$, because of thermionic emission-based carrier transport in conventional FETs. This limit can be surpassed by the use of tunnel FETs (TFETs), where carrier transport is based on band-to-band tunneling [4–6]. Although TFETs enable subthermionic operation, their on-state current is significantly compromised due to tunneling-based transport, which gives less

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current when compared to the drift current in conventional transistors.

On the other hand, the second term, $d\psi/dV_G$, is dependent on the electrostatic design of the transistor and is at best approximately 1 in the ideal case of complete gate control over the channel. In this context, there has been a lot of interest in the use of ferroelectric materials to endow a negative capacitance (NC) in the transistor gate stack [8–16]. As a result, NC FETs can achieve $d\psi/dV_G > 1$ and attain a SS below the Boltzmann limit. However, there are certain challenges to be addressed because of the energetic instability in the NC regime of ferroelectric insulators [17].

Looking ahead, it is also possible to engineer $d\psi/dV_G$ to be greater than unity via a faster-than-linear translation of the band gap with the topological phase transition between the TI phase (*on* state) and the trivial BI phase (*off* state) [18–23] in two-dimensional (2D) TIs. This can be achieved via the inclusion of an electric field-dependent Rashba spin-orbit interaction [18], which can be termed as the topological quantum field effect (TQFE). The TQFE adds to the electrostatic field effect from the gates, potentially propelling a steeper SS [18]. One can thus envision a topological quantum field-effect transistor (TQFET) built to harness the TQFE.

The combination of the steep-subthreshold slope performance with the dissipationless edge modes in the TI phase makes TQFETs excellent prospects for futuristic low-power electronics. A great deal of experimental effort has thus already been geared toward the realization of topological transistors [24–27]. Quantum spin Hall (QSH) materials such as group-IV and -V Xenes (X can be a group-IV or -V element such as Si, Ge, Sn, As, Sb or Bi) with buckled 2D honeycomb lattices [21,22,28–32], monolayer transition-metal dichalcogenides in the 1*T* configuration [33], HgTe nanoribbons [34], and thin films of three-dimensional (3D) topological insulators Bi₂Se₃ [35,36], as well as Dirac semimetals such as Na₃Bi [37], are among the prominent material candidates.

The demonstration of a workable device design uniting the merits of a dissipationless channel along with the possibility of overcoming Boltzmann's tyranny using the TQFE [18] can thus underline the operational criteria for designing TQFETs as a building block for low-power electronics. In this work, we present such a framework for a holistic analysis of TQFETs and highlight the engineering intricacies involved in harnessing the Rashba spin-orbit interaction (SOI) for a steep SS, while simultaneously preserving the topological robustness of the *on* state. Building on this, we propose a device structure that utilizes the spin quantum anomalous Hall (SQAH) state induced via an outof-plane antiferromagnetic (AF) exchange to achieve the desired performance.

Furthermore, employing the Keldysh nonequilibrium Green's function (NEGF) formalism [41–43], we uncover

fundamental subthreshold limits posed by the gating mechanism that effectuates such a transition. By presenting an in-depth analysis of the band translations necessitated by the field effect, we demonstrate that the thermionic limit of the SS in the TQFETs, designed according to conventional principles, is half as steep as that of the conventional FETs, i.e., $k_B T \ln(10)/q$ [18]. In an attempt to alleviate this issue, we propose to engineer the gate biasing to modulate one of the bands while restricting the other, ultimately attaining a SS transcending the thermionic limit of 60 mV per decade at room temperature. However, this also introduces dissipative conduction modes from the bulk in the on state, defeating one of the desired attributes in a TQFET. As a tactical solution, we demonstrate that the introduction of out-of-plane antiferromagnetic exchange interaction, which can be induced via proximity coupling [44], restores the dissipationless on state and can effectively harness the Rashba-assisted TQFET.

II. FORMULATION

All the transport calculations are based on the Keldysh NEGF formalism [41–43,45], within the tight binding framework of the model Hamiltonian, well described in various works, which we briefly describe [19,20,23,46].

A. Device Hamiltonian

The building block of the TQFET is a 2D TI with a buckled-honeycomb-lattice structure that forms the channel as depicted in Fig. 1(a). For numerical calculations pertinent to our proposed topological transistor, we consider the typical tight-binding Hamiltonian model for the 2D buckled-honeycomb lattice [47,48] in the second quantized notation:

$$\hat{H} = -t \sum_{\langle i,j \rangle \alpha} c^{\dagger}_{i\alpha} c_{j\alpha} + i \frac{\lambda_{\rm SO}}{3\sqrt{3}} \sum_{\langle \langle i,j \rangle \rangle \alpha\beta} v_{ij} c^{\dagger}_{i\alpha} s^{z}_{\alpha\beta} c_{j\beta} + \lambda_{v} \sum_{i\alpha} c^{\dagger}_{i\alpha} \mu_{i} c_{i\alpha} + i \lambda_{R} \sum_{\langle ij \rangle \alpha\beta} c^{\dagger}_{i\alpha} (s_{\alpha\beta} \times \hat{d}_{ij})_{z} c_{j\beta}, \quad (1)$$

where $c_{i\alpha}^{(\dagger)}$ represents the electronic annihilation (creation) operator on site *i* with a spin $\alpha = \uparrow (\downarrow)$ and $\langle i, j \rangle$ and $\langle \langle i, j \rangle \rangle$ characterize the nearest-neighbor and the next-nearestneighbor hopping, respectively. The spin indices are represented with corresponding values +1/-1, respectively. The first term in Eq. (1) represents the nearest-neighbor hopping term with a hopping strength *t*. The second term represents the intrinsic spin-orbit (SO) coupling with strength λ_{SO} , where $v_{ij} = +1$ (-1) for anticlockwise (clockwise) next-nearest-neighbor hopping with respect to the positive *z* axis. The third term denotes the staggered sublattice potential of strength λ_v , with $\mu_i = +1$ (-1), where *i* denotes the sublattice *A* (*B*). The fourth term represents the nearest-neighbor Rashba spin-mixing interaction,



FIG. 1. The device structure and phase transitions. (a) A 2D buckled-honeycomb-monolayer Xene is used as the channel (C), left (L), and right (R) lead material. The leads are colored green to distinguish them from the channel region, where the two sublattices, A and B, are represented in red and blue, respectively. (b) A schematic representation of a dual-gated device structure. The top and bottom gates have applied potentials V_A and V_B , respectively, so that the net potential difference across the channel material is $(V_A - V_B)$. For the symmetric bias arrangement, $V_A = \lambda_v/2$ and $V_B = -\lambda_v/2$. (c),(d) The band structures of the channel and leads for the TQFET, in the on and the off state, respectively. The Fermi level (E_f) is represented by a solid black line. (e) The phase diagram of a monolayer Xene nanoribbon with homogeneous perpendicular electric field and antiferromagnetic exchange field [38–40].

with $s_{\alpha\beta}$ denoting the corresponding matrix elements indicating the spin polarization α and β at lattice sites *i* and *j*, respectively, and \hat{d}_{ij} is the distance vector between lattice sites *i* and *j*.

B. Calculation of the transmission coefficient

The current-voltage (I-V) characteristics are calculated from the energy-resolved transmission coefficient T(E), which is evaluated using the Green's function as

$$T(E) = \operatorname{Tr}[\Gamma_L(E)G^R(E)\Gamma_R(E)G^A(E)], \qquad (2)$$

$$[\Gamma_{L,R}(E)] = i[\Sigma_{L,R}(E) - \Sigma_{L,R}(E)^{\dagger}], \qquad (3)$$

$$[G^{R}(E)] = [(E + i\eta)I - H - \Sigma_{L}(E) - \Sigma_{R}(E)]^{-1}, \quad (4)$$

where Tr represents the trace operation, $[\Gamma_{L(R)}(E)]$ is the broadening matrix corresponding to the lead L(R), and $[G^{R}(E)]$ and $[G^{A}(E)]$ are the matrix representations of the retarded and advanced Green's functions, respectively. All quantities in the above equations can be obtained from the Hamiltonian defined in Eq. (1) and the self-energy matrices $[\Sigma_{L,R}]$, which are calculated recursively, based on the formalism prescribed in Refs. [45,46].

Finally, the current calculations are performed based on the Landauer transmission formula, with the transmission coefficient evaluated from the device-retarded Green's function

$$I = \frac{e^2}{h} \int_{-\infty}^{\infty} T(E)(f(E, \mu_L, T) - f(E, \mu_R, T)) dE, \quad (5)$$

where $f(E, \mu, T) = (1 + \exp(E - \mu/k_BT))^{-1}$ is the Fermi-Dirac distribution at Fermi energy μ and temperature *T*. The impressed voltage across the device is given as $qV = \mu_L - \mu_R$, where $\mu_{L(R)}$ represents the Fermi energy of the left (right) lead.

III. RESULTS AND DISCUSSION

In the transistor setup depicted in Fig. 1(b), an electric field (E_Z) applied perpendicular to the buckled lattice manifests as a staggered potential between the sublattices A and B of the honeycomb unit cell. The dual-gate structure helps in realizing the electric field between the two plates, hence imparting a capacitive action. Such a dual-gate manifestation of a topological transistor also enables a twofold biasing scheme: (a) symmetric biasing, where equal and opposite bias voltages are applied to the two gates, i.e., $V_A = -V_B$; and (b) rigid biasing, where the entire voltage is applied to one of the gate plates, with the other plate grounded. For the symmetric bias setup, the Fermi level is positioned as in Figs. 1(c) and 1(d) to ensure topological *on*-state conduction.

It is worth remarking at this point that we are primarily focusing on group-IV and -V Xenes with a buckledhoneycomb lattice. The buckled structure possessed by these materials allows us to manipulate their topological nature by means of a perpendicular electric field created using a dual-gate structure. Also, the inclusion of additional effects such as Rashba SOI and antiferromagnetic exchange, critical for our device design, can be modeled very conveniently by adding extra terms to the channel Hamiltonian, as discussed in the subsequent sections. It is also worth mentioning that more innovative and advanced spin-orbit materials such as $1T' MoS_2$ could also be potential candidates for the channel material. However, incorporating such materials as the channel would demand investigation into the effect of Rashba SOI and antiferromagnetic exchange on the Hamiltonian from first-principles calculations. Also, these materials have a more complicated lattice structure than group-IV and -V Xenes and, hence, a detailed study of the electric-fieldinduced topological quantum field effect is needed for such materials.

Previous proposals of topological transistors using buckled Xene nanoribbons have been mostly based on the QSH-quantum valley Hall (QVH) phase transition on varying the out-of-plane electric field, which effectively navigates the horizontal axis of the phase diagram, as depicted by points i, ii, and iii in Fig. 1(e). Apart from the above, one can have new topological phases on the inclusion of an out-of-plane AF exchange field, represented by the vertical axis in Fig. 1(e). Navigating along the horizontal direction for an AF exchange greater than some critical value, as depicted by points 1, 2, and 3 in Fig. 1(e), one can have a topological transition between an insulating quantum spin-valley Hall (QSVH) phase and a conducting SQAH phase [38–40]. In the SQAH phase, the AF interaction breaks the time-reversal symmetry (TRS), resulting in spin-polarized conducting modes without a chiral counterpropagating partner.

To analytically investigate the subthreshold physics of topological transistors, we adopt the low-energy effective four-band Bloch Hamiltonian H_{η} in the vicinity of Dirac points *K* and *K'* as given by Eq. (6). This Dirac Hamiltonian is derived from the tight-binding Hamiltonian model described in Eq. (1) for the 2D buckled-honeycomb lattice [21,22,47,48]:

$$H_{\eta} = \hbar v_f \left(\eta k_x \tau_x + k_y \tau_y\right) \sigma_0 + \eta \lambda_{\text{SO}} \tau_z \sigma_z + \lambda_v \left(E_Z\right) \tau_z \sigma_0 + \frac{\lambda_R \left(E_Z\right)}{2} (\eta \tau_x \sigma_y - \tau_y \sigma_x), \quad (6)$$

where $\eta = +1$ or -1 is the valley index denoting K(K')and σ and τ are the spin and pseudospin Pauli matrices, respectively. Here, \hbar is the reduced Planck's constant and v_f denotes the Fermi velocity, given by the expression $v_f = 3ta_o/2$, where t is the hopping parameter and a_o is the lattice constant. The quantities λ_{SO} , λ_v , and λ_R denote the strengths of the intrinsic spin-orbit coupling, the staggered sublattice potential, and the Rashba spin-mixing interaction, respectively.



FIG. 2. The band structures of the channel for different λ_v . (a) The QSH phase, characterized by topologically protected edge states. Here, we assume that $\lambda_v = 0$ and consider two cases of $\lambda_R = 0$ and $\lambda_R \neq 0$. (b) The transition from the QSH to the QVH phase for the $\lambda_R = 0$ case. For the $\lambda_R \neq 0$ case, the system has already entered the BI phase. Here, we consider $\lambda_v = \lambda_{SO}$, where λ_{SO} is the intrinsic spin-orbit coupling strength. (c) A demonstration of the faster retreat of the CB in the $\lambda_R \neq 0$ case compared to the $\lambda_R = 0$ case. The VB in both cases remains almost pinned. Here, $\lambda_v = 1.5\lambda_{SO}$.

In the context of an electric-field-induced topological phase transition between the QVH and the QSH phases [46], it is important to analyze the Chern number [23] (C) and the nature of the edge states. For $\lambda_v < \lambda_{SO}$, the QSH phase is characterized by a zero total Chern number C and a nonzero spin Chern number $2C_s = +2$, resulting in helical edge states as illustrated in Fig. 2(a). A phase transition at $\lambda_v = \lambda_{SO}$, as in Fig. 2(b), results in the QVH phase for $\lambda_v > \lambda_{SO}$. This BI phase is characterized by both zero Cand $2C_s$, leading to a trivial gap as shown in Fig. 2(c). The faster closing and reopening of the gap for the $\lambda_R \neq 0$ case when compared to $\lambda_R = 0$ case, as shown in Fig. 2, nicely illustrates the TQFE switching.

The total current with components I_c and I_v due to the electrons in the conduction band (CB) and holes in the valence band (VB) is given as

$$I_{c} = I_{c_{o}} \exp -\frac{q\left(E_{c} - E_{f}\right)}{k_{B}T},$$

$$I_{v} = I_{v_{o}} \exp \frac{q\left(E_{v} - E_{f}\right)}{k_{B}T},$$
(7)

where $I_{c_o(v_o)}$ is the CB (VB) current maximum, $E_{c(v)}$ represents the CB (VB) minimum (maximum), and E_f denotes the equilibrium Fermi energy level. Here, k_BT is the thermal energy at temperature T.

The SS of a transistor during the *on-off* state transition is defined as

$$SS = \left| \frac{d(\log_{10} I)}{dV_G} \right|^{-1}, \tag{8}$$

where $I (= I_c + I_v)$ represents the current in response to an applied gate voltage V_G . Substituting I from Eq. (7) in Eq. (8), we obtain

$$SS = \frac{k_B T}{q} \ln(10) \frac{I}{\left| I_v \left(\frac{dE_v}{dV_G} \right) - I_c \left(\frac{dE_c}{dV_G} \right) \right|}, \qquad (9)$$

where $k_B T \ln(10)/q$ is the thermionic limit at temperature T, which reduces to 60 mV per decade at room temperature. We then define S^* , which is the reduced SS [18] as

$$S^* = \frac{I}{\left|I_v\left(\frac{dE_v}{dV_G}\right) - I_c\left(\frac{dE_c}{dV_G}\right)\right|}.$$
 (10)

For conventional MOSFETs, it has hitherto been assumed that $S^* \ge 1$. Moreover, it is anticipated in Ref. [18] that the introduction of Rashba interactions can achieve $S^* \le 1$ to overcome the Boltzmann limit. However, we now demonstrate that this limit (S^*) for a TQFT is, unfavorably, twice as much.

Figure 3(a) depicts the *n*-MOS operation of a conventional transistor. For an applied gate bias ΔV_G , both the CB and the VB move equally by an amount proportional to ΔV_G . For an *n*-MOS device, this upward ascent of the bands results in $I_c \gg I_v$. In this case, both (dE_c/dV_G) and (dE_v/dV_G) are unity, since both bands translate by an equal amount ($\propto \Delta V_G$).

For a TQFET with $\lambda_R = 0$, however, the translation of bands in response to ΔV_G is nontrivial. As depicted in Fig. 3(b), both the bands move away from the Fermi level by an amount proportional to $\Delta V_G/2$ in the off state. So, $(dE_c/dV_G) = 1/2$ and $(dE_v/dV_G) = -1/2$ for a TQFET with $\lambda_R = 0$. Moreover, due to symmetry in the band translation, the current components $I_c \approx I_v \approx I/2$. This results in $S^* \approx 2$ and hence the SS in a standard TQFET is restricted to $2k_BT \ln(10)/q$ instead of $k_BT \ln(10)/q$. At room temperature, this translates to the thermionic limit being restricted to 120 mV per decade instead of 60 mV per decade in the conventional case.

With the introduction of the Rashba SOI term, the band translation during the *off* state (the QVH phase) is asymmetric. From the Dirac Hamiltonian elaborated in Eq. (6), we calculate E_c and E_v for $\lambda_v > \lambda_{SO} > 0$, i.e., in the *off*





FIG. 3. The band-translation schematics and *I-V* characteristics for a QSH-QVH-transition-based FET. (a) A representation of the band movement in an ordinary *n*-MOSFET for an applied bias potential of ΔV_G . Here, $I_C > I_V$. (b) A representation of the band movement in the *off* state of a topological transistor with $\lambda_R = 0$. Here, $I_C = I_V$. (c) A representation of the band movement in the *off* state of a topological transistor with $\lambda_R \neq 0$. Here, $I_C < I_V$. (d) The *I-V* characteristics of a topological transistor based upon phase transition from *on* ($V_G < 0.8$ V) to *off* ($V_G > 0.9$ V) phase, for different Rashba strengths of $\lambda_R = 0$, $\lambda_R = 0.3\Delta_Z$, and $\lambda_R = 0.5\Delta_Z$. Here, $\Delta_Z = \lambda_v$. For all the three cases, the subthreshold swing (SS) remains confined to 120 mV per decade of current.

state, as follows:

$$E_v = \lambda_{\rm SO} - \lambda_v,$$

$$E_c = -\lambda_{\rm SO} + \sqrt{\lambda_v^2 + \lambda_R^2},$$
(11)

where λ_v and λ_R can be represented as $\alpha_V E_Z$ and $\alpha_R E_Z$, respectively, since they are both linearly proportional to the gate electric field E_Z . Taking derivatives with respect to V_G , we obtain $(dE_v/dV_G) = -1/2$ and $(dE_c/dV_G) =$ $0.5\sqrt{(1 + \alpha_R^2/\alpha_V^2)}$. Note that putting $\alpha_R = 0$, we obtain the same results as estimated previously for the $\lambda_R = 0$ case. Also, we note that in the QVH phase, the CB translates faster with increasing gate bias than the VB due to the effect of the Rashba term α_R . However, since $|E_v| < |E_c|$, we expect I_v to contribute more to the current than I_c . Thus, from Eq. (10), we expect (dE_v/dV_G) to contribute more to the SS. Thus, the improved SS due to (dE_c/dV_G) is undone by the relatively smaller contribution from I_c . This mechanism is represented schematically in Fig. 3(c).

In Fig. 3(d), we show the evaluated subthreshold characteristics using the NEGF approach [41–43,45]. We set T = 300 K and $\lambda_{SO} = 0.41$ eV with a hopping parameter t = 1.6 eV, consistent with first-principles calculations [18].

We assume a finite-sized nanoribbon as the channel material, with a device length $N_L = 45$ and width $N_W = 20$. The NEGF simulations reconcile with the analytical conclusions drawn. Despite the introduction of Rashba interactions, the SS is limited to $2k_BT\ln(10)/q$ or 120 mV per decade at T = 300 K. With the symmetric gate biasing, as seen in previous sections, the channel Fermi level is pinned in the middle of the band gap of the channel. As a result, in the QVH phase (off) the channel conducts the smallest possible current. Moreover, using symmetric gate biasing, the SS cannot be improved significantly below 120 mV per decade even in the presence of Rashba SOI. Hence, an alternative approach is required that relies upon smart positioning of the channel Fermi level to create an imbalance in the rate at which the two bands move away from the channel Fermi level, as a function of the applied gate voltage.

The easiest way to do this would be via an asymmetric gate biasing, where V_A and V_B , corresponding to Fig. 1(b), are set to V_G and zero, respectively. This particular gating scheme has an added advantage that it is compatible with modern-day transistor architectures because it requires only a single gate voltage as opposed to the dual-gate-voltage requirement of symmetric gate biasing. Now, positioning the Fermi level at E = 0 [solid line in Figs. 4(a)-4(d) leads to an inherent problem, as described below. At $\lambda_v = 0$, as shown in Fig. 4(a), the Fermi level lies right in the middle of the band gap. Because of rigid biasing in the QSH phase, only the VB moves with varying gate voltage and after a certain point, the Fermi level slips inside the VB. Beyond the critical field, the Fermi level remains pinned inside the VB. As a result, the TQFET does not turn off in the QVH phase, because of the VB bulk states participating in the conduction. Despite the Fermi level in the leads being aligned to the CB, leakage current conduction in the off state may be facilitated by band-to-band tunneling, as depicted in Fig. 4(e), which is undesirable. (Note that in ideal operation, the device does not rely on any band-to-band tunneling effects.)

The problem highlighted above arises because of the Fermi level lying inside the VB in the QVH phase, resulting in a deteriorated off state. One obvious way to alleviate this issue is to align the Fermi level inside the band gap for the QVH phase. However, in this scenario, the Fermi level moves inside the CB in the QSH phase (on state). Thus, apart from the dissipationless edge modes, even the dissipative bulk states participate in conduction. This strategy restores the full advantage of the Rashba SOI-enabled TQFE in reducing the SS. However, conduction no longer occurs solely through dissipationless edge states. This may be disadvantageous, though the details of the on-state conduction depend on material and device parameters, and in principle dissipative bulk states can also contribute to enhanced on current. Thus, by allowing dissipative bulkstate conduction, it is possible to achieve subthermionic performance with a negligible off current, by aligning



FIG. 4. The rigid-biasing approach, wherein $V_A = V_G$ and $V_B = 0$. (a)–(d) The band structures for varying λ_v along with the corresponding Fermi levels (elaborated in the text). (e) The possible band-to-band tunneling when the channel Fermi level lies inside the VB, leading to undesirable *off* current. (f) The *I-V* characteristics for a rigidly biased TQFET with a suitably positioned Fermi level for different values of λ_R . The corresponding SS values for $\lambda_R = 0$, $0.3\Delta_z$, and $0.5\Delta_z$ are 60 mV per decade, 52 mV per decade, and 49 mV per decade, respectively.

the Fermi level as shown by the dashed lines in Figs. 4(a)-4(d).

The obtained *I-V* characteristics for the above case are as shown in Fig. 4(f). The *on* current is significantly higher (> 10⁴) when compared to that of the symmetric biasing case in Fig. 3(d), owing to the fact that the current-carrying states in the *on* state are now the bulk modes of the QSH phase. Because of rigid gate biasing, as illustrated by our numerical simulations, the SS calculated for $\lambda_R = 0$ is around 60 mV per decade, the thermionic limit being at 300 K. The inclusion of Rashba SOI further enhances the subthreshold performance, with SS values of 52 mV per decade and 50 mV per decade for the cases of $\lambda_R = 0.3 \Delta_z$ and $0.5 \Delta_z$, respectively, thus exemplifying the subthermionic performance enabled by the introduction of Rashba SOI for a rigidly biased TQFET with a suitably positioned Fermi level.

While the above strategy is a robust route to a subthermionic transistor, we would also like to understand whether it is possible to retain both the subthermionic SS and the dissipationless edge transport in the *on* state. Dissipationless edge transport should provide significant advantages for certain device geometries and, hence, is an indispensable feature to retain. We thus explore ideas beyond the QSH-QVH transition and look into new topological phases. As suggested by Eq. (9), one way to achieve $S^* \leq 1$ is by ensuring that at least one of the quantities (dE_c/dV_G) and (dE_v/dV_G) exceeds unity. If, say, the CB satisfies this, then for subthermionic performance, the CB current should be the major contributor to the total current. In other words, we can attain subthermionic performance by ensuring that $(dE_c/dV_G) \geq 1$ and $I_c \gg I_v$.

In the QSH-QVH-transition-based TQFET with symmetric biasing, evident from Eq. (11), it is possible to achieve $(dE_c/dV_G) \ge 1$ in the presence of a large enough Rashba SOI. However, as a result of this, in the QVH phase, the CB moves away from the Fermi level at a greater rate than the VB and we obtain $I_v \gg I_c$, as illustrated in Fig. 3(c), and thus there is no discernible improvement in S^* . This happens because in the off state, the band gap opens as we increase the gate voltage. For the Rashba-influenced band to contribute more to the total current, the band gap should close as the applied field increases. In such a scenario, the Rashba-influenced band would be closer to the Fermi level throughout the sub-threshold regime (off state). This will eventually lead to subthermionic performance.

The above scenario can be realized by the addition of AF exchange interaction, which can be incorporated via proximity coupling [44] to a 2D topological insulator, implying the addition of the term $M_{\rm AF}\tau_z\sigma_z$ to the low-energy Hamiltonian in Eq. (6). As represented by points 1, 2, and 3 in Fig. 1(e), for $M_{\rm AF} > \lambda_{\rm SO}$, one can realize the QSVH phase and the SQAH phases by varying the perpendicular electric field [38–40]. For $\lambda_v < M_{\rm AF} - \lambda_{\rm SO}$, we obtain the QSVH phase with a Chern number C = 0 and no gapless edge states. On the other hand, $\lambda_v > M_{\rm AF} - \lambda_{\rm SO}$ opens the SQAH phase with a Chern number C = 1, possessing spin-polarized chiral edge states. The perfect spin polarization of the edge currents may also provide connections to spintronics applications. Figure 5 shows the band structures for the various phases that arise under the influence of out-of-plane AF exchange interaction when the gate voltage is varied. Here, the QSVH phase represents the off state, i.e., the transition is from off to on as the gate voltage increases, contrary to the scenario in the QSH-QVH transition.

Now, as depicted in Fig. 6(a), the band gap closes in the subthreshold regime on increasing gate voltage and the Rashba-influenced VB moves closer to the Fermi level, such that $I_v \gg I_c$. In this case, if λ_R is large enough for dE_v/dV_G to be greater than unity, it is possible to achieve $S^* < 1$. Analytically, based on the low-energy Dirac Hamiltonian in Eq. (6), and in the presence of Rashba SOI, we have the following in the QSVH phase:

$$E_{v} = \lambda_{\rm SO} - M_{\rm AF} + \sqrt{\lambda_{v}^{2} + \lambda_{R}^{2}},$$

$$E_{c} = M_{\rm AF} - \lambda_{\rm SO} - \lambda_{v}.$$
(12)



FIG. 5. The band structures of the channel for different λ_v , highlighting the underlying switching principle under the influence of an antiferromagnetic term. (a) A representation of the quantum spin-valley Hall (QSVH) phase characterized by an insulating gap for the two valleys *K* and *K'*. Here, we assume that $\lambda_v = 0$ and consider two cases of $\lambda_R = 0$ and $\lambda_R \neq 0$. (b) A depiction of the QSVH-SQAH transition for the $\lambda_R = 0$ case. For the $\lambda_R \neq 0$ case, topologically protected edge states are prominent. Here, we consider $\lambda_v = 0.7\lambda_{SO}$, λ_{SO} being the intrinsic spin-orbit coupling strength. (c) A demonstration of the onset of the *on* phase for both the $\lambda_R = 0$ and $\lambda_R \neq 0$ case. Here, we choose $\lambda_v = 1\lambda_{SO}$.

Clearly, on increasing E_z , the VB approaches the Fermi level at a greater rate for a nonzero λ_R and the VB current is the major contributor.

These analytical findings are well supported by the simulated results in Fig. 6(b). Here, the following parameters are considered: $\lambda_{SO} = 0.41$ eV and $M_{AF} = 1.7\lambda_{SO}$. We consider three values of λ_R for comparison— $\lambda_R = 0$, $0.5\Delta_z$ and $0.8\Delta_z$ —where $\Delta_z = \lambda_v$. The $\lambda_R = 0$ case, similar to the previous QSH-QVH case, gives a SS of around 120 mV per decade, because of symmetric band translation under symmetric biasing. However, upon increasing λ_R , we note a significant improvement in the SS, with the topological transistor achieving SS < 60 mV per decade for $\lambda_R = 0.8\Delta_z$. Thus the addition of an out-of-plane AF exchange interaction to a 2D TQFET under symmetric biasing can attain subthermionic characteristics. One thing to note is that the current remains constant in the *on*



FIG. 6. Transistor operation with the inclusion of the AF interaction. (a) The band-translation schematics in the *off* state of a TQFET is when $I_C < I_V$. The Fermi level is closer to the VB than the CB. (b) The *I-V* characteristics based on phase transitions in the subthreshold region for different Rashba interactions, for $\Delta_Z = \lambda_v$. We note a progressive improvement in the SS as λ_R increases.

state for an appreciable range of gate voltage, suggesting that the dissipationless edge modes are responsible for the *on*-state conduction. Adding to this, a TQFET hosting chiral QAH edge modes is expected to be more resilient to backscattering than one having helical QSH edge modes. This is because QSH requires the TRS to be preserved to maintain its robustness. However, this is not the case with the QAH phase, which is robust even to backscattering by magnetic disorder, because of the absence of any time-reversal partner for the chiral edge modes.

IV. CONCLUSIONS

This work deals with an in-depth analysis of how a topological field-effect transition can effectuate a subthermionic transistor operation. We investigate realistic device structures that exploit the quantum field-effect transition between the dissipationless topological phase and the BI phase. Our analysis reveals that the previously considered dual-gate structure is disadvantageous, leading to a near doubling of the subthreshold swing. However, we identify a single-gate strategy capable of beating the thermionic limit at the cost of sacrificing the dissipationless on-state conduction. By introducing an out-of-plane antiferromagnetic exchange in the material via proximity coupling, we demonstrate how to exploit transitions between the QSVH and the SQAH phase, which restores the topological robustness of the on state while simultaneously surpassing the thermionic limit. Our work thus outlines a realistic pathway to topological transistors that can overcome Boltzmann's tyranny while preserving the topological robustness. Further analysis along the lines of introducing defects and the study of dephasing [46,49] and their effects on the topological robustness is a fruitful direction in which to move the analysis forward. Future works that develop electrothermal transport [50], as well as high-frequency analysis [51-53], in order to concretize the transistor operation are necessary to realize the goal of topological electronics [24]—the engineering of emerging devices from topological quantum matter.

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