Sub-5-nm Monolayer GaSe MOSFET with Ultralow Subthreshold Swing and High *On*-State Current: Dielectric Layer Effects

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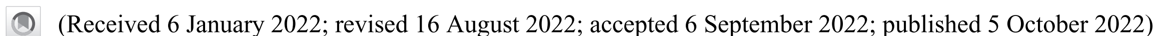

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With the increasing demand for miniaturized devices and integrated circuits, ultrasmall-scale device units have attracted increasing attention. However, the short-channel effects severely limit the development of high-performance micro- and nanodevices. Here, we design sub-5-nm dual-gate monolayer GaSe metal-oxide-semiconductor field-effect transistors (MOSFETs) and systemically analyze the transmission spectrum, local density of states, *on*-state current (I_{on}), and subthreshold swing (SS), considering different dielectric layer thicknesses, dielectric constants, and underlap lengths. The results show that, with decreasing equivalent oxide thickness, the SS (I_{on}) shows a downward (uptrend) trend. Compared with Al_2O_3 and HfO_2 substrates, the SS and I_{on} can be modified obviously through the dielectric layer thickness for 3-nm GaSe MOSFETs with SiO_2 substrate. The I_{on} can be tuned from 904 to 1766 μA/μm, which is about 2 times higher than the high-performance requirements of the International Technology Roadmap for Semiconductors (ITRS) (900 μA/μm) for 2028. Meanwhile, the SS is upgraded from 134.8 to 62.7 mV/dec, closing the Boltzmann tyranny (60 mV/dec). Therefore, this work provides a route to realize ultrashort-scale MOSFETs with an ultralow subthreshold swing and a high *on*-state current through engineering the dielectric layer.

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I. INTRODUCTION

With the progress of science and technology, electronic device units tend to be miniaturized. However, it is very difficult for silicon transistors to sustain Moore's law [1]. Recently, two-dimensional (2D) semiconductors WSe_2were expected to replace silicon for future highly integrated nanodevices [2–6]. For instance, 2D WSe_2 is used in neuromorphic computing, solar cells, and binary convolutional neural networks [7–10]. A high-quality Schottky diode is prepared by using the low Schottky contact barrier between InSe and graphene [11]. The peak-to-valley ratio of black-phosphorus (BP) tunnel-field-effect transistors (TFETs) is 130 at room temperature [12], which indicates that BP TFETs is promising for application in multiple-value logic circuits. In addition, the carrier mobility of MoS_2 metal-oxide-semiconductor field-effect transistors (MOSFETs) is improved obviously by using the high-*k* dielectric layer [13].

Among the various 2D materials, GaSe possesses excellent electric and optical characteristics [14–18]. Mechanical exfoliation, chemical vapor deposition (CVD), and epitaxial growth are feasible methods to fabricate 2D GaSe nanosheets [19–21], which provides the possibility for the fabrication of GaSe-based devices. Three-terminal memristors based on 2D GaSe possess a series of merits, including a large switching ratio, high cycling endurance, and long-term retention ($\sim 10^4$ s) [22]. The GaSe/transition metal dichalcogenides (TMDCs) heterojunctions have a bright future in self-driven photoelectric detection, rectification, and optical response modulation [23–25]. By setting the compliance-current value, a resistive-switching (RS) device based on 2D GaSe exhibits remarkable bipolar-resistive-switching and threshold-switching behaviors [26]. Considering the superior performance of the GaSe monolayer, there are few studies on the effect of dielectric layer engineering on the performance of 2D semiconductor sub-5-nm MOSFETs, so we select monolayer GaSe as an example to design ultrashort-scale MOSFETs and study the corresponding properties.

Here, we investigate the effects of dielectric layer thickness, dielectric constant, and underlap length on the ballistic transport properties of GaSe-based *n*-MOSFET. The results show that, when the equivalent oxide thickness is decreased, the subthreshold swing (SS) and *on*-state current (I_{on}) present downward and upward trends, respectively. Moreover, utilizing the optimal underlap (UL) structure and high-*k* dielectric layer simultaneously, the SS

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can be reduced by 53.5%. Compared with the performance of GaSe MOSFETs and other 2D n-MOSFETs, regardless of the SS or I_{on}, GaSe shows excellent performance in MOSFETs with a gate length of 3 nm.

II. METHODS

The Atomistix ToolKit 2017 package is implemented to simulate the transport properties of GaSe-based MOSFETs. The calculation method is based on the combination of the density-functional-theory framework and the nonequilibrium Green function [27,28]. According to the Landauer-Büttiker formula, the drain current (I_{DS}) is calculated as follows:

$$I(V_{DS}, V_g) = \frac{2e}{h} \int_{-\infty}^{+\infty} \{T(E)[f_S(E-\varepsilon_S) - f_D(E-\varepsilon_D)]\}. \quad (1)$$

where V_{DS} is the bias voltage and V_g is the gate voltage; e and h are the elementary charge and the Planck constant, respectively. In addition, the transmission coefficient is denoted by $T(E)$, and f_S (f_D) stands for the Fermi-Dirac distribution function of the source (drain). Besides, the electrochemical potential of the source and drain are expressed as ε_S and ε_D, respectively. We would like to point out that phonon-scattering effects can affect the transport performance of transistors. According to previous publications on the transport properties of 2D transistors [29–33], ballistic transport is considered to be a good approximation for 2D devices with ultrashort-channel lengths. Thus, for simplicity, here, the transport characteristics of GaSe MOSFETs are studied without considering the phonon-scattering effects.

To obtain accurate and efficient results, the norm-conserving pseudopotential and the basis set are SG15 and "high," respectively [34,35]. For self-consistency of electronic structure, we set the real-space mesh cutoff of 120 hartree and $1 \times 31 \times 151$ Monkhorst-Pack grids. The Neumann, periodic, and Dirichlet boundary conditions are used in the x, y, and z directions, respectively, where x is the vertical direction, y corresponds to the transverse direction, and the z direction is the direction of charge transmission. The temperature is set to 300 K. In addition, the exchange-correlation interaction is determined by the generalized gradient approximation and the Perdew-Burke-Ernzerhof functional [36].

III. RESULTS AND DISCUSSION

A. Device model and electronic properties

Monolayer GaSe is a honeycomb lattice composed of Se-Ga-Ga-Se atomic layers joined by covalent bonds, as shown in Fig. 1(a). The optimized lattice parameters of the GaSe monolayer are $a = b = 3.821$ Å, the bond length of Ga—Ga is 2.47 Å and that of Se—Se is 4.83 Å, which are consistent with previous reports [37,38]. In Fig. 1(b), we present the MOSFET model constructed with n-doped monolayer GaSe for the source and drain electrodes and intrinsic GaSe as the channel. Analysis of the doping concentration is shown in Fig. S1 within the Supplemental Material [39]. Considering I_{on} and the SS performance, an electron doping value of 1×10^{13} cm^{-2} is used to carry

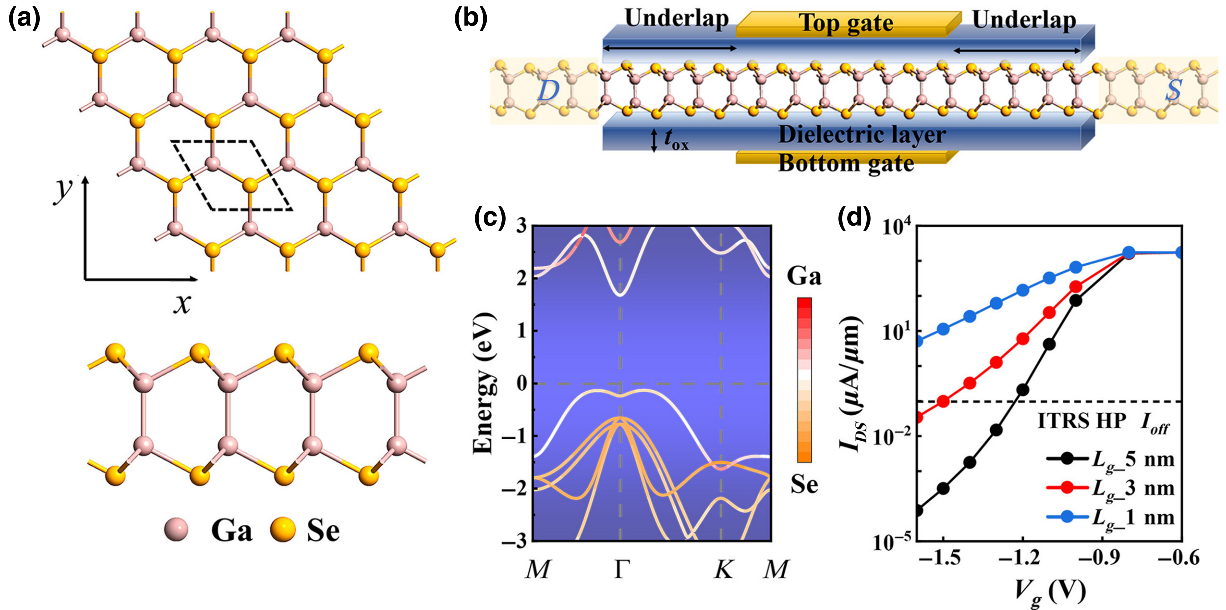

FIG. 1. (a) Top and side views of GaSe monolayer. Dashed rhombus represents the primitive unit cell. (b) Device model of dual-gate monolayer GaSe MOSFET. (c) Projected band structures of GaSe monolayer. (d) Transfer characteristics of GaSe n-MOSFET at $L_g = 1$, 3, and 5 nm.

out subsequent calculations. Based on high-performance (HP) technology for the 2028 horizon, the dielectric layer thickness and the V_{DS}, are set to 0.41 nm and 0.64 V, respectively. In addition, to avoid the interaction between adjacent slabs, a vacuum region (greater than 20 Å) is set along the direction perpendicular to that of transport. In Fig. 1(c), we present the projected band structures of the GaSe monolayer with an indirect band gap of 1.808 eV. The conduction-band minimum (CBM) is located at Γ, and the valence-band maximum (VBM) is located between the Γ and M points. The shapes of the CBM and VBM are completely different, where the former is sharp and the latter is relatively flat. Note that the CBM of GaSe has a similar band dispersion along the armchair and zigzag directions in Fig. S2 within the Supplemental Material [39], the electron effective mass in both directions is the same, with negligible anisotropy along the zigzag and armchair directions. Thus, in the following, we consider only the transport properties along the armchair direction, which is similar to that in previous publications for the graphenelike buckling structure [6,31,40,41]. Compared with 2D materials, such as BiN ($m_e = 0.23\ m_0$) [41], MoS_2 ($m_e = 0.56\ m_0$) [42], and ReS_2 ($m_e = 0.89\ m_0$, armchair direction) [43], the lighter electronic effective mass facilitates GaSe FETs obtaining higher currents [44,45]. In Figs. S3(a) and S3(b) within the Supplemental Material [39], the orbital-projected band structures of Ga and Se atoms are plotted. The CBM of GaSe is mainly contributed to by the Ga s orbital and to a lesser extent by Se p_z orbitals, while the VBM is mainly attributed to Se p_z orbitals and some Ga p_z orbitals. Additionally, the partial charge densities of the CBM and VBM are shown in Fig. S3(c) within the Supplemental Material [39]. The difference in charge-density distributions at the VBM and CBM will affect the transport characteristics of n- and p-type GaSe devices.

The large I_{on} is necessary for the high switching speed of logical transmission systems in digital devices. In terms of International Technology Roadmap for Semiconductors (ITRS) high-performance applications, the *off* -state current (I_{off}) is set to 0.1 μA/μm. When $I_{DS} = I_{off}$, the corresponding V_g is defined as the *off* -state gate voltage ($V_{g,off}$). Therefore, I_{on} can be extracted from the transfer characteristics at $V_g = V_{g,on}$. $V_{g,on}$ stands for the *on*-state gate voltage, which can be calculated by $V_{g,off} + V_{DS} = V_{g,on}$ [45–47]. In Fig. 1(d), the transfer characteristics can reach the I_{off} standard when the gate length is 3 and 5 nm. I_{on} of GaSe n-MOSFETs with 5 and 3-nm L_g is 1730 and 904 μA/μm, respectively. Details are given in Table I. When L_g is reduced to 1 nm, it is an arduous task to meet ITRS standards due to the increased tunneling between source and drain. The low SS value, which is defined as $SS = \partial V_g / \partial \lg I_{DS}$, indicates that the transistor has a strong gate-control ability in the subthreshold region. The SS value of the GaSe MOSFET with a 3-nm gate length is 134.8 mV/dec, which is more than twice the Boltzmann tyranny (60 mV/dec). To improve the SS and I_{on} properties of GaSe MOSFET with $L_g = 3$ nm, we study the influence of the dielectric layer on the device transport properties, including the thickness and dielectric constant of the dielectric layer and UL construction.

B. The dielectric layer influence on transport properties

To analyze the influence of dielectric layer thickness, we calculate the transfer characteristics, I_{on}, and SS of GaSe MOSFETs. In Fig. 2(a), when the gate voltage ranges from

TABLE I. Performance metrics of sub-5-nm-gate ML GaSe n-MOSFETs with different ULs in our work against the requirements of the ITRS for HP transistors in 2028. L_g, gate length; L_{UL}, underlap length; V_{DD}, supply voltage; t_{ox}, dielectric layer thickness; τ, delay time; PDP, power-delay product.

	L_g (nm)	L_{UL} (nm)	V_{DD} (V)	t_{ox} (nm)	I_{on} (μA/μm)	I_{on}/I_{off}	SS (mV/dec)	τ (ps)	PDP (fJ/μm)
ITRS 2028 (HP)	5.1	0	0.64	0.41	900	9.00×10^3		0.423	0.24
	5	0	0.64	0.41	1730	1.73×10^4	76.8	0.054	0.228
		1	0.64	0.41	1770	1.77×10^4	69.8	0.051	0.214
		2	0.64	0.41	1880	1.88×10^4	65.6	0.044	0.201
		3	0.64	0.41	1610	1.61×10^4	66.1	0.044	0.178
	3	0	0.64	0.41	904	9.04×10^3	134.8	0.074	0.194
		1	0.64	0.41	1700	1.7×10^4	107.0	0.047	0.211
		2	0.64	0.41	1699	1.7×10^4	92.1	0.044	0.199
		3	0.64	0.41	1398	1.4×10^4	77.3	0.041	0.137
		4	0.64	0.41	972	9.72×10^3	71.0	0.044	0.111
	1	0	0.64	0.41	...	...	266.9	...	...
		1	0.64	0.41	...	...	177.1	...	...
		2	0.64	0.41	842	8.42×10^3	123.2	0.051	0.117
		3	0.64	0.41	841	8.41×10^3	110.4	0.054	0.119
		4	0.64	0.41	853	8.53×10^3	96.4	0.048	0.087

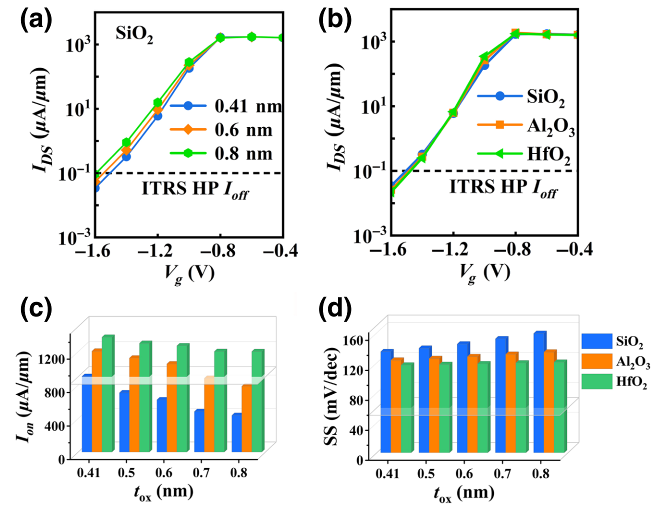

FIG. 2. Transfer characteristics of GaSe MOSFETs with different dielectric layer thicknesses (a) and different dielectric constants (b). I_{on} (c) and SS (d) as functions of t_{ox} for devices with different dielectric layers. Transparent planes in (c),(d) represent the HP standard of the ITRS 2028 horizon and the Boltzmann tyranny.

−1.6 to −0.6 V, the transfer characteristics are different for dielectric layer thicknesses of 0.8, 0.6, and 0.41 nm. The *off* -state current of the device with t_{ox}= 0.8 nm is relatively difficult to reach, 0.1 μA/μm, which indicates that a large leakage current occurs in the architecture. When t_{ox} is equal to 0.6 nm, both the leakage current and *off* -state gate voltage decrease; however, I_{on} is barely close to 600 μA/μm. As t_{ox} is set to 0.41 nm, the leakage current is further suppressed, so the *off* -state gate voltage approaches −1.5 V and I_{on} goes up to 904 μA/μm. The transport properties of the device can be improved when the dielectric layer thickness is reduced, owing to the reduction of the natural length (λ). For the dual-gate MOSFET, λ can be defined as $\lambda = (\varepsilon_{ch}t_{ch}t_{ox}/2\varepsilon_{ox})^{1/2}$, where t_{ch} (t_{ox}) is the thickness of the channel (dielectric layer); ε_{ch} and ε_{ox} represent the dielectric constant of the channel and dielectric layer, respectively [31,48–50]. The diminution of λ is a key factor to improve gate control, and the detailed relationship between them is demonstrated in the Supplemental Material [30,39,51]. To illustrate the mechanism more intuitively, the transmission spectra of devices with different dielectric layer thicknesses are given in Fig. S4 within the Supplemental Material [39]. At the same gate voltage ($V_g = -1.6$ V), the transmission probability decreases with a reduction of the dielectric layer thickness. As a consequence, the device with t_{ox}= 0.41 nm has a small leakage current, which can be seen in Fig. 2(a). The *on*-state and *off* -state transmission spectra of the dielectric layer at 0.41, 0.6, and 0.8 nm are shown in Figs. S4(b)–S4(d) within the Supplemental Material [39]. The devices show similar *on*-state and *off* -state transmission spectra under these three conditions. However, it can be seen from the illustration that the transmission probability in the bias window increases as the dielectric layer thickness decreases from 0.8 to 0.41 nm.

Moreover, Fig. 2(b) presents the transfer characteristics of monolayer GaSe MOSFETs with different dielectric layers. The devices with HfO_2 ($\varepsilon = 25$) and Al_2O_3 ($\varepsilon = 9$) as dielectric layers show inhibition of the leakage current. According to the formula $C_{ox} = (\varepsilon_{ox}\varepsilon_0)/t_{ox}$ [52,53], an increase of ε_{ox} can lead to an increase in dielectric capacitance (C_{ox}). In the *off* state, there is a significant number of positively charged holes accumulating beneath the dielectric layer. It also can be seen from Fig. S6(a) within the Supplemental Material [39] that, when $V_g = -1.6$ V, the edge of the transmission spectrum of SiO_2 is closer to the bias window than that of HfO_2 as the substrate. Thus, the barrier height rises when HfO_2 (Al_2O_3) is used as the dielectric layer. When the absolute value of the gate voltage is lower than 1.2 V, the drain current of the device with a high dielectric constant is slightly higher than the device with the SiO_2 ($\varepsilon = 3.9$) substrate; this is related to the enhancement of the gate-control ability and the reduction of the barrier. In Fig. S5 within the Supplemental Material [39], the transfer characteristics of the device with SiO_2, Al_2O_3, and HfO_2 as substrates under different t_{ox} are given. The results show that, with increasing t_{ox}, the high-*k*-material effect on the device performance is gradually enhanced. When V_g is equal to −1.6 V, the transmission spectrum varies with the thickness and dielectric constant, as shown in Fig. S6 within the Supplemental Material [39]. The decrease of t_{ox} induces the difference in transmission spectra between HfO_2 and SiO_2 substrates. When t_{ox}= 0.8 nm, the device with the HfO_2 substrate has a lower transmission spectrum than that of SiO_2, and the edge of the transmission spectrum is farther from the bias window. When t_{ox}= 0.41 nm, their transmission spectra almost overlap, which is consistent with the small change of transfer characteristics in Fig. 2(b).

To further evaluate the role of the dielectric layer, Figs. 2(c) and 2(d) show the variation of I_{on} and SS with t_{ox} at different dielectric constants. For SiO_2, Al_2O_3, and HfO_2 as the substrate, both I_{on} and SS are gradually improved with a decrease in t_{ox}. For instance, when Al_2O_3 is the substrate, I_{on} increases from 786 to 1206 μA/μm, and the SS values decrease from 134.2 to 123.4 mV/dec. Under the same t_{ox} condition, the SS of the device decreases when the high-*k* material replaces SiO_2 as the substrate, indicating that the gate-control capability in the subthreshold region is improved. The effect of dielectric layer change on the device with t_{ox}= 0.8 nm is greater than that of 0.41 nm. For example, when Al_2O_3 is replaced by HfO_2, I_{on} increases by 415 and 166 μA/μm for t_{ox}= 0.8 and 0.41 nm, respectively. In light of this, t_{ox} and ε are mutually matched to get the equivalent oxide thickness (EOT = $t_{ox}\varepsilon_{SiO_2}/\varepsilon_{ox}$).

TABLE II. Performance metrics of 3-nm-gate monolayer GaSe n-MOSFETs with different ULs, dielectric layer thicknesses, and dielectric constants.

Dielectric constant	L_g (nm)	L_{UL} (nm)	V_{DD} (V)	t_{ox} (nm)	EOT (nm)	I_{on} (μA/μm)	I_{on}/I_{off}	SS (mV/dec)
3.9	3	0	0.64	0.8	0.8	437	4.37×10^3	159.1
		0	0.64	0.7	0.7	484	4.84×10^3	152
		0	0.64	0.6	0.6	624	6.24×10^3	144.9
		0	0.64	0.5	0.5	708	7.08×10^3	139.4
		0	0.64	0.41	0.41	904	9.04×10^3	134.8
		3	0.64	0.41	0.41	1398	1.4×10^4	77.3
9	3	0	0.64	0.8	0.35	786	7.86×10^3	134.2
		0	0.64	0.7	0.3	882	8.82×10^3	131.2
		0	0.64	0.6	0.26	1053	1.05×10^4	128.2
		0	0.64	0.5	0.22	1123	1.12×10^4	125.6
		0	0.64	0.41	0.18	1206	1.21×10^4	123.4
		3	0.64	0.41	0.18	1786	1.79×10^4	69.7
25	3	0	0.64	0.8	0.13	1201	1.2×10^4	120.7
		0	0.64	0.7	0.11	1202	1.2×10^4	119.7
		0	0.64	0.6	0.09	1270	1.27×10^4	118.6
		0	0.64	0.5	0.08	1299	1.3×10^4	117.7
		0	0.64	0.41	0.06	1372	1.37×10^4	116.9
		3	0.64	0.41	0.06	1766	1.77×10^4	62.7

In Fig. S7 within the Supplemental Material [39], we plot I_{on} and SS as a function of EOT. As EOT decreases, the SS shows a downward trend, whereas I_{on} exhibits an upward trend. Therefore, the gate-control capability can be adjusted by scaling the EOT. The details are shown in Table II.

The UL is regarded as the region between the gate and the electrode, as noted in Fig. 1(b). The isometric UL is adopted near the source and drain. It is reported that, if the UL length is too long and beyond the control of the gate, the performance of the device will degrade [29]. Thus, the length of the UL is strongly required to be systematically discussed. In Fig. S8 within the Supplemental Material [39] and Table I, we completely investigate the transfer characteristics of GaSe MOSFETs with 1- and 5-nm gate lengths under different UL lengths. At $L_g = 5$ nm, I_{on} is as high as 1730 μA/μm, and the SS is only 76.83 mV/dec. In this case, we can see from Table I that the utilization of the UL structure is less effective at promoting the transport properties. For the GaSe MOSFETs with 1-nm gate lengths, it is difficult for I_{on} to reach the HP requirements of the ITRS 2028 horizon, especially without the UL. When the UL length increases from 1 to 4 nm, I_{on} is invariably plagued by the impact of a large *off* -state gate voltage. Therefore, we focus on the merits and limits of the device with $L_g = 3$ nm. Figure 3(a) shows the transfer characteristics of GaSe MOSFETs with different UL lengths. With an increase in UL length, the SS value decreases gradually, and the *off* -state gate voltage reduces from -1.5 to -1.2 V. However, I_{DS} near I_{on} also decreases, which means that the gate-control capability of the superthreshold region is weakened. To visualize the impact of the UL length, SS and I_{on} are extracted in Fig. 3(b). The results show that I_{on} reaches a maximum value at an UL length of 1 nm. However, when L_{UL} is larger than 2 nm, I_{on} exhibits a decreasing trend. As the L_{UL} reaches 3 nm, although I_{on} decreases to 1399 μA/μm, the SS of the device is greatly improved. For $L_{UL} = 4$ nm, the value of SS remains on a downswing, while I_{on} is only 972 μA/μm. Therefore, the optimal UL length is 3 nm.

To further elucidate the modulation mechanism of the gate, we investigate the *on*- and *off* -state LDOS for the GaSe MOSFETs with a 3-nm gate length. In Figs. 3(c)–3(f), when the device is designed with an optimal UL ($L_{UL} = 3$ nm), the LDOS and spectral current show remarkable differences with and without the UL. In the *off* state, the channel barrier height (Φ_B) of the optimal UL structure is 0.19 eV, which is about half of that without the UL ($\Phi_B = 0.45$ eV). Φ_B is defined as the energy difference between the chemical potential of the source and the lowest point energy of the conduction band. The relationship between the tunneling current (I_{tunnel}) and the barrier can be expressed as

$$I_{tunnel} \propto \exp\left(-\Lambda\sqrt{m * \Phi_B}\right) \tag{2}$$

where m^* and Λ are the electron effective mass and barrier width, respectively [29,45,54]. The detailed derivation can be seen in the Supplemental Material [39]. In light of Eq. (2), the Φ_B and Λ enhancement can give a decreasing I_{tunnel}. The optimal UL structure possesses a relatively large Λ, which is about 2 nm greater than that without the UL. Thus, one of the reasons for the reduction in leakage current caused by the use of the UL is that the effect of Λ

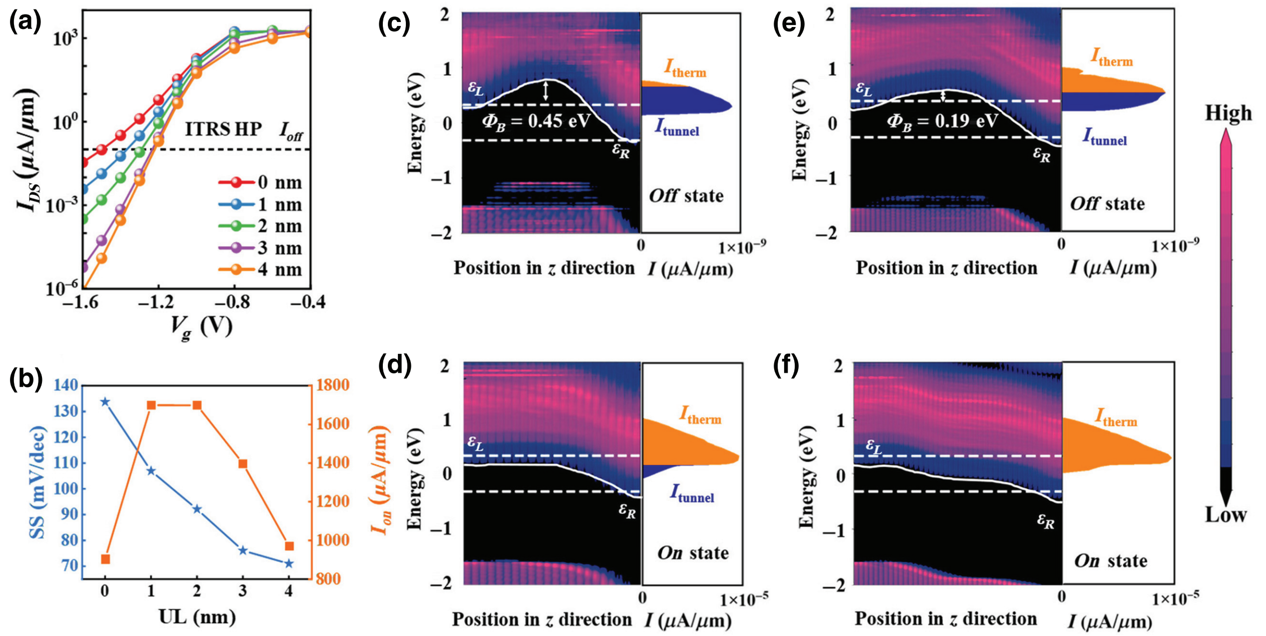

FIG. 3. (a) Transfer characteristics of GaSe MOSFETs with 3-nm L_g and UL from 0 to 4 nm. (b) SS and I_{on} as a function of L_{UL}. Local density of states (LDOS) and the spectral current in the channel region for the device without an UL at the off state ($V_g = -1.497$ V) (c) and on state ($V_g = -0.857$ V) (d) and with $L_{\mathrm{UL}} = 3$ nm at $V_g = -1.23$ and -0.59 V for the off state (e) and on state (f). Ratio of I_{tunnel} to I_{therm} is proportional to the shaded area. ε_L and ε_R are the electrochemical potentials of the (left) source and (right) drain.

offsets the increase in I_{tunnel} caused by the Φ_B. In the *on* state, the former has more states in the bias window than the latter, so a larger I_{on} can be obtained in the structure with the optimal UL. The results can be also seen from the spectral current. In the case without the UL, the total current in the *off* state is basically contributed to by I_{tunnel}. On the contrary, when the optimal UL is considered, the contribution of I_{tunnel} decreases in the *off* state, and all the current in the *on* state comes from the thermal current (I_{therm}). Therefore, considering the UL structure, the gate-control ability can be greatly improved.

The intrinsic delay time (τ), PDP, and SS of GaSe-based MOSFETs with different L_g are plotted in Fig. S9 within the Supplemental Material [39]. The τ value is exploited to evaluate the switching ability of a logic device. The lower the τ value, the faster the switching speed. It is defined as $\tau = (Q_{on} - Q_{off})W^{-1}I_{on}{}^{-1}$, where Q_{on} and Q_{off} are the total charges in the channel region in the *on* state and *off* state, respectively. W is the width of the channel [55]. Fig. S9(b) within the Supplemental Material [39] shows the relationship between τ and the UL length at $L_g = 5$, 3, and 1 nm. The delay time ranges from 0.044 to 0.074 ps, which is far below the HP goals of the ITRS 2028 horizon (0.423 ps). Another significant concern for MOSFET applications is the PDP, which can be calculated by the formula PDP $= (Q_{on} - Q_{off})V_{DD}/W$ [55]. The PDP as a function of L_{UL} with different gate lengths is depicted in Fig. S9(c) within the Supplemental Material [39]. For all the GaSe MOSFETs, the estimated PDP (0.087−0.228 fJ/μm) is much lower than the ITRS requirements for HP (0.420 fJ/μm) devices, the details of these values are also listed in Table I. With the extension of the UL length, the PDP generally presents a trend of continuous decline.

Considering the optimal dielectric parameters comprehensively, we replot the transfer characteristics of devices with HfO_2 and SiO_2 dielectric layers at $L_{\mathrm{UL}} = 0$ and 3 nm in Fig. 4(a). The results show that the SS of the GaSe-based MOSFET with HfO_2 as the dielectric layer is marginally lower than that with SiO_2. When taking HfO_2 as the substrate, I_{DS} near the *on*-state current increases at $L_{\mathrm{UL}} = 0$ and 3 nm. Therefore, the use of a high-k dielectric layer can improve the gate-control capability in the superthreshold region. When $L_{\mathrm{UL}} = 3$ nm, the *off* -state gate voltage and leakage current decrease sharply, and the SS value drops to 77.3 mV/dec for the GaSe-based MOSFET with the SiO_2 substrate, as shown in Fig. 4(b). As for the device with the HfO_2 substrate, the *off* -state gate voltage increases by tens of mV; however, the SS is further improved, and I_{on} is also increased by nearly 500 μA/μm.

In Fig. 4(c), we compare the SS and I_{on} of monolayer GaSe MOSFET with other n-MOSFETs. The I_{on} values of these 2D MOSFETs can meet the HP standards of ITRS (2028 horizon) at the 5-nm scale, such as monolayer blue P, Bi_2O_2Se, arsenene, and antimonene MOSFETs. For the case of $L_g = 3$ nm, the SS of GaSe n-MOSFET is lower

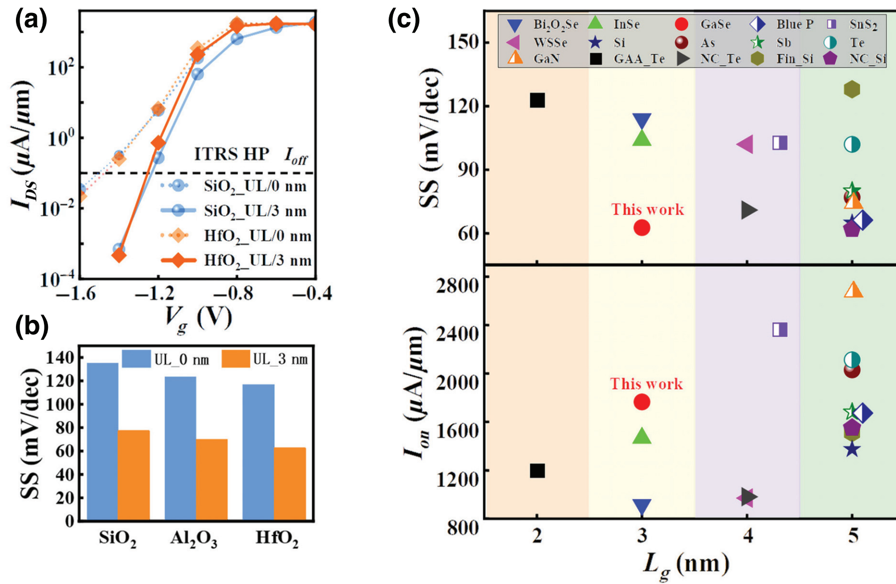

FIG. 4. Transfer characteristics (a) and SS (b) of 3-nm GaSe MOSFETs with $L_{UL} = 3$ nm when different dielectric layers are used. (c) SS and I_{on} of 2D monolayer n-MOSFETs at sub-5-nm gate length [6,30,56–63]. NC stands for negative capacitance. Fin and GAA denote the fin-type and gate-all-around field-effect transistors, respectively.

than those of Bi_2O_2Se and InSe. Moreover, the I_{on} value of GaSe MOSFET can be nearly twice as much as that of Bi_2O_2Se. It is even higher than those of WSSe and blue phosphorus MOSFETs, which have gate lengths of 4 and 5 nm, respectively.

IV. CONCLUSIONS

We study the performance of monolayer dual-gate GaSe n-MOSFETs at the sub-5-nm scale, including the *on*:*off* ratio, *on*-state current, delay time, and power-delay product. In addition, the relationship between dielectric layer properties and the device performance are investigated, and the related physical mechanism is also given. The results show that the 3-nm GaSe MOSFET has excellent performance under a suitable dielectric layer structure. The thinner dielectric layer gives a smaller natural length, corresponding to better gate control. With a suitable dielectric layer structure, the SS value is reduced from 134.8 to 62.7 mV/dec, and I_{on} can be improved from 904 to 1766 μA/μm, which is distinctly satisfactory for the ITRS goal in 2028. This work indicates that engineering of the dielectric layer can achieve ultrashort-scale MOSFETs with strong gate-control ability and high performance.

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