Tuning Positive and Negative Transconductance in Multilayer MoS₂ with Indium Contacts

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We report unusual behavior in the transconductance of multilayer MoS_2 at a low temperature. Multilayer MoS_2 with indium top contacts exhibits negative transconductance at an intermediate back-gate bias and reentrant positive transconductance at a higher back-gate bias. We further determine that the transconductance can be modulated via controlling the channel length, which originates from competition between the intralayer in-plane transport and interlayer vertical transport. These features emerge owing to the van der Waals contact between indium and MoS_2 and become more prominent as the sample thickness increases. Our results provide further insights for carrier transport in multilayer MoS_2 and its practical applications.

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I. INTRODUCTION

Transition-metal dichalcogenide (TMD) consists of a metal layer covalently bonding two-nearest chalcogen layers as a unit layer, which are weakly bonded by van der Waals (vdW) interactions between two chalcogen layers to form the bulk material. Various physical properties can be exploited using these materials composed of semiconductors, metals, ferroelectrics, magnetics, and superconductors [1-5]. In particular, the weak vdW interactions between the layers allow easy exfoliation down to the monolayer, which has attracted much interest owing to a direct band gap and remarkable properties related to the broken inversion symmetry [6,7]. In addition, the inherent nature of a monolayer, such as strong Coulomb interactions, reduced dielectric screening, large exciton-binding energy, large work-function variance, phase engineering, substrate-dependent strain, and charge transfer [8-15], is beneficial for various optical, electronic, and optoelectronic applications, such as photodetectors [16,17], valleytronics [18–21], and piezoelectrics [22,23].

Meanwhile, multilayers are more attractive for optical absorbance and electrical mobility [11,12,24]. Specifically, the higher mobility due to reduced charge scattering from the substrates [25] is favorable for field-effect-transistors (FETs). As the thickness increases further, however, complexity of the FET operation arises. In thick-multilayer TMD devices, there are effectively three distinguishable paths for the transport channel: the top surface layer is exposed to gas adsorbates under ambient conditions, the bottom layer sits on the dielectric insulator of the substrate, and the middle layer is sandwiched by the top and bottom layers. The carrier density varies in different layers, leaving anisotropic mobility according to the vertical depth profile [26]. Therefore, the channel current and transfer characteristics depend strongly on the sample thickness [25].

Recent experimental reports show various intriguing phenomena in multilayers that can be understood along this vein. For example, ambipolar behavior is demonstrated for the edge metal contact of thick molybdenum disulfide (MoS₂) samples, and this is attributed to selective charge transport through differently doped layers, that is, the *n*-doped top and bottom layers for electron transport and intrinsic or weakly *p*-doped middle layer for hole transport [27]. Quantum interference and the Coulomb drag phenomenon are observed in 50-70-nm-thick tungsten diselenide (WSe₂), which result from the carrier interaction between the top and bottom layers across the intrinsic middle layer [28]. Negative transconductance (NTC) in a thick MoS₂ device is observed at low temperature and demonstrated to be utilized for frequency doubling or in a phase-shift keying circuit, in which graphene electrodes are employed as the top contact. The origin of NTC is assigned to the existence of a potential barrier in the vertical direction due to the *p*-doped (or intrinsic) middle and *n*-doped bottom layers [29]. Such phenomena in the channel materials, however, are often obscured by a large contact resistance or an intrusive property of typical metal

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FIG. 1. (a) Device schematics and energy-band diagrams. (b) Contact resistance obtained from TLM at $V_{BG} = 60$ V and T = 300 K. Inset is an optical image of the device (c) Temperature dependence of contact resistance measured at $V_{BG} = 60$ V.

contacts resulting from thermal vapor deposition. In this study, we are able to tailor the NTC and positive transconductance (PTC) in multilayer MoS_2 with indium contacts by varying the gate bias, thickness, and channel length. Indium as the metal top contact is the key to a noninvasive nearly ohmic contact owing to the vdW interface property [30].

II. PROPERTIES OF INDIUM CONTACT

Multilayer MoS₂ flakes are exfoliated on SiO₂(300 nm)/ Si (heavily *p*-doped) substrates. For the electrodes, indium is evaporated at a temperature of $T \sim 100$ K. This method allows us to prepare a uniform indium film (~100 nm) with an extremely clean vdW interface with a MoS₂ channel [31]. Figure 1(a) illustrates the device schematic (left) and the energy-band diagram for the indium junction (work function, $\phi_{In} \sim 4.1 \text{ eV}$) and multilayer MoS₂ (affinity, $\chi_{MoS_2} \sim 4.0 \text{ eV})$ (right) before and after the contact. Charge transfer between MoS₂ and indium is expected to yield electron doping in MoS_2 [31]. The presence of a van der Waals gap mitigates the Fermi-level pinning effect [30]. More remarkably, a decrease in the contact resistance (R_c) at a lower temperature for multilayer MoS₂ indicates that the nature of the contact is not a Schottky type but rather nearly ohmic [31]. To further confirm this property, we measure the contact resistance of an about 3-nm-thick MoS₂ device with a series of In electrodes using the transfer-length measurement (TLM) [inset in Fig. 1(b)]. Including the TLM, all data presented in this study are obtained using a two-probe method. At a high source–drain-current regime of $V_{BG} = 60 \text{ V}$, $2R_c = 3.2 \text{ k}\Omega \ \mu\text{m}$ at room temperature, which is comparable to the lowest value reported [30]. The contact resistance drops slightly with decreasing temperature and finally saturates to $2R_c \sim 2.5 \text{ k}\Omega \ \mu\text{m}$ below 100 K [Fig. 1(c)].

The high quality of the In contact can be further assessed from the output I_{DS} - V_{DS} characteristics. Figure 2(a) shows the results for the device with dimensions of 1 μ m long, 4 μ m wide, and 10 nm thick, which is measured at T = 10 K for various back-gate biases, V_{BG} . I_{DS} increases with elevating V_{BG} , demonstrating the *n*-doped MoS_2 channel. The nonlinear I_{DS} - V_{DS} characteristics near $V_{DS} = 0$ exhibit two different behaviors for the low and high regimes of V_{BG} . For clarity, we show two chosen traces for $V_{\rm BG} = -10$ V (left axis) and 40 V (right axis), as shown in Fig. 2(b). At $V_{BG} = -10$ V, the rate of the current increment is small at low V_{DS} and becomes larger at higher V_{DS} . Conversely, at $V_{BG} = 40$ V, it has a maximum at $V_{DS} = 0$ and gradually decreases as V_{DS} increases. This behavior is attributed to the transition from the insulating phase to the metallic phase of the channel material, MoS_2 , across $V_{BG} = 0$. This phenomenon is, in general, hardly observed in two-probe measurements for most metal contacts at low temperature owing to the large contact resistance in the presence of the Schottky barrier. In such a case, I_{DS} - V_{DS} characteristics are always similar to those at $V_{\rm BG} = -10$ V in Fig. 2(b), regardless of the channel state.



FIG. 2. (a) $I_{DS} - V_{SD}$ characteristics for the MoS₂ device with a thickness of $t \sim 10$ nm, channel width of 4 μ m, and channel length of $L_{ch} = 1 \mu$ m. (b) $I_{DS} - V_{SD}$ for the chosen back-gate biases. (c) Differential conductance, $G_{diff} = dI_{DS}/dV_{DS}$, extracted from (a). (d) Total resistance as a function of V_{BG} measured at $V_{DS} = 1$ mV and T = 10 K.

Figure 2(c) shows the transition of the channel state more clearly through the differential conductance, $G_{\text{diff}} =$ dI_{DS}/dV_{DS} , extracted from Fig. 2(a). G_{diff} near zero voltage exhibits two distinct behaviors, a valley for $V_{BG} \lesssim 0$ V and a peak for $V_{BG} > 0$ V, which represent the metallic feature and the insulating feature of the channel, respectively [32]. In other words, the metal-insulator phase transition of MoS_2 occurs at $V_{BG} \sim 0$ V. The increase of conductance with V_{DS} in the insulating phase is generally attributed to the field-enhanced hopping or the electron-heating effects, while the decrease of conductance in the metallic phase is attributed to the electron-heating effects in the channel [32,33]. With our two-probe measurements, the observation of such channel properties at low temperature and low V_{DS} is fairly remarkable, demonstrating the high value of indium contacts for the study of the intrinsic properties of MoS_2 . As shown in Fig. 2(d), the total resistance, R_T , at $V_{DS} = 1 \text{ mV}$ and T = 10 K is only several k Ω in the metallic regime, again underlining the minor effect of the contact resistance. In the case of the Schottky contact, the contact resistance, in general, becomes larger for a smaller V_{DS} because tunneling is weaker [32]. In addition, accurate measurements with such a small V_{DS} are more challenging at low temperature, since the suppression of the thermionic emission yields a seriously high contact resistance.

The properties of the indium contact, i.e., a van der Waals interface and a low contact resistance, are immensely beneficial for revealing not only the intrinsic properties of the channel material but also the diverse mechanisms of charge transport. Next, we discuss unusual transport features observed using this indium contact.

III. NEGATIVE AND REENTRANT POSITIVE TRANSCONDUCTANCE

Figure 3(a) shows the transfer characteristics for various temperatures (*T*) measured at $V_{DS} = 5 \text{ mV}$ for the same device as the one discussed for Fig. 2. There is a crossover in the magnitude of the current, indicated by a red arrow, for the traces at low temperatures, as V_{BG} (carrier density) changes. This is likely to indicate the phase transition from the insulating state to the metallic state in MoS₂, consistent with the result in Fig. 2(c). One unusual feature in this figure is the downturn in current for $V_{BG} > 20 \text{ V}$ at 10 K, as indicated by black arrows. This NTC is observed at low temperature in multilayer MoS₂ using graphene contacts, and it is observed that the more pronounced NTC of the higher peak-to-valley ratio (PVR) appears in the thicker sample. The origin of NTC is attributed to the existence of the *p*-doped layers above the *n*-doped bottom layer,



FIG. 3. (a) Transfer $I_{DS} - V_{BG}$ characteristics for the MoS₂ device with a thickness of $t \sim 10$ nm and channel length of $L_{ch} = 1 \ \mu m$. (b) $I_{DS} - V_{BG}$ measured at T = 10 K and $V_{DS} = 50$ mV for two different devices of $t \sim 22$ and 10 nm. Channel length of all devices is 1 μm . (c) $I_{DS} - V_{BG}$ for the 22-nm-thick MoS₂ device with $L_{ch} = 1 \ \mu m$. (d) $I_{DS} - V_{BG}$ at T = 20 K for several chosen V_{DS} .

leading to more resistive vertical transport at lower temperature [29]. We discuss this in more detail in later. This thickness dependence is clearly seen in Fig. 3(b) for two samples with different thickness of 10 and 22 nm. Data are recorded at a temperature of T = 10 K for a channel length of $L_{ch} = 1 \ \mu$ m using $V_{DS} = 5$ mV and 50 mV for 10- and 22-nm-thick samples, respectively.

In addition to the thickness dependence, the NTC exhibits similar temperature and V_{DS} dependences as those discussed in Ref. [29]. Figure 3(c) shows the I_{DS} - V_{BG} characteristics for the 22-nm-thick MoS_2 device of $L_{ch} =$ 1 μ m at various temperatures. NTC is clearly observed at T < 100 K and becomes more apparent at lower temperature. On the other hand, Fig. 3(d) shows the V_{DS} dependence of NTC, where NTC is weaker as V_{DS} increases. This V_{DS} dependence is attributed to the drain-induced barrier-lowering effect with a tunneling contribution [29]. This feature of NTC is more easily observed when the contact is less invasive to the materials. The observation of the clear NTC in the 22-nm-thick MoS₂ device with indium contact supports the van der Waals interface between indium and MoS₂ similar to that of graphene contacts to MoS₂.

As the sample is even thicker, we observe an additional feature. Here, we discuss this for the 75-nm-thick sample in more detail. Figure 4(a) shows the device schematic with a current flow indicated by the black arrows. The red and the gray colors designate *n*-doped and *p*-doped areas, respectively. In a previous report, it was demonstrated that the middle layer was intrinsic or *p*-doped, but the top layer could be *n*-doped when it was exposed to air. In such a case, electrons from the top diffuse into the bulk, with a diffusion length of about 10 nm [26]. Thus, considering n doping from charge transfer due to the difference in Fermi levels between In and MoS_2 , we do not exclude the possibility of an *n*-doped top layer in our 75-nm-thick MoS_2 . Figure 4(b) shows the transfer I_{DS} - V_{BG} characteristics of this device for various temperatures at $V_{DS} = 50$ mV. The clear shoulder feature in the curve for T = 200 K implies electron conduction via multiple channels, which are likely to be top and bottom layers. This feature weakens as the temperature decreases. The reason follows below. In addition, NTC starts to appear at $T \sim 50$ K and becomes manifest with substantial current suppression at T = 10 K. The curve at T = 10 K is shown again in Fig. 4(c) with the transconductance, $g_m = dI_{DS}/dV_{BG}$ (right axis). NTC develops due to the vertically inhomogeneous carrier concentration, as we previously mentioned, and the finite critical screening length, λ , which is experimentally



FIG. 4. (a) Device schematics of 75-nm-thick MoS₂. (b) $I_{DS} - V_{BG}$ characteristics of the MoS₂ device with a channel length of $L_{ch} = 1 \ \mu m$ for various temperatures. (c) I_{DS} and transconductance $g_m = dI_{DS}/dV_{BG}$ with respect to V_{BG} on the left and right axes, respectively, at T = 10 K (top). Schematic band diagrams in the vertical direction for the area in the dashed box in Fig. 4(a) corresponding to low (blue dot) and high V_{BG} (red dot). (d) $I_{DS} - V_{DS}$ for several chosen ... at T = 50 and 10 K at the top and bottom, respectively.

estimated to be about 28 nm in a MoS_2 device with 300nm-thick SiO_2 as a back-gate dielectric [29]. Because of this short screening length, the carrier density in the top and middle layers is poorly controlled by the back-gate bias in this thick device. In addition, the carriers are frozen at a low temperature, which causes the top layer to become nonconductive, even under the large back-gate bias. Thus, the vertical position of the main current path for in-plane transport is determined via competition with the vertical transport, which plays a role in the occurrence of NTC at low temperatures.

The bottom part of Fig. 4(c) shows schematic band diagrams in the area in the dotted box in Fig. 4(a) for the two cases of low V_{BG} (blue dot) and high V_{BG} (red dot). Considering two aspects, the inhomogeneous carrier concentration and finite λ , the Fermi level rises in the bottom layer, but it remains nearly unchanged in the intrinsic middle layer as V_{BG} increases. Thus, we expect a higher potential barrier, ϕ_b , at a higher V_{BG} for vertical transport, as shown in these band diagrams, which causes NTC when the in-plane current path is along the bottom layer far below this potential barrier [solid arrow in Fig. 4(a)], since the top layer is too resistive at low temperatures. As V_{BG} increases further, the current begins to increase again. This feature, the increase in current after the antibipolar behavior with V_{BG} (we call it reentrant positive transconductance, RPTC), is observed in heterostructures of p- and n-type semiconducting materials [34–36] but is unusual in a single material. When these features of NTC and RPTC appear at T = 10 K, the $I_{DS} - V_{DS}$ characteristic is extremely nonohmic, as shown in the bottom part of Fig. 4(d), in contrast to the top part for T = 50 K, which supports the primary role of the energy barrier in vertical transport as an origin of these features.

Next, based on our findings of their strong dependence on L_{ch} and V_{DS} , we discuss how the RPTC occurs. Figure 5(a) shows an optical image of the same 75-nm-thick MoS₂ device with several different channel lengths defined by the indium electrodes. Figure 5(b) exhibits I_{DS} - V_{BG} characteristics for $L_{ch} = 0.5$, 1, and 4 μ m, respectively. For the shortest channel length, $L_{\rm ch} = 0.5 \ \mu {\rm m}$, the current level is the highest but the PVR is smaller than that for longer $L_{\rm ch} = 1 \ \mu m$, as shown in Fig. 5(c), since the RPTC starts to occur at a lower V_{BG} . For $L_{ch} = 4 \ \mu m$, a consistent RPTC is not clearly observed, despite the existence of several local peaks and valleys. Thus, we conclude that the RPTC is stronger for shorter L_{ch} , and the current path for RPTC should differ from the path in the NITC regime to circumvent the large energy barrier in vertical transport. Considering $\lambda \sim 28$ nm and the large current modulation by V_{BG} in the regime of RPTC, the current path of minimal resistance should be near the middle layer in the short-channel case [dashed arrow in Fig. 4(a)]. For the long-channel case, transport along the more resistive middle channel is not beneficial over that along the bottom



FIG. 5. (a) Optical image of the 75-nm-thick MoS₂ device. (b) $I_{DS} - V_{BG}$ for $L_{ch} = 0.5$, 1, and 4 μ m at T = 10 K from the top to the bottom, respectively. (c) Peak-to-valley ratio with respect to V_{DS} for two different channel lengths of $L_{ch} = 0.5$ and 4 μ m.

channel and entire vertical paths. Thus, NTC behavior is maintained over a wider range of V_{BG} .

In Ref. [29], the MoS₂ device with a thickness of 41 nm using a graphene contact exhibits prominent NTC behavior but no RPTC over the experimental range of V_{BG} similar to that of our thinner 22-nm-thick MoS_2 device with $L_{ch} =$ 1 μ m using indium contacts (Fig. 3). Since the RPTC is not observed in this thinner device, we infer that the entire vertical path down to the bottom layer in this device is still not so resistive as to take other route to evade that path. It still chooses the whole vertical path plus the bottom layer for a current path within our V_{BG} range. This conclusion can be justified by comparing the I_{DS} - V_{BG} characteristics measured under the same conditions for devices of different thickness, i.e., 75- and 22-nm-thick devices [Figs. 3(b) and 4(c)]. The thinner device exhibits a much higher current in the NTC regime than in the RPTC regime of the thicker device. The short-channel effect may play a role in the RPTC regime in the thicker device, since the characteristic length for the short-channel effect is generally longer for a thicker MoS₂ device [37].

Lastly, we note that evaporated indium for the electrodes may create some contacts to the sample sides. According to previous reports [27,38], it, however, usually does not provide decent metal contacts to all layers without an etching process, leading to resistive and impractical charge injection to the sides. This argument is supported by the experimental observation that the MoS_2 devices with well-defined side (or edge) contacts produced after the etching process exhibit ambipolar behavior, while the MoS_2 devices with the usual top contacts exhibit only *n*-type behavior, regardless of sample thickness [27].

IV. CONCLUSION

We measure the transport properties of multilayer MoS_2 using indium contacts, which produce a noninvasive van der Waals interface with MoS_2 . In particular, the low contact resistance at low temperatures is extraordinarily advantageous for investigating the intrinsic physical properties of channel materials. The mechanism of charge transport in the multilayer structure should be understood by taking account of the competition between in-plane transport and vertical transport. Negative transconductance emerges due to the existence of the *p*-*n* junction in the vertical direction, while the bottom layer is the most conductive for acting as the main current path. As the thickness increases, the entire vertical path becomes more resistive, and the charges traverse along a new path of minimal resistance, which is less resistive in the vertical direction;

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