Reconfigurable Noise-Assisted Logic Gates Exploiting Nonlinear Transformation of Input Signals

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We demonstrate the direct implementation of *all* basic logical operations utilizing a single bistable system driven by nonlinearly transformed input signals, in the presence of noise. Exploiting the hopping between the dynamical states of the bistable system, assisted by the noise floor, in response to the transformed inputs, allows the implementation of the full set of logic operations. So this idea can form the basis of the design of a dynamical computing element that can be rapidly morphed to yield any desired logic gate by varying just a single control parameter. Further, the results are verified in electronic circuit experiments, demonstrating the robustness of the concept and the potential of this idea to be realized in wide-ranging systems.

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I. INTRODUCTION

Nonlinear systems are renowned for the richness of their dynamics that range from fixed points, limit cycles of varying periodicities and to chaotic attractors. In recent years, using the behavioral richness of nonlinear dynamical systems for computational tasks has offered an avenue of research, both from the conceptual as well as the applied point of view. Further, in recent years, it has become increasingly evident that the interplay of noise and nonlinearity in a dynamical system is critical in understanding how complex systems evolve and give rise to alternative effects. Stochastic resonance (SR) provides one such example wherein the cooperative behavior between noise and dynamics produces interesting physical phenomena that are often counterintuitive [1–4].

Recently, it has been shown that a noisy bistable system, subjected to two square waves as inputs, produces a logical response in some optimal range of noise [5–24]. The probability of getting such a logic response increases to unity with increasing noise intensity, and then decreases for noise strengths exceeding the optimal noise strength. This effect has been named *logical stochastic resonance* (LSR), and it has been experimentally tested and used in different fields, including electrical [25,26], nanomechanical [27,28], optical [29,30], chemical [31], biological systems [32–35], chaotic attractors [36], and strange nonchaotic attractors [37–39].

The LSR paradigm was conceived to explore the potential utility of system noise in the performance of computational devices. In particular, as computational devices and platforms continue to shrink in size, we are increasingly encountering fundamental noise characteristics that cannot be suppressed or eliminated. The main feature of LSR is its ability to exploit nonlinearity and noise, to build a logic gate functionality by using a nonlinear bistable system. So far, the concept of LSR has been mainly utilized to realize standalone logic gate structures. However, reconfiguration of such logic gate structures to realize morphable all logic gates by varying a single control parameter has not been studied. Here, we investigate the response of a single nonlinear bistable system (acts as a threshold detector) to nonlinearly tranformed input signals, consisting of two random square waves. We find that, in an optimal band of noise, the output is a morphable logical combination of the two input signals by varying a single control parameter in the nonlinear transformation of the inputs.

One of the most promising directions of this idea is the ability to obtain all possible logic operations from a single nonlinear system. In contrast to a conventional field programmable gate array (FPGA) element, where reconfiguration is implemented by switching between multiple single-purpose gates, the operations of our proposed reconfigurable noise-assisted logic gates (RNLGs) can be morphed simply through the varied patterns inherent in the nonlinear transformation of the inputs. Thus architectures based on such elements may serve as ingredients of a flexible computing device that can be optimized for

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special applications or reconfigured on the fly in response to varying operational demands.

The plan of the paper is as follows: Sec. II discusses the general scheme for implementing two-input and a single-output morphable logical gate architecture by using a single nonlinear bistable system. In Sec. III, we consider a proof-of-principle experimental demonstration of RNLG using analog simulation circuits. Finally, in Sec. IV, we present a summary and discussion of our results.

II. SCHEME

Consider a general nonlinear dynamical system (shown schematically in Fig. 1), given by [5]

$$\dot{x} = g(x) + F(I) + D\eta(t), \tag{1}$$

where $g(x)$ is a nonlinear function obtained as the gradient of a bistable potential. $F(I)$ is a nonlinear transformation function, I is a low-amplitude external input signal, and $\eta(t)$ is an additive zero-mean Gaussian white noise with unit variance and intensity parameter D. The noise is considered to have correlation time smaller than any other time scale in the system, and so that it may be represented, theoretically, as δ correlated. For weak noise intensity the motion is confined to either the left well or right well depending upon the initial conditions. At an appropriate noise intensity switching between the two wells is initiated [40].

Usually, a logical input-to-output correspondence can be achieved by encoding N inputs by N square waves. Specifically, for two logic inputs, the system is driven with a small amplitude signal I, taken to be the sum or two trains of aperiodic pulses: $I_1 + I_2$, with I_1 and I_2 encoding the two logic inputs. Since the logic inputs can be either 0 or 1, they can combine to give four logic input sets (I_1, I_2): $(0,0)$, $(0,1)$, $(1,0)$, and $(1,1)$. Since the input sets $(0,1)$ and $(1,0)$ give rise to the same I, the four input conditions (I_1, I_2) reduce to three distinct values of I. Hence, the input signal I, generated by adding two independent uncorrelated input signals, is a three-level aperiodic waveform.

The output of the system can be considered as a logical 1 if it is in, say the right well, and logical 0 if it is in the left well. The output then *toggles* when the system switches wells. The focus here is on the following question: given a set of inputs (I_1, I_2), can the state of the noisy nonlinear system reflect a logical output, in accordance with the truth tables of the basic logic operations shown in Table I? The crucial result obtained in Ref. [5] was that the hopping mirroring logic functions occurred consistently and robustly only in a window of optimal noise. So, while no consistent output was obtained for very small or large noise, in a band of moderate noise, the system produced the desired logical outputs with remarkable consistency.

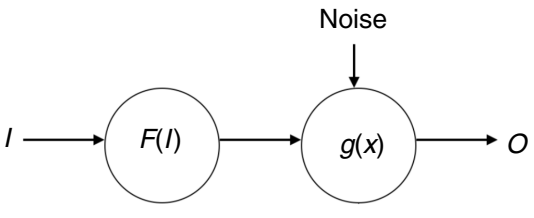

FIG. 1. Schematic diagram of a logic unit comprised of a nonlinear system forced by an input signal $I = I_1 + I_2$ and noise, where I_1 and I_2 encode two logic inputs.

TABLE I. Relationship between the two inputs and the one output of the fundamental OR, AND, NOR, NAND, XOR, and XNOR logic operations, for the four distinct possible input sets $(0,0)$, $(0,1)$, $(1,0)$, and $(1,1)$ [41].

Input set (I_1,I_2)	OR	AND	NOR	NAND	XOR	XNOR
(0,0)	0	0	1	1	0	1
(0,1)	1	0	0	1	1	0
(1,0)	1	0	0	1	1	0
(1,1)	1	1	0	0	0	1

Specifically we now consider a noise-driven bistable system given as

$$\dot{x} = g(x) + F(I_1 + I_2 + I_0) + D\eta(t), \tag{2}$$

where $g(x) = 4x - 20x^3$, I_0 is a control parameter and $F(I)$ is given by the following nonlinear transformation function:

$$F(I) = a^2 I(1-I)[1 - aI(1-I)] - c, \tag{3}$$

where $c = 0.5$ and $a = 4.0$. The form of nonlinear transformation $F(I)$ is represented in Fig. 2 and I is given by $I_1 + I_2 + I_0$.

Thus the drive signals I_1 and I_2 are input streams that encode the two binary inputs are nonlinearly transformed by Eq. (3) and drives the nonlinear bistable system [cf.

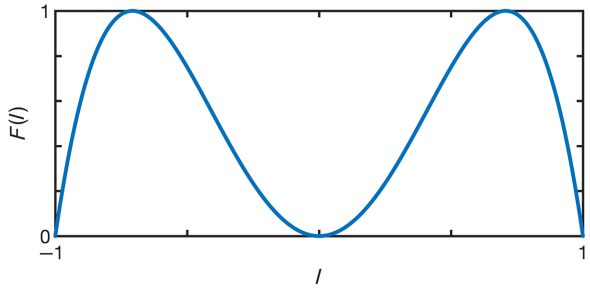

FIG. 2. Nonlinear transformation function $F(I)$ represented by Eq. (3) for $c = 0.0$.

Eq. (2)]. A constant bias I_0 that acts as a single control parameter is responsible for reconfigurability of logic responses in the present scheme.

We first present some results obtained via numerical simulations of the system [cf. Eqs. (2) and (3)]. With no loss of generality, we consider the input signal strength to be 0.1, i.e., the two (randomly switched) inputs I_1 and I_2 to take value -0.1 when the logic input is 0, and value 0.1 when logic input is 1, with the input signal $I = I_1 + I_2 + I_0$ being a three-level aperiodic square-wave form. We observe that, under optimal noise, interpreting the state $x(t) < 0$ as logic output 0 and the state $x(t) > 0$ as logic output 1, the system yields a clean logical response as detailed in Tables I and II. It is worthwhile to note that these input signals cannot cause a transition between potential wells on their own and the transitions are aided by the noise floor, which is the phenomenon called logical stochastic resonance. The time waveforms of the system variable $x(t)$ thus obtained for various values of noise strength D and I_0 are depicted in Figs. 3 and 4. Of note, we demonstrate that changing the reconfigurable parameter I_0 offers a reliable control that allows us to obtain all six fundamental logic operations for an optimal noise intensity level D. So it is clearly evident that the nonlinear bistable system acts as a noise-assisted threshold detector (logical stochastic resonator) to extract a two-state logical output reliably, and I_0 can efficiently control the nature of the logic output, thereby serving as an excellent logic reconfiguration parameter.

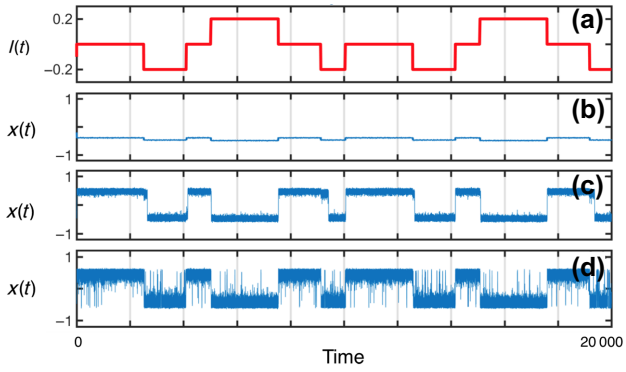

FIG. 3. Time series $I(t) = I_1 + I_2$, and $x(t)$ associated with the XOR logic operation using the nonlinear system [cf. Eq. (2)]. The inputs I_1 and I_2, take value -0.1 when logic input is 0 and value 0.1 when logic input is 1. The asymmetry control parameter c is fixed at 0.5. The output $x(t)$ is used to extract logic operations for the logic reconfiguration parameter $I_0 = 0.8$. (a) The signal $I(t)$. (b)–(d) For low-noise level $D = 0.1$, the input is not able to produce reliable transitions between the two states. As the noise level is increased, an optimal noise level is reached ($D = 0.35$) in which the nonlinear bistable system switches synchronously with the input, obtaining in this way a reliable XOR logic response. Further increase of the noise level $D = 1.2$ leads to the occurrence of random switches, destroying the reliability of the logic gate.

TABLE II. Necessary and sufficient conditions, derived from the logic truth tables, to be satisfied simultaneously by the nonlinear dynamical element, in order for it to have the capacity to implement the logical operations,OR, AND, NOR, NAND, XOR, and XNOR logic operations (cf. Table I) with the same system represented by Eq. (2), for the four distinct possible input sets $(0, 0)$, $(0, 1)$, $(1, 0)$, and $(1, 1)$.

Input set (I_1,I_2)	Logic operation	Output	Necessary and sufficient condition
(0,0)	OR	0	$x(t) < 0$
(0,1)/(1,0)	OR	1	$x(t) > 0$
(1,1)	OR	1	$x(t) > 0$
(0,0)	AND	0	$x(t) < 0$
(0,1)/(1,0)	AND	0	$x(t) < 0$
(1,1)	AND	1	$x(t) > 0$
(0,0)	NOR	1	$x(t) > 0$
(0,1)/(1,0)	NOR	0	$x(t) < 0$
(1,1)	NOR	0	$x(t) < 0$
(0,0)	NAND	0	$x(t) < 0$
(0,1)/(1,0)	NAND	1	$x(t) > 0$
(1,1)	NAND	1	$x(t) > 0$
(0,0)	XOR	0	$x(t) < 0$
(0,1)/(1,0)	XOR	1	$x(t) > 0$
(1,1)	XOR	0	$x(t) < 0$
(0,0)	XNOR	1	$x(t) > 0$
(0,1)/(1,0)	XNOR	0	$x(t) < 0$
(1,1)	XNOR	1	$x(t) > 0$

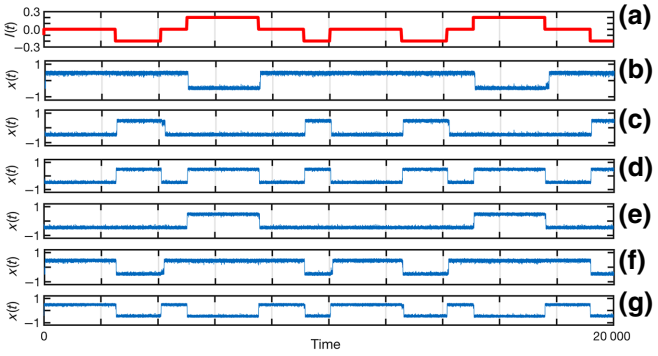

FIG. 4. Time series $I(t) = I_1 + I_2$, and $x(t)$ associated with the reconfigurable logic operations using the nonlinear bistable system [cf. Eq. (2)]. Here noise intensity $D = 0.35$ and the inputs I_1 and I_2, take value -0.1 when logic input is 0 and value 0.1 when logic input is 1. The asymmetry control parameter c is fixed as 0.5. The output $x(t)$ is used to extract logic operations for various logic reconfiguration parameter I_0. (a) The signal $I(t)$ and (b)–(g) depict the NAND, NOR, XNOR, AND, OR, and XOR logic responses for $I_0 = 0.3$, 0.4, 0.5, 0.6, 0.75, and 0.8, respectively.

We can quantify the consistency (or reliability) of obtaining a given logic output by estimating the probability of obtaining the desired logic output for different input sets to Eq. (2) through numerical simulation. This probability, denoted by P(logic), is the ratio of the number of correct logic outputs to the total number of runs, with each run sampling over different permutations of the four input sets $(0,0)$, $(0,1)$, $(1,0)$, and $(1,1)$. If the logic output, as obtained from $x(t)$, matches the logic output of the truth table for *all* four input sets in the run, it is considered a success, and is deemed unsuccessful even if one of the input sets does not yield a correct output. So this is a stringent measure of reliability, and when P(logic) is close to 1, the logic operation is obtained very reliably. Using this quantifier we find that all the logic operations can be obtained robustly in specific ranges of parameters. We show the representative case of P(logic) for the fundamental logic operation NOR, in the parameter space of the noise strength versus logic reconfiguration parameter I_0 in Fig. 5, and in the parameter space of the noise strength and the amplitude of the logic input signal in Fig. 6. Clearly the reliability of logic operations is close to 1 in an optimal band of moderate noise.

Note that both the logic reconfiguration parameter I_0 and the input signal strength have to be optimized to get the best operational range. For certain operations, such as XNOR, the robust operational range in parameter I_0 may be narrow for specific input signal strengths (cf. Fig. 7, where the input signal strength is 0.1). However, for different input signal strengths one can find a good operational range for XNOR as well (see Fig. 8 for an illustrative example).

The interesting observation here is that these robust logic operations are only realized, for subthreshold input signals, in the presence of noise. More specifically, in relatively wide windows of moderate noise, the system

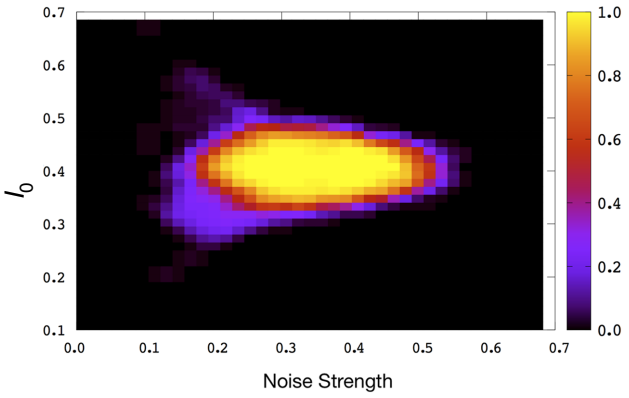

FIG. 5. Density map of P(logic) for NOR logic operation, as a function of the noise strength (x axis) and the logic reconfiguration parameter I_0 (y axis), obtained from numerical simulations. Here the input signal strength is 0.1. All other control parameters are fixed as in Fig. 4.

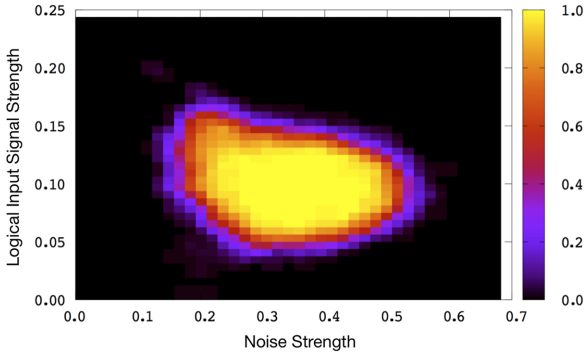

FIG. 6. Density map of P(logic) for NOR logic operation, as a function of the noise strength (x axis) and input signal strength (y axis), obtained from numerical simulations. Here $I_0 = 0.4$. All other control parameters are fixed as in Fig. 4.

yields logic operations with near certain probability, i.e., P(logic) $= 1$, and so is robust to background fluctuations. This effect is also observed for the case of parametric perturbations, usually manifested as multiplicative or state-dependent noise.

III. EXPERIMENTAL REALIZATION

In this section, we verify this concept in electronic circuit analogs of the nonlinear system described by Eq. (2), and ascertain its robustness in experiments [42]. The schematic of the circuit realization is shown in Fig. 9. This type of system can also experimentally be implemented with integrated circuits by combining CMOS transistors

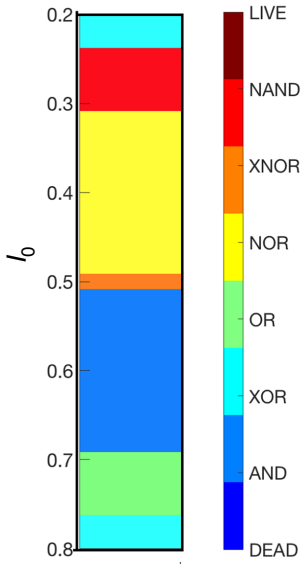

FIG. 7. Schematic showing the different logic patterns obtained under varying I_0, in the range [0.2:0.8], corresponding to the system described by Eqs. (2) and (3), with all other parameters as given in Figs. 3 and 4.

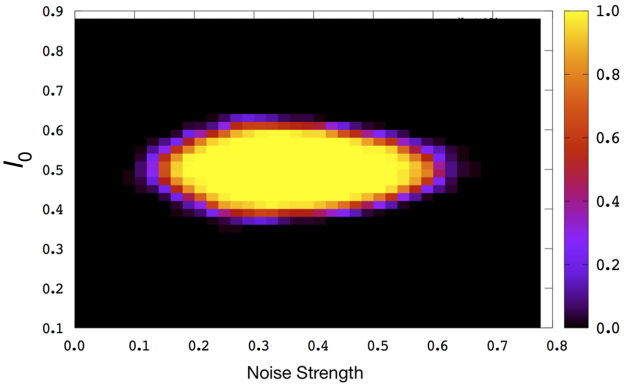

FIG. 8. Density map of P(logic) for XNOR logic operation, as a function of the noise strength (x axis) and the logic reconfiguration parameter I_0 (y axis) obtained from numerical simulations. Here the input signal strength is 0.17. All other control parameters are fixed as in Fig. 4.

and a set of linear resistors and capacitors [25]. In Fig. 9, $I(t)$ corresponds to logic input signal $(I_1 + I_2 + I_0)$, where the logic input signals I_1 and I_2 take value -100 mV when logic input is 0 and value 100 mV when logic input is 1. The bias voltage c is set equal to -500 mV and noise intensity value $D = 1$ V. The reconfiguration control parameter I_0 is varied from 200 to 800 mV. The output node voltage $x(t)$ of operational amplifier OA2 corresponds to state

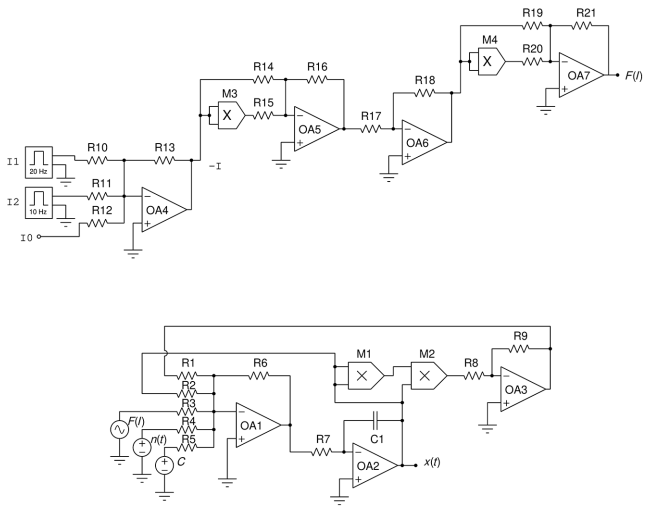

FIG. 9. Analog circuit diagram of Eqs. (2) and (3). Here OA1–OA7 are operational amplifiers (μA 741 or AD712). M1–M4 are analog multipliers (AD633). The resistor values are fixed as R = R3 = R4 = R5 = R6 = R9 = R10 = R11 = R12 = R13 = R16 = R17 = R18 = R21 = 100 KΩ. R1 = R14 = R19 = 25 KΩ, R2 = 5 KΩ, R7 = 10 KΩ, R8 = 1 KΩ, R15 = R20 = 2.5 KΩ. The capacitor value is fixed as $C_1 = 0.01$ μ-Farad. The nonlinear transformation function $F(I)$ generated by the top circuit is used to drive the bottom circuit. The response state variable $x(t)$ is obtained from the op-amp integrator circuit (OA2).

variable $x(t)$ of Eq. (2). The component values of this circuit are indicated in the schematic (Fig. 9). A combination of op-amp adder, scale changer, and multiplier circuits are used to produce the nonlinear transformation signal $F(I)$ from the op-amp OA7. Further, the output $F(I)$ is coupled to the bottom circuit, again consisting of op-amp summing amplifier, scale changer, integrator,

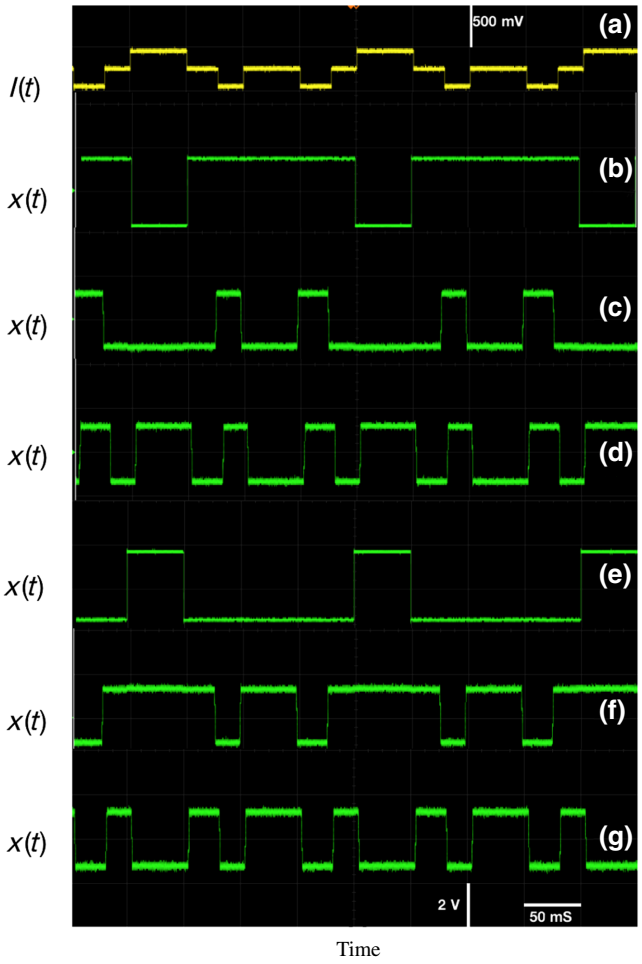

FIG. 10. Experimental observation of different logic operations through the analog simulation circuit of Fig. 9. (a) Input signal $I(t) = I_1 + I_2$. Here, I_1 and I_2 are two logic input signals, which take value -100 mV when logic input is 0 and value $+100$ mV when logic input is 1; (b)–(g) the waveforms of the output voltage $x(t)$, for noise amplitude $D = 1$ V and bias value $c = -500$ mV. (b)–(g) NAND, NOR, XNOR, AND, OR, and XOR logic responses for $I_0 = 0.3$, 0.4, 0.5, 0.6, 0.75, and 0.8 V, respectively. Both for low- and high-noise levels, no desired logic output is observed. The noise signal is drawn from Agilent or Keysight 33522A, Function/Arbitrary Waveform Generator. The oscilloscope used is Agilent or Keysight DSOX2012A. The power supply to op-amps and the bias voltage I_0 and c are drawn from Agilent or Keysight E3631A DC Power Supply. The scale of the traces are 50 ms/Div (X axis). For (a), the scale in the trace is 500 mV/Div (Y axis), for (b)–(g), the scale in the traces are 2 V/Div.

and multipliers to produce the dynamical state variable $x(t)$. In the circuit, op-amps are realized with AD712 or μA741. The multipliers are realized with AD633. The noise signal is drawn from Agilent or Keysight 33522A, Function/Arbitrary Waveform Generator. All oscilloscope trails are obtained using Agilent or Keysight DSOX2012A. The power supply to op-amps and the bias voltage I_0 and c are drawn from Agilent or Keysight E3631A DC Power Supply. The representative oscilloscope traces for various values of I_0 from the circuit realization of Fig. 9 are displayed in Fig. 10. A comparison with Fig. 4 clearly shows that the same phenomenon is observed in these experiments. That is, only with noise intensity D with moderate value, equal to 1 V, do we get the desired logic gate operation reliably.

Although we demonstrate our idea with the specific bistable system given in Eq. (2), we can also obtain all these reconfigurable logic operations in a similar fashion, in the presence of a noise floor, using any bistable system, including a simple Schmitt trigger as the basic bistable unit.

IV. CONCLUSIONS

In summary, we demonstrate a scheme for the direct and flexible implementation of all basic logic gates utilizing nonlinear dynamics and the interplay of noise. The richness of nonlinearity allows us to select out all the different binary logic gate responses from the same nonlinear (bistable) dynamical system by simply setting suitable bias values and an optimal band of noise. The reconfigurable bias values are known exactly from theory and are thus available as a look-up table. This scheme is implemented both through numerical simulations and electronic experiments. Thus our results suggest the potential of exploiting nonlinear transformations of inputs to implement flexible logic gates in the presence of a noise floor. The ideas presented here, combining the research directions of chaos computing [43–51] and logical stochastic resonance [5,6], has potential to be realized in wide-ranging systems, and denotes a direction in exploiting noise-assisted nonlinear dynamical systems to design computational devices.

An open direction of research would be to investigate possible implementations of this idea on many-valued logic, such as three-valued ternary logic, potentially using multistable systems, rather than bistable ones. Further the use of machine-learning techniques to optimize the system parameters in order to find the best operational range of different gates, given a typical noise floor, will be the next step to design the most optimal and robust set of reconfigurable gates.

In conclusion, the ideas presented and explicitly demonstrated through numerical simulations and proof-of-principle circuit experiments here, can provide impetus for further developments to optimize the basic idea, as well as to implement it in a range of systems. So this work offers ideas for an alternate computing platform, that may potentially yield rich dividends in the future.

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