Ion Migration in Monolayer MoS_2 Memristors

Sotirios Papadopoulos,[1] Tarun Agarwal,[2] Achint Jain,[1,†] Takashi Taniguchi,[3] Kenji Watanabe,[3]
Mathieu Luisier,[4] Alexandros Emboras,[4] and Lukas Novotny[1,*]

[1] *Photonics Laboratory, ETH Zurich, 8093 Zurich, Switzerland*
[2] *Dept. of Electrical Engineering, IIT Gandhinagar, Palaj, Gujarat 382355, India*
[3] *National Institute for Material Science, 1-1 Namiki, Tsukuba 305-0044, Japan*
[4] *Integrated Systems Laboratory, ETH Zurich, 8092 Zurich, Switzerland*

(Received 20 April 2022; accepted 10 June 2022; published 8 July 2022)

Memristors hold great promise as building blocks for future computing architectures where memory and logic are combined at the hardware level. However, scaling down the dimensions of memristive devices has been limited by high leakage currents, thus inhibiting further progress. Recent studies have demonstrated memristors with monolayers of MoS_2 and large high-to-low resistance ratios. Defects combined with metallic ion migrations are often seen as a possible explanation for this behavior. A detailed understanding of the switching mechanisms, in particular the role of metal ion diffusion into vacancy sites and crystal defects, remains elusive. Here we investigate how defect densities affect the performance of monolayer MoS_2 memristors. We experimentally demonstrate that the resistive switching ratio becomes larger if the defect density in MoS_2 is increased. Furthermore, by means of *ab initio* quantum transport simulations, we reveal the existence of an optimum range of defect densities and explore the theoretical limits of monolayer MoS_2 memristors. Our results highlight the importance of defect engineering and control in transition metal dichalcogenides memristors.

DOI: 10.1103/PhysRevApplied.18.014018

I. INTRODUCTION

In a period where Moore's scaling law is under siege [1] and the demand for high-density memories is constantly increasing [2], fundamentally new electrically switchable structures are needed to further push technological limits. Memristive devices (or memristors) have shown great potential as alternative building blocks for nonvolatile memories and computing applications beyond the von Neumann architecture [3]. Moreover, memristors with multiple resistive switching states enable the realization of neuromorphic computing at a hardware level, making it important to investigate such structures in depth [4]. The initial conception of a memristor by Chua in 1971 [5] and its experimental demonstration in 2008 [6] were followed by substantial research efforts to determine the physical mechanisms involved in memristive switching and optimize their characteristics. Since then, several memristive mechanisms have been observed, such as electrochemical metallization [7], valence-change, [8] and phase-change effects [9]. Current state-of-the-art memristor cross-bar arrays feature approximately 10 nm-sized active regions, at par with today's silicon complementary metal oxide semiconductor integrated circuitry [10]. A further downscaling of memristors brings more challenges than benefits, especially in terms of stability, reproducibility, and robustness.

The rise of various two-dimensional (2D) materials such as graphene and transition metal dichalcogenides (TMDs) inspired alternative platforms for memristive devices [11–18]. Recent reports have shown very low leakage currents in monolayer (1L) MoS_2-based memristors compared to traditionally used oxides, allowing for thickness scaling down to less than 1 nm [17,19,20]. However, the mechanisms behind the memristive effects observed in 2D materials are not yet understood, especially in devices employing monolayers, for which reports present highly contradictory results [17,21]. Moreover, a recent scanning tunneling microscopy study has shown that point defects such as sulfur vacancies can give rise to memristive behavior through Au ion diffusion in monolayer TMDs [22].

*lnovotny@ethz.ch
†Present address: Centre for Quantum Computation and Communication Technology, School of Physics, University of New South Wales, Sydney, NSW 2052, Australia

Published by the American Physical Society under the terms of the Creative Commons Attribution 4.0 International license. Further distribution of this work must maintain attribution to the author(s) and the published article's title, journal citation, and DOI.

In multilayer structures independent studies have revealed contrasting findings, attributing the switching mechanism to either phase-transition or defect-mediated atomic migration [12,23]. A detailed investigation of the influence of varying defect densities and fabrication process parameters on the memristive characteristics in 2D TMDs is still lacking.

Here we investigate the influence of defect densities in monolayer MoS_2 on the resistive switching ratio. Our experimental findings reveal that memristors comprised of defective MoS_2 switch at lower voltages and exhibit a stronger change in resistance than memristors made of pristine MoS_2. We support our observations with *ab initio* quantum transport simulations and develop a model that suggests the existence of an optimum range of defect densities at which the resistive switching difference is maximum. This work highlights the importance of defect engineering in memristors built from 2D materials and provides guidelines for enhancing performance.

II. DEVICE PREPARATION

Our memristors were built by sandwiching 1L-MoS_2 between a 1L-graphene top electrode and a 50 nm gold (Au) bottom electrode, in a vertical charge transport configuration [cf. Fig. 1(d)]. For protection, we cover the top graphene electrode by a thin layer of hexagonal boron nitride (*h*-BN). MoS_2 crystals synthesized by chemical vapor transport with 99.9999% purity were purchased from 2D Semiconductors®. MoS_2, graphene, and *h*-BN flakes were mechanically exfoliated from bulk crystals on Si/SiO_2 substrates. A poly-dimethylsiloxane (PDMS) stamp covered by a thin polycarbonate film [24] was used to sequentially pick up top *h*-BN, graphene, and MoS_2 flakes in air. The resulting stack was then transferred on top of Au electrodes prepatterned by photolithography on a glass substrate (see Sec. S1 in the Supplemental Material for more details [25]). It is known that evaporation of contact metals, including Au, can introduce a significant amount of defects in MoS_2 and lead to metal-MoS_2 chemical bonding [26]. The use of graphene as a top electrode in our devices allows for evaporation-free fabrication, thereby preventing any inadvertent defect generation in MoS_2 due to metal evaporation and decoupling the influence of contact metallization on the memristive behavior, something that has been largely overlooked so far. The dry pickup and assembly avoids polymer and solvent contamination at any stage, resulting in pristine interfaces.

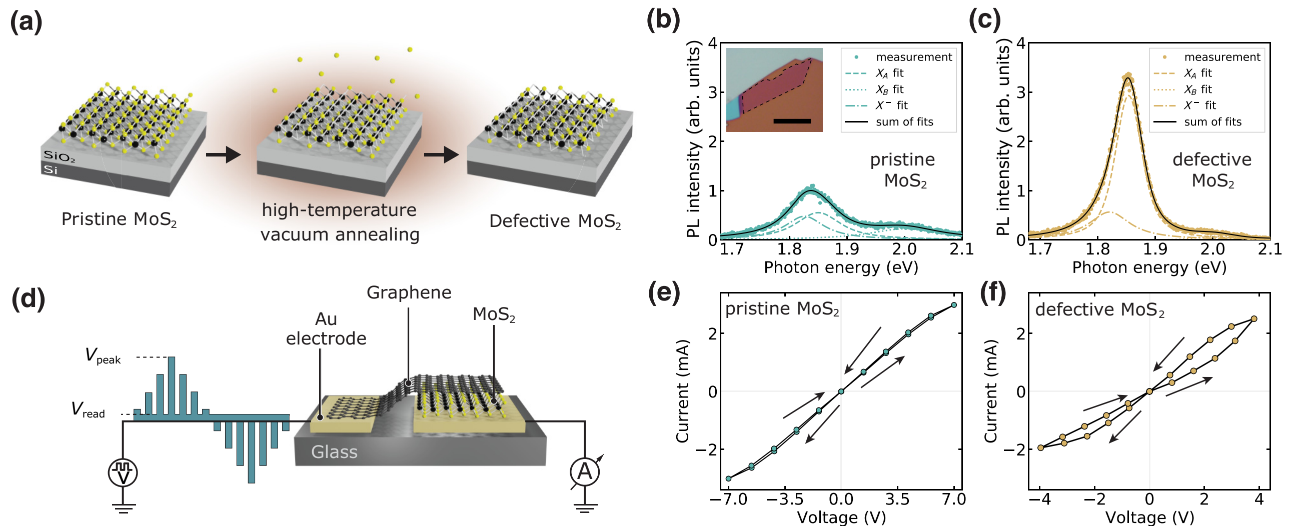

FIG. 1. (a) Illustration of the MoS_2 treatment process. MoS_2 exfoliated on a Si/SiO_2 substrate is annealed in high vacuum (HV) at 400°C for 1 h during which some sulfur atoms escape the MoS_2 crystal lattice due to the high temperature, resulting in a defective MoS_2 flake. (b),(c) Photoluminescence spectra of (b) an as-exfoliated (pristine) MoS_2 flake on Si/SiO_2 substrate and (c) after HV annealing at 400°C (defective). X_A, X_B and X^- refer to the A-exciton, B-exciton and trion spectral contributions respectively, fitted with Voigt distribution functions. Both spectra were measured from the same MoS_2 region with 532 nm laser excitation at 24 μW power under ambient conditions and were normalized to the peak intensity of the spectrum in (b) for ease of comparison. The inset in (b) shows an optical microscope image of the MoS_2 flake before annealing (monolayer outlined by black dashed line). The scale bar is 12.5 μm. (d) Schematic illustration of a memristor built by sandwiching 1L-MoS_2 between graphene and Au electrodes. The top *h*-BN flake used for encapsulation has been omitted from the illustration for clarity. Electrical measurements were performed using pulsed voltage sweeps to eliminate hysteresis. After each write pulse, the device resistance was probed with a much lower read voltage (V_{read} = 100 mV). Pulse duration and period are 10 ms and 30 ms, respectively. (e),(f) Pulsed *I*-*V* measurements of memristors with pristine and defective 1L-MoS_2 flakes showing an enhanced switching behavior after high-temperature annealing. The black arrows indicate the voltage sweep directions in both plots. All measurements were carried out in air at room temperature.

Moreover, the asymmetric electrode configuration allows for material-oriented analysis of the results connecting the memristive effect to Au ion diffusion, as discussed later in this paper. Furthermore, the top *h*-BN encapsulation avoids material degradation during measurements under ambient conditions. Thus, the above fabrication methodology preserves the purity and high crystal quality of our MoS_2 flakes at every step, allowing us to study MoS_2 in its pristine state, in contrast to previous studies [17]. In order to compare the memristive performance between pristine MoS_2 and those with increased defect densities, we also built devices by intentionally introducing defects in MoS_2 flakes after exfoliation.

Two different treatments were used to generate defects in our devices: high-temperature annealing in high vacuum at 400°C; and argon (Ar) sputtering in a plasma chamber at room temperature. Both of these methods have previously been shown to introduce defect sites in the MoS_2 crystal lattice [22,27,28]. The annealing process is illustrated in Fig. 1(a). We confirmed the generation of defects through photoluminescence (PL) spectroscopy. Figures 1(b) and 1(c) show the PL spectra of a monolayer MoS_2 flake before (pristine) and after high vacuum (HV) annealing (defective) treatment. A strong enhancement of the A-exciton (X_A) PL contribution is observed after annealing. This enhancement originates from the introduction of sulfur vacancies (V_s) in MoS_2 upon annealing that act as sites for physisorption of N_2 and O_2 molecules present in air [29]. These molecules lead to an effective p-doping of MoS_2, thereby decreasing the free-electron density, and resulting in a stronger X_A PL emission [30]. It must be noted that this strong PL enhancement cannot be explained by the release of built-in strain and elimination of polymer residues (if any) upon annealing, as these effects were previously shown by us to not result in any appreciable PL increase in MoS_2 [31]. However, in order to further test the creation of defects during HV annealing, we performed studies on the localized increase of PL efficiency as a function of illumination time, an effect that has been attributed to sulfur vacancies in ambient conditions [32]. Measurement results and discussion on that matter can be found in Sec. S2 of the Supplemental Material [25]. In case of Ar-sputtered MoS_2 flakes, a reduction in the PL emission was observed, in strong contrast to annealed flakes, which can be attributed to the formation of more extended defects including MoS_6, Mo, and S vacancies [33], resulting in a decrease of the PL quantum yield (see Sec. S2 of the Supplemental Material [25]). Lastly, in order to study the impact of defects introduced during evaporation of metal electrodes on the memristive behavior of MoS_2 devices, we also fabricated devices with graphene as the bottom electrode and evaporated Au as the top electrode, following an inverse stacking sequence. It has been shown that during Au evaporation, Mo and S atoms can be substituted by Au atoms, leading to defects in the MoS_2 layer [26] that can favor the formation of conductive channels and thereby enhance the memristive effect.

III. ELECTRICAL CHARACTERIZATION

The memristive performance of the devices prepared with different defect densities and fabrication procedures was electrically characterized by applying a voltage pulse sequence and measuring the current with a low-noise source meter. A periodic triangular bipolar pulsed sweep was performed with an offset voltage V_{read} to allow for low-voltage estimation of the resistance after every applied pulse [see Fig. 1(d)]. Pulsed electrical measurements have a dual benefit. Firstly, continuous electrostatic stress for long periods of time is avoided, which was found to increase the lifetime of our devices and allowed us to study their behavior at voltages as high as 7.5 V without any apparent degradation. Secondly, this procedure prevents any inadvertent parasitic hysteresis due to charge accumulation from influencing our measurements [34]. This ensures that the hysteresis we observe arises solely from a nonvolatile resistance change, indicative of memristive behavior. Pulsed I-V measurements of devices with pristine and vacuum annealed MoS_2 are plotted for comparison in Figs. 1(e) and 1(f), respectively. Every point in the plot corresponds to the average value of the current flow during an applied voltage pulse versus the magnitude of that pulse. In the pristine device, we only observe a weak hysteresis even after applying significantly high voltages ($V_{\text{peak}} = \pm 7$ V). In the case of vacuum annealed MoS_2, the hysteresis gets enhanced and appears at lower applied voltages compared to the pristine MoS_2 device. We attribute this effect to the increased defect density of the MoS_2 flake caused by high-temperature annealing. This is an indication that an increase in defect density can provide the means for a stronger memristive performance.

We also find that the devices switch from a high-resistance state to a low-resistance state only with a positive voltage applied at the Au electrode and with the graphene electrode grounded. This polarity-dependent switching behavior is an indicator of material-specific properties. More specifically, we attribute this observation to the migration of Au ions from the Au electrode to defect sites in the MoS_2 flake. It is well known that Au atoms can ionize and migrate under the influence of an applied electric field. Defect sites offer an energetically favorable state for Au ions to bond with the MoS_2 crystal. This process can be reversed by flipping the direction of the applied electric field. Since bound Au atoms at the MoS_2 flake lower the resistance of the Au-MoS_2 interface, this can lead to resistive switching effects when excited with a bipolar voltage sweep [22]. We also observed an increased hysteresis in devices with Ar-sputtered MoS_2 as well as in those with

evaporated Au as a top electrode, which further corroborates our hypothesis. A comparison of I-V measurements from differently treated devices can be found in Sec. S3 of the Supplemental Material [25].

The observation of hysteresis in the I-V characteristics of our devices is a strong indicator of the occurrence of resistive switching. To gain further insight we also characterized the resistance at low voltages during the pulsed sweep. After every applied pulse, the device resistance is measured at $V_{\mathrm{read}} = 100$ mV, as indicated in Fig. 2(a), which shows a time-trace of the applied sweep. Figure 2(b) presents the change in resistance $\Delta R = R_0 - R_{\mathrm{read}}$ during the pulsed voltage sweep, where R_0 is the resistance measured before starting the sweep and R_{read} is the resistance measured after each pulse. Results from different devices are shown for comparison. “Pristine MoS_2” no. 1 and no. 2 refer to two devices fabricated without any treatment of the MoS_2 flake. “Au evaporated” no. 1 and no. 2 refer to two devices featuring an evaporated Au top electrode and a graphene bottom electrode and using otherwise untreated MoS_2. “Ar sputtered” and “vacuum annealed” refer to devices with MoS_2 flakes treated with the corresponding methods. In all devices the same voltage sweep range was used with $V_{\mathrm{peak}} = \pm 4$ V. We define the on region as the region after the application of the highest voltage pulse and before the application of the lowest. The region before and after the on region is referred to as the off region. A clear difference in the magnitude of ΔR between pristine and defective devices can be seen, with the latter exhibiting a stronger change in ΔR.

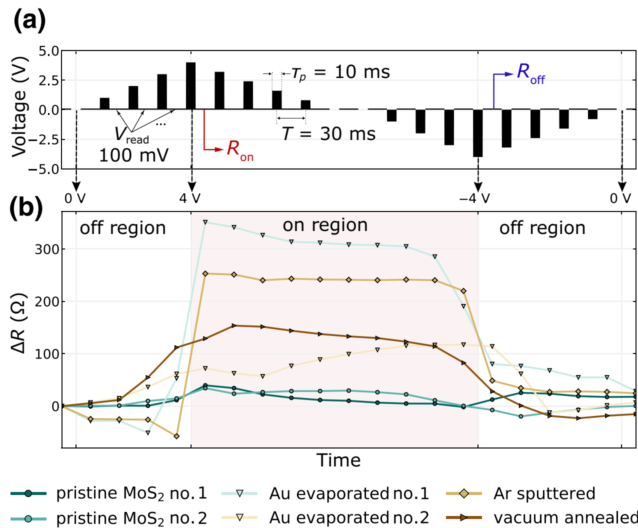

FIG. 2. (a) Time-trace of the applied voltage sweep. Black solid arrows indicate the low-voltage regions where the resistance is measured. Black dashed arrows indicate the voltage level positions for 0, 4, and −4 V. Pulse duration $\tau_p = 10$ ms and pulse period $T = 30$ ms. Red and blue arrows indicate the time instances where the R_{on} and R_{off} values are measured, respectively. (b) Time-trace of the low-voltage resistance difference ΔR for different devices measured during the pulsed voltage sweep presented in (a). The resistance is measured with $V_{\mathrm{read}} = 100$ mV after every applied pulse. An increase in ΔR in the on region can be observed for all devices. Defective devices show a much stronger increase in ΔR compared to pristine ones.

We use ΔR to compare different devices since it cancels out any other series resistances such as contact and graphene sheet resistance. However, resistance also scales with the vertical junction area in every device, which is difficult to estimate accurately from optical microscope images due to edge effects at the graphene/MoS_2/Au junction interface. Therefore, the switching ratio, which is an experimental quantity that is immune to the variations in junction areas among different devices, was also investigated. The switching ratio is given by $R_{\mathrm{off}}/R_{\mathrm{on}}$, where R_{off} and R_{on} are the resistances of the device after the application of the largest and the smallest voltage pulses, as indicated in Fig. 2(a) with blue and red arrows, respectively. The total resistance measured also includes the series graphene sheet resistance which can vary between devices. To estimate its contribution to the overall resistance and subtract it from R_{off} and R_{on} values we estimated the graphene sheet resistance per unit length by fabricating a multielectrode device where Au electrodes with different spacings were connected by one graphene flake and performing transmission line measurements. The estimated graphene resistance was then subtracted from the total device resistance according to the graphene electrode length used in each device.

Taking the aforementioned under consideration, in Fig. 3(a) we plot the switching ratios $R_{\mathrm{off}}/R_{\mathrm{on}}$ for sweeps performed with different V_{peak} values for all devices. Here the values of V_{peak} have been adjusted to account for the voltage drop across the graphene sheet. We observe that in the case of pristine devices, the ratio reaches a modest value of 1.1 only at high V_{peak} voltages around 6.5 V. On the other hand, for devices with higher MoS_2 defect

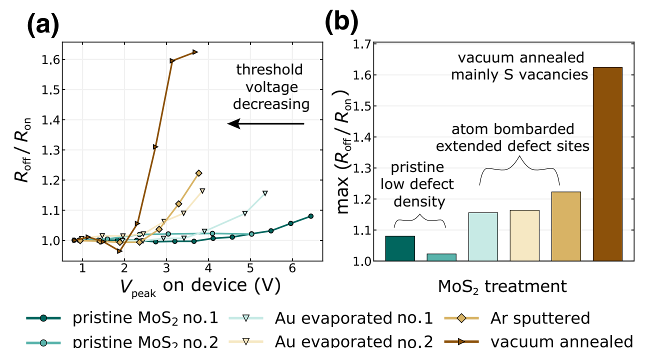

FIG. 3. (a) Switching ratio $R_{\mathrm{off}}/R_{\mathrm{on}}$ as a function of V_{peak} for all reported devices. (b) A comparison of the maximum switching ratios achieved for the different MoS_2 treatments associated with different defect types and densities. Colors in the plot correspond to the legend shown at the bottom.

density, the ratio reaches values as high as 1.6 at much lower V_{peak} values. This clearly indicates that memristive switching depends on the defect density. In Fig. 3(b), we plot the maximum ratio achieved experimentally for the different MoS_2 treatment procedures. Interestingly, we find that vacuum annealing leads to the highest switching ratio at low V_{peak} voltages. Our PL measurements reveal that in this case mainly S vacancies are created in the crystal whereas in the cases of Ar sputtering and evaporation of Au as a top electrode, more extended defect sites are expected to be created. The existence of extended defect sites lowers R_{off} and hence when Au atoms diffuse into the vacancy sites, a smaller change in R_{on} is observed leading to a lower switching ratio.

Our measurements indicate that the switching ratio can be enhanced by increasing the defect density of MoS_2. However, we did not observe switching ratios higher than 1.7. This observation is in contrast to recent reports of vertical graphene/MoS_2/Au structures where switching ratios up to 10^4 were observed [17]. One of the probable reasons for this contradiction is the fabrication process reported in [17], which includes invasive steps, such as direct contact with polymers and solvents such as PDMS and de-ionized water. Direct contact with these materials compromises the interface quality and can introduce contaminants and could explain the unusually high R_{off} observed for subnanometer tunnel barriers. We note, however, that some studies report tunneling resistances closer to those observed in our study [21]. An increased memristive effect was also reported for transfer-free and litho-free fabrication with evaporated top electrodes [17]. In an effort to reproduce these results, we fabricated and tested devices with evaporated Au top electrodes without any success. The only distinguishable difference between our work and [17] is the use of chemical vapor deposition (CVD) grown 1L-MoS_2 vacuum annealed at 600 K, instead of high-quality pristine flakes as in our work. The main differences between CVD-grown and exfoliated MoS_2 is that the former typically hosts a higher defect and grain boundary density, lower interface quality and more process contaminants like oxides and multilayer domains.

IV. QUANTUM TRANSPORT MODELING

In order to further our understanding of the memristive behavior of MoS_2 we performed *ab initio* quantum transport simulations [35]. Illustrations of the studied configurations are presented in Figs. 4(a)–4(c). The three models account for different MoS_2 crystal configurations, namely (a) pristine, (b) including a single sulfur vacancy (V_s), and (c) including a migrated Au atom at the V_s site. We denote the resistances for the three configurations by R_{pr}, R_{V_s}, and R_{Au}. The resistances are evaluated at 100 mV bias voltage and the cell area of the simulation is $A = 2.14 \times 3.79\ nm^2$.

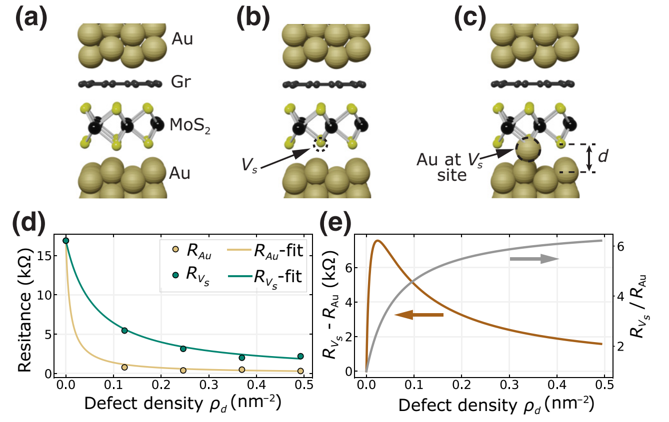

FIG. 4. (a)–(c) Illustration of the atomic models simulated with (a) pristine MoS_2, (b) one sulfur vacancy V_s and (c) with one Au atom at the V_s site. (d) Simulation results and model fit for the resistances evaluated in the device models presented in (a)–(c) for different defect densities. R_{Au} is the resistance evaluated for the model in (c), R_{V_s} is the resistance evaluated for the model in (b), and the resistance for defect density $\rho_d = 0$ (pristine) is the resistance for the model in (a). The fit function is given by Eq. (1). (e) Calculated values of resistance difference $R_{V_s} - R_{Au}$ and switching ratio R_{V_s}/R_{Au} using the fitted values in (d).

The resistances are calculated for an interlayer distance of $d = 4.7$ Å [Fig. 4(c)]. This interlayer distance has been chosen as the one where $R_{V_s} - R_{Au}$ is maximum since the resistance difference diminishes at smaller and larger interlayer distances due to metal- induced gap states, and high tunneling resistances, respectively (see Sec. S4 in the Supplemental Material for more details [25]).

By increasing the number of defects in the cell area of the simulation we can evaluate the resistances as a function of defect density (colored dots in Fig. 4(d)). Due to limits on the cell area size posed by computation time, the region of low defect densities cannot be easily explored, thus we employ a classical model to predict the resistance as a function of defect density ρ_d. The estimated overall resistance can be written as

$$R(\rho_d) = \frac{R_{pr} \times R_d}{R_d + (R_{pr} - R_d)\,\rho_d \times A} \quad (1)$$

where R_d refers to either R_{V_s} or R_{Au}, depending on the configuration. Details on the formation of the model can be found in Sec. S5 of the Supplemental Material [25]. We use the simulation results to fit the function in Eq. (1). The result is shown in Fig. 4(d). Both R_{V_s} and R_{Au} drop with increasing ρ_d due to defect states that appear inside the MoS_2 bandgap (see Fig. S6d in the Supplemental Material). R_{Au} takes on lower values than R_{V_s}, which highlights the importance of Au migration in resistive switching. The difference in resistance $R_{V_s} - R_{Au}$, as well

as the switching ratio R_{V_s}/R_{Au}, are plotted as a function of ρ_d in Fig. 4(e). Interestingly $R_{V_s} - R_{\mathrm{Au}}$ is not monotonic but features a maximum in the low ρ_d region. On the other hand, the switching ratio R_{V_s}/R_{Au} increases constantly with ρ_d, with a tendency to saturate. Although the ratio increases for high ρ_d, the resistances R_{V_s} and R_{Au} drop significantly, making the performance dependent on any other possible series resistances present in the system. However, in the region where $R_{V_s} - R_{\mathrm{Au}}$ is maximum, the ratio R_{V_s}/R_{Au} is already at half of its maximum value, making this region preferable for memristive operation. These results reveal the need for defect engineering of such memristive devices for optimized performance. Furthermore, for $\rho_d \to \infty$, $R_{V_s}/R_{\mathrm{Au}} = 6.8$. Although the case of infinite ρ_d seems nonphysical, it can be translated to the situation of an Au scanning tunneling microscope tip over a V_s site exchanging an Au atom. Recent studies have experimentally demonstrated this, reporting a very similar switching ratio for the same interlayer distance range [22]. This increases the validity of our simulations. Furthermore, our experimental observations confirm the theoretical prediction that increasing the defect density of the material increases the ΔR and the $R_{\mathrm{off}}/R_{\mathrm{on}}$ ratio.

V. DISCUSSION

The objective of our study is to explore the limitations of monolayer 2D memristors from a theoretical and experimental perspective. Even in the optimal case of the simulation model the high tunneling current in the off state due to the presence of defects does not allow switching ratios higher than 7.

The simulated and experimentally observed resistance ratios are of the same order of magnitude. The small discrepancy observed may be due to limited knowledge of the actual defect densities in the fabricated devices or due to sample imperfections, such as bubbles and/or unaccounted contact resistances. Additionally, in our simulations we assume that all the V_s are filled immediately and abruptly, whereas in reality the occupation of the V_s by Au ions happens gradually.

Another important result is that R_{V_s} (the R_{off} value) drops significantly with increasing ρ_d due to defect states in the bandgap while the switching ratio saturates at the same time. We note that some previous studies reported surprisingly strong memristive effects [17]. We have not been able to experimentally reproduce these observations. Our theoretical treatment provides further evidence that such strong memristive effects in monolayer MoS_2 cannot be achieved solely due to defects. Our experimental observations support this claim and emphasize the need for further studies to clarify the exact mechanisms responsible for the strong memristive effects reported in recent studies.

VI. CONCLUSION

To conclude, we fabricated different monolayer MoS_2 memristive devices by employing noninvasive fabrication methods with pristine, Ar-sputtered and vacuum-annealed MoS_2, as well as devices with evaporated Au as a top electrode. We compared their memristive performance and showed that with increased defect density, both ΔR and the $R_{\mathrm{off}}/R_{\mathrm{on}}$ ratio get enhanced. We attribute this effect to Au ion migration into MoS_2 defect sites. Our experimental observations are in good agreement with numerical and theoretical models. Moreover, we explored the relation between defect density and memristive performance and revealed the existence of an optimum range of defect densities for designing efficient memristors. Additionally, we compared our results with previous studies and concluded that Au ion migration cannot be the sole reason for the reported results in [17]. Still, our analysis establishes a clear understanding of the role of defects in resistive switching in MoS_2 monolayers and provides guidelines for controlling their memristive performance. Finally, our work provides theoretical insights into the relation between defect density and memristive performance for memristors based on ion migration.

ACKNOWLEDGMENTS

This study was supported by funding from ETH Zurich under ETH Grant No. ETH-15 19-1 SYNEMA, the ETH Zurich Foundation project number 2013-08 (11) with a donation from the Stavros Niarchos Foundation, and by a grant from the Swiss National Supercomputing Centre (CSCS) under Project s971. Use of the cleanroom facilities at the FIRST Center for Micro and Nanoscience, ETH Zurich is gratefully acknowledged. T.T. and K.W. acknowledge support from the Elemental Strategy Initiative conducted by the MEXT, Japan and JSPS KAKENHI (Grant No. JP15K21722). The authors thank Ronja Khelifa and Anna Kuzmina for fruitful discussions and Paul Lehmann for providing experimental support.

[1] M. M. Waldrop, The chips are down for Moore's law, Nature **530**, 144 (2016).

[2] Editorial, Testing memory downsizing limits, Nature Nanotechnology **14**, 1 (2019).

[3] T. Hasegawa, K. Terabe, T. Tsuruoka, and M. Aono, Atomic switch: Atom/ion movement controlled devices for beyond von-Neumann computers, Adv. Mater. **24**, 252 (2012).

[4] D. S. Jeong and C. S. Hwang, Nonvolatile memory materials for neuromorphic intelligent machines, Adv. Mater. **30**, 1704729 (2018).

[5] L. Chua, Memristor—The missing circuit element, IEEE Trans. Circuit Theory **18**, 507 (1971).

[6] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, The missing memristor found, Nature **453**, 80 (2008).
[7] R. Waser, R. Dittmann, C. Staikov, and K. Szot, Redox-based resistive switching memories nanoionic mechanisms, prospects, and challenges, Adv. Mater. **21**, 2632 (2009).
[8] H. S. Wong, H. Y. Lee, S. Yu, Y. S. Chen, Y. Wu, P. S. Chen, B. Lee, F. T. Chen, and M. J. Tsai, Metal-oxide RRAM, Proc. IEEE **100**, 1951 (2012).
[9] H.-S. Wong, S. Raoux, S. Kim, J. Liang, J. Reifenberg, B. Rajendran, M. Asheghi, and K. Goodson, Phase change memory, Proc. IEEE **98**, 2201 (2010).
[10] S. Pi, C. Li, H. Jiang, W. Xia, H. Xin, J. J. Yang, and Q. Xia, Memristor crossbar arrays with 6-nm half-pitch and 2-nm critical dimension, Nat. Nanotechnol. **14**, 35 (2019).
[11] Q. Zhao, Z. Xie, Y. P. Peng, K. Wang, H. Wang, X. Li, H. Wang, J. Chen, H. Zhang, and X. Yan, Current status and prospects of memristors based on novel 2D materials, Mater. Horiz. **7**, 1495 (2020).
[12] F. Zhang, H. Zhang, S. Krylyuk, C. A. Milligan, Y. Zhu, D. Y. Zemlyanov, L. A. Bendersky, B. P. Burton, A. V. Davydov, and J. Appenzeller, Electric-field induced structural transition in vertical $MoTe_2$ and $Mo_{1-x}W_xTe_2$-based resistive memories, Nat. Mater. **18**, 55 (2019).
[13] P. Cheng, K. Sun, and Y. H. Hu, Memristive behavior and ideal memristor of 1T phase MoS_2 nanosheets, Nano Lett. **16**, 572 (2016).
[14] Y. Wang, J. Xiao, H. Zhu, Y. Li, Y. Alsaid, K. Y. Fong, Y. Zhou, S. Wang, W. Shi, Y. Wang, A. Zettl, E. J. Reed, and X. Zhang, Structural phase transition in monolayer $MoTe_2$ driven by electrostatic doping, Nature **550**, 487 (2017).
[15] X. Wu, R. Ge, P. A. Chen, H. Chou, Z. Zhang, Y. Zhang, S. Banerjee, M. H. Chiang, J. C. Lee, and D. Akinwande, Thinnest nonvolatile memory based on monolayer h-BN, Adv. Mater. **31**, 1806790 (2019).
[16] H. K. He, R. Yang, W. Zhou, H. M. Huang, J. Xiong, L. Gan, T. Y. Zhai, and X. Guo, Photonic potentiation and electric habituation in ultrathin memristive synapses based on monolayer MoS_2, Small **14**, 1 (2018).
[17] R. Ge, X. Wu, M. Kim, J. Shi, S. Sonde, L. Tao, Y. Zhang, J. C. Lee, and D. Akinwande, Atomristor: Non-volatile resistance switching in atomic sheets of transition metal dichalcogenides, Nano Lett. **18**, 434 (2018).
[18] A. Krishnaprasad, N. Choudhary, S. Das, D. Dev, H. Kalita, H.-S. Chung, O. Aina, Y. Jung, and T. Roy, Electronic synapses with near-linear weight update using MoS_2/graphene memristors, Appl. Phys. Lett. **115**, 103104 (2019).
[19] D. Akinwande, Memory, memristors, and atomristors, IEEE Micro **38**, 50 (2018).
[20] S. Bhattacharjee, E. Caruso, N. McEvoy, C. Ó Coileáin, K. O'Neill, L. Ansari, G. S. Duesberg, R. Nagle, K. Cherkaoui, F. Gity, and P. K. Hurley, Insights into multilevel resistive switching in monolayer MoS_2, ACS Appl. Mater. Interfaces **12**, 6022 (2020).
[21] R. Xu, H. Jang, M. H. Lee, D. Amanov, Y. Cho, H. Kim, S. Park, H. J. Shin, and D. Ham, Vertical MoS_2 double-layer memristor with electrochemical metallization as an atomic-scale synapse with switching thresholds approaching 100 mV, Nano Lett. **19**, 2411 (2019).
[22] S. M. Hus, R. Ge, P. A. Chen, L. Liang, G. E. Donnelly, W. Ko, F. Huang, M. H. Chiang, A. P. Li, and D. Akinwande, Observation of single-defect memristor in an MoS_2 atomic sheet, Nat. Nanotechnol. **16**, 58 (2021).
[23] I. M. Datye, M. M. Rojo, E. Yalon, S. Deshmukh, M. J. Mleczko, and E. Pop, Localized heating and switching in $MoTe_2$-based resistive memory devices, Nano Lett. **20**, 1461 (2020).
[24] P. J. Zomer, M. H. Guimarães, J. C. Brant, N. Tombros, and B. J. Van Wees, Fast pick up technique for high quality heterostructures of bilayer graphene and hexagonal boron nitride, Appl. Phys. Lett. **105**, 013101 (2014).
[25] See Supplemental Material at http://link.aps.org/supplemental/10.1103/PhysRevApplied.18.014018 for additional information, which includes Refs. [22,24,26,29,32,36–41].
[26] Y. Liu, J. Guo, E. Zhu, L. Liao, S.-J. Lee, M. Ding, I. Shakir, V. Gambin, Y. Huang, and X. Duan, Approaching the Schottky–Mott limit in van der Waals metal–semiconductor junctions, Nature **557**, 696 (2018).
[27] F. Bussolotti, J. Yang, H. Kawai, C. P. Y. Wong, and K. E. J. Goh, Impact of S-vacancies on the charge injection barrier at the electrical contact with the MoS_2 monolayer, ACS Nano **15**, 2686 (2021).
[28] Q. Ma, P. M. Odenthal, J. Mann, D. Le, C. S. Wang, Y. Zhu, T. Chen, D. Sun, K. Yamaguchi, T. Tran, M. Wurch, J. L. McKinley, J. Wyrick, K. Magnone, T. F. Heinz, T. S. Rahman, R. Kawakami, and L. Bartels, Controlled argon beam-induced desulfurization of monolayer molybdenum disulfide, J. Phys.: Condens. Matter **25**, 252201 (2013).
[29] S. Tongay, J. Suh, C. Ataca, W. Fan, A. Luce, J. S. Kang, J. Liu, C. Ko, R. Raghunathanan, J. Zhou, F. Ogletree, J. Li, J. C. Grossman, and J. Wu, Defects activated photoluminescence in two-dimensional semiconductors: Interplay between bound, charged, and free excitons, Sci. Rep. **3**, 2657 (2013).
[30] D. H. Lien, S. Z. Uddin, M. Yeh, M. Amani, H. Kim, J. W. Ager, E. Yablonovitch, and A. Javey, Electrical suppression of all nonradiative recombination pathways in monolayer semiconductors, Science **471**, 468 (2019).
[31] A. Jain, P. Bharadwaj, S. Heeg, M. Parzefall, T. Taniguchi, K. Watanabe, and L. Novotny, Minimizing residues and strain in 2D materials transferred from PDMS, Nanotechnology **29**, 265203 (2018).
[32] S. V. Sivaram, A. T. Hanbicki, M. R. Rosenberger, G. G. Jernigan, H. J. Chuang, K. M. McCreary, and B. T. Jonker, Spatially selective enhancement of photoluminescence in MoS_2 by exciton-mediated adsorption and defect passivation, ACS Appl. Mater. Interfaces **11**, 16147 (2019).
[33] S. Bae, N. Sugiyama, T. Matsuo, H. Raebiger, K. I. Shudo, and K. Ohno, Defect-induced vibration modes of Ar+-irradiated MoS_2, Phys. Rev. Appl. **7**, 1 (2017).
[34] I. M. Datye, A. J. Gabourie, C. D. English, K. K. Smithe, C. J. McClellan, N. C. Wang, and E. Pop, Reduction of hysteresis in MoS_2 transistors using pulsed voltage measurements, 2D Mater. **6**, 011004 (2019).
[35] M. Calderara, S. Brück, A. Pedersen, M. H. Bani-Hashemian, J. VandeVondele, and M. Luisier, Pushing back the limit of ab-initio quantum transport simulations

on hybrid supercomputers, Proc. Int. Conf. High Perform. Comput., Networking, Storage Anal. **3**, 1 (2015).

[36] A. Kumar, K. Schauble, K. M. Neilson, A. Tang, P. Ramesh, H. S. Wong, E. Pop, and K. Saraswat, in *IEEE International Electron Devices Meeting (IEDM)* (2021), p. 7.3.1.

[37] C. D. English, G. Shine, V. E. Dorgan, K. C. Saraswat, and E. Pop, Improved contacts to MoS_2 transistors by ultra-high vacuum metal deposition, Nano Lett. **16**, 3824 (2016).

[38] J. Hutter, M. Iannuzzi, F. Schiffmann, and J. Vandevondele, Cp2k: Atomistic simulations of condensed matter systems, Wiley Interdiscip. Rev.: Comput. Mol. Sci. **4**, 15 (2014).

[39] F. Ducry, A. Emboras, S. Andermatt, M. H. Bani-Hashemian, B. Cheng, J. Leuthold, and M. Luisier, in *IEEE International Electron Devices Meeting (IEDM)* (2017), p. 4.2.1.

[40] M. Luisier, A. Schenk, W. Fichtner, and G. Klimeck, Atomistic simulation of nanowires in the $sp^3d^5s^*$ tight-binding formalism: From boundary conditions to strain calculations, Phys. Rev. B - Condens. Matter Mater. Phys. **74**, 1 (2006).

[41] M. Luisier and A. Schenk, Atomistic simulation of nanowire transistors, J. Comput. Theor. Nanosci. **5**, 1031 (2008).