van der Waals Ferroelectric Halide Perovskite Artificial Synapse

Yao Cai,[1,2,‡] Yang Hu,[2,‡] Zhizhong Chen,[2] Jie Jiang,[2] Lifu Zhang,[2] Yuwei Guo,[2] Saloni Pendse,[2] Ru Jia,[2] Jiahe Zhang,[3] Xiaolong Ma,[3] Chengliang Sun,[1,*] and Jian Shi[2,4,†]

[1] *The Institute of Technological Sciences, Wuhan University, Wuhan 430072, China*

[2] *Department of Materials Science and Engineering, Rensselaer Polytechnic Institute, Troy, New York 12180, USA*

[3] *Hongyi Honor College of Wuhan University, Wuhan 430072, China*

[4] *Center for Materials, Devices, and Integrated Systems, Rensselaer Polytechnic Institute, Troy, New York 12180, USA*

(Received 22 December 2021; accepted 9 June 2022; published 7 July 2022)

Ferroelectricity is promising in emulating the synaptic characteristics of human brains. Utilizing ferroelectricity for brain-inspired computing is proposed as a feasible route to address technical challenges in memory and computing. Here, we demonstrate the use of a ferroelectric van der Waals (vdW) halide perovskite for synaptic emulation. The two-terminal ferroelectric synapse based on the vdW material (*R*)-(−)-1-cyclohexylethylammonium)PbI_3 (*R*-CYHEAPbI_3) exhibits voltage-pulse-dependent weight modulation with a total *on*:*off* ratio of 50 and good endurance up to 10^7 cycles. The energy consumption per synaptic operation for both short-term plasticity and long-term plasticity reaches the picojoule level. The device also shows reasonable write linearity and small cycle-to-cycle variation, as well as promising spike-timing-dependent plasticity and a paired-pulse-facilitation function. Numerical simulations with the *R*-CYHEAPbI_3-synapse-based neural network suggest the potential of *R*-CYHEAPbI_3 synapses for pattern recognition. Ferroelectric vdW halide perovskites provide opportunities for exploiting their dimensionality, superior optoelectronic properties, and mild material-processing conditions for engineering of the synaptic device performance.

DOI: 10.1103/PhysRevApplied.18.014014

I. INTRODUCTION

Artificial synapses, as one of essential building blocks in neuromorphic circuits, mimic the way biological synapses memorize and learn in the human brain [1–6]. In neuromorphic circuits, learning is achieved by the tuning of the weight of each synaptic device following certain mathematical algorithms [1]. To realize efficient parallel learning and inference in neuromorphic computing, synaptic devices must carry attributes of linear and symmetric weight-excitation relationships, a large number of nonvolatile states, and a fast switching speed [1,7,8].

Among extensive demonstrations of synaptic devices [9–11], the ferroelectricity-enabled multistate memristive synapse has recently attracted attention [11–15]. In a ferroelectric synapse, nonvolatile synaptic weights are encoded in ferroelectric polarization. The multilevel polarization states of ferroelectrics are mainly due to the multiple-domain structure. So far, the most studied ferroelectric materials for synapses have been oxide ferroelectrics. They show a large polarization, reasonable number of synaptic states, good endurance, and good retention. However, material processability and defects (e.g., vacancies) have been issues for their scalability and reliable operation [16]. Expanding the materials space beyond oxides for synaptic applications may provide opportunities for addressing some issues that oxide ferroelectrics suffer from. van der Waals (vdW) halide perovskites exhibit superior electrical and optical properties with great feasibility in material processing and device miniaturization [17–21]. The demonstration of ferroelectric synapse in halide perovskites would provide us with an alternative material platform to design synapses with required characteristics [20,22–25].

Herein, we demonstrate the use of a one-dimensional (1D) vdW halide perovskite, [(*R*)-(−)-1-cyclohexylethylammonium]PbI_3 (*R*-CYHEAPbI_3), for ferroelectric synapses. As shown in Fig. 1(a), in our ferroelectric *R*-CYHEAPbI_3, Pb-I atoms crystallize as 1D face-sharing octahedral chains loosely bound by organic ligands. The inorganic lead iodine octahedra dominate the semiconducting properties, while organic molecules are responsible for switchable ferroelectric polarization [26]. The vdW nature of this material allows structural flexibility

*sunc@whu.edu.cn

†shij4@rpi.edu

‡These authors contributed equally to this work.

to enable both band transport (PbI_6) and ferroelectricity (organic groups). We successfully achieve synaptic plasticity in the *R*-CYHEAPbI$_3$ ferroelectric diode, which features a reasonable number of nonvolatile states, pulse-dependent weight update, good endurance, nearly linear weight updates, small cycle-cycle variances, and nondestructive read operations. Based on such a device, we further demonstrate short- and long-term plasticity (STP and LTP, respectively), spike-timing-dependent plasticity (STDP), and a paired-pulse-facilitation (PPF) function. With the experimental synaptic characteristics, parallel training with a back-propagation algorithm is executed in a crossbar-based two-layer neural network, which achieves a high classification accuracy.

II. METHODS AND CHARACTERIZATION

Figures 1(b) and 1(c) show the atomic crystal structures of *R*-CYHEAPbI$_3$. *R*-CYHEAPbI$_3$ belongs to the $P2_1$ space group and has lattice constants $a = 8.628$ Å, $b = 8.211$ Å, $c = 22.994$ Å, and $\beta = 89.5121°$ at room temperature [26,27]. Compared with most conventional ferroelectrics of $BaTiO_3$ and $Pb(Zr_xTi_{1-x})O_3$ [28], the halide perovskite *R*-CYHEAPbI$_3$ features large lattice constants and a low processing temperature due to the existence of large organic groups and vdW gaps [Fig. 1(a)]. We employ a solution method to synthesize mm-sized bulk crystals of *R*-CYHEAPbI$_3$ and apply a standard spin-coating approach to synthesize the thin-film form (see Experimental Section in the Supplemental Material [29]). For the spin-coating method, briefly, a saturated solution of *R*-CYHEAPbI$_3$ is spin-coated on the substates and then the film is crystallized. Figure 1(d) shows the x-ray diffraction (XRD) patterns of both *R*-CYHEAPbI$_3$ powder (ground from their single crystals) and the spin-coated film on silicon substrate with an Au electrode deposited on top. With the simulated XRD result for an ideal *R*-CYHEAPbI$_3$ crystal from our previous research [26], we can confirm the synthesis and deposition of the expected polar $P2_1$ phase (Experimental Section in the Supplemental Material [29]).

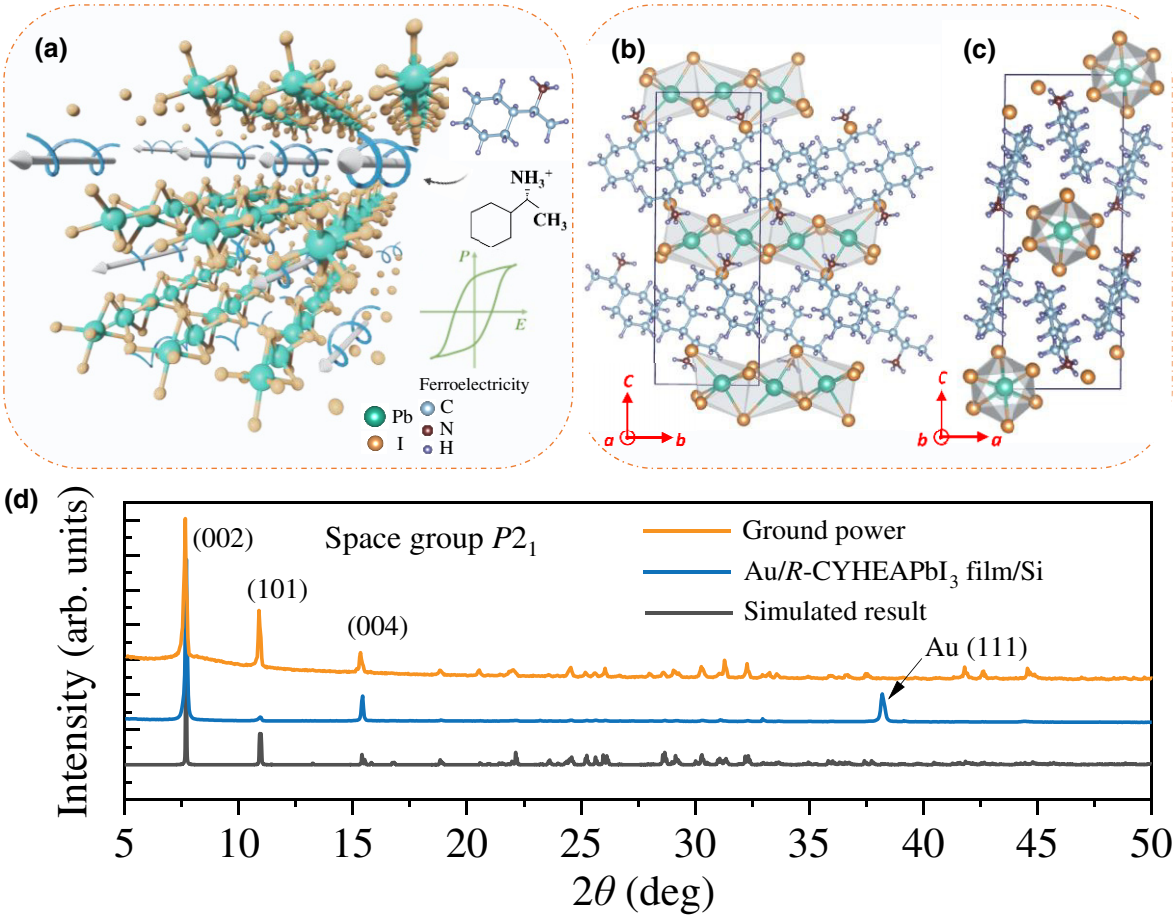

FIG. 1. Ferroelectric 1D soft vdW halide perovskite *R*-CYHEAPbI$_3$. (a) Schematic of *R*-CYHEAPbI$_3$ crystal structure consisting of lead halogen octahedra (PbI_6) and chiral organic groups. Helixes represent the chiral organic groups and arrows represent the direction of ferroelectric polarization (*b* direction). Atomic structures of the *R*-CYHEAPbI$_3$ crystal: (b) side view from *a* direction and (c) side view from *b* direction. (d) Experimental XRD results of ground powder form of *R*-CYHEAPbI$_3$ and spin-coating film compared to the simulated one. Au (111) peak rises from the top Au electrode.

In the spin-coated film with an Au electrode, the XRD result shows the presence of the Au (111) peak. The simple spin-coating approach for fabricating the *R*-CYHEAPbI$_3$ thin film makes it easily to integrate into many technologically important substrates.

The ferroelectric property of *R*-CYHEAPbI$_3$ for both the single-crystal and thin-film forms is reported in our previous work [26]. More information about the intrinsic properties of *R*-CYHEAPbI$_3$ can be found in our previous work [26]. It is shown that the polar axis of *R*-CYHEAPbI$_3$ is the *b* direction. Similar to many other vdW materials [30], when the thin-film form is developed, most grains align their nonpolar axes (the axes that are perpendicular to the vdW-gap planes) along the out-of-plane direction of the film and only a small portion of grains with their polar axes are aligned with the out-of-plane direction of the film [26]. Under a vertical device configuration, the ferroelectric polarization of the device is thus proportional to the percentage of grains with the *b* axis aligned along the out-of-plane direction of the film. Such a relationship was experimentally confirmed in our previous work [26]. Based upon our current and former understanding of the ferroelectric property of the *R*-CYHEAPbI$_3$ material, we further fabricate a synaptic device and explore the synaptic behavior [Fig. 2(a)] based on the thin-film structure of *R*-CYHEAPbI$_3$. A schematic and the morphology of the two-terminal ferroelectric diode is shown in Figs. S1(a) and S1(b) within the Supplemental Material [29], in which the *R*-CYHEAPbI$_3$ thin film is sandwiched between the top Au electrode and the bottom *n*-type Si (*n*-Si). The polarization-electric field measurement [Fig. S1(c) in the Supplemental Material [29]] shows that the magnitude of ferroelectric polarization of our thin film is consistent with previously reported ones. Figure S1(d) within the Supplemental Material [29] confirms the stable *I*-*V* curves with applied voltages from −0.6 to 0.6 V for 50 loops.

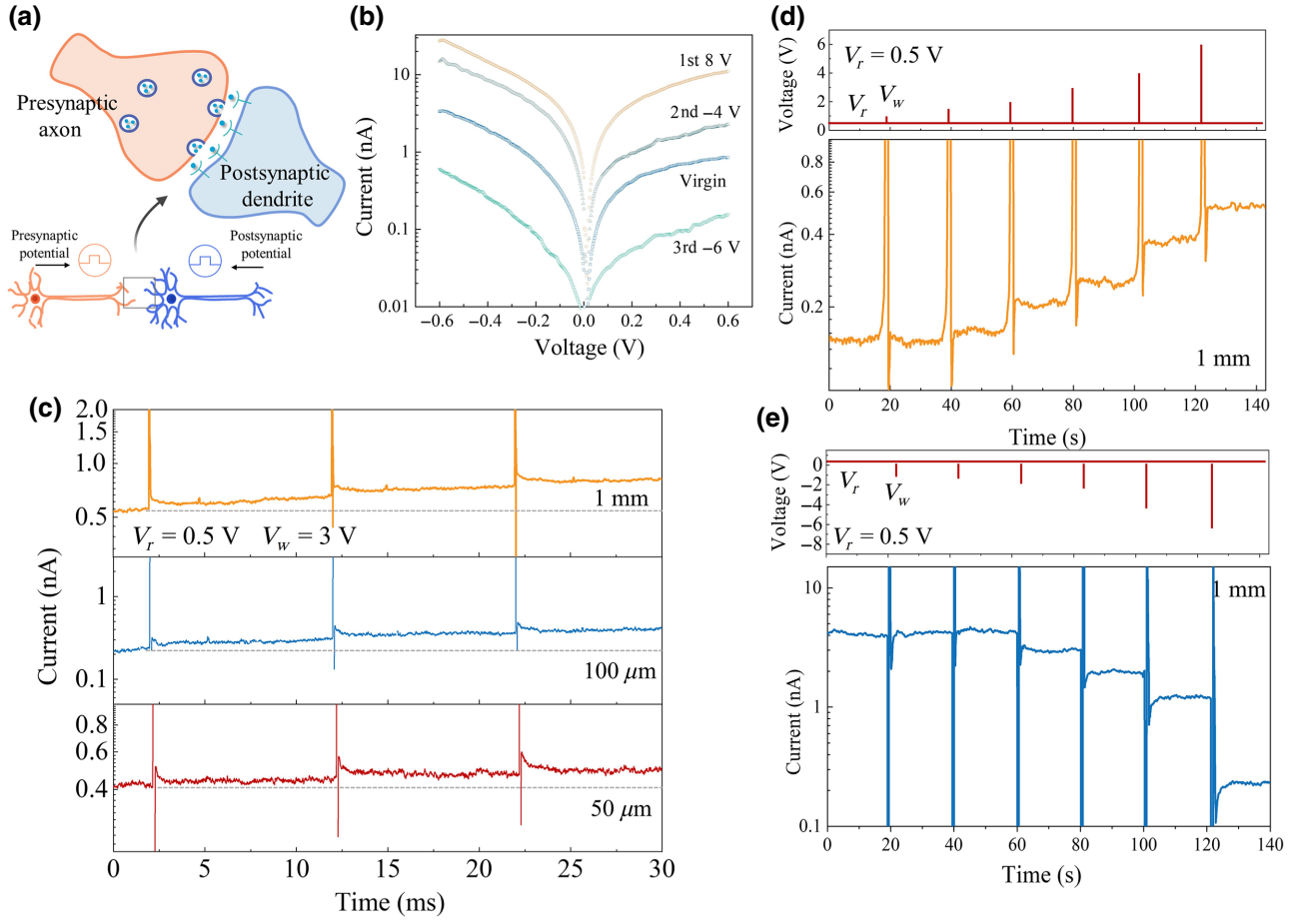

FIG. 2. Characterization of a two-terminal *R*-CYHEAPbI$_3$ ferroelectric diode. (a) Our proposed ferroelectric synaptic device mimics the biological synapse, the weight of which is modified by presynaptic and postsynaptic potentials. (b) *I*-*V* curves of *R*-CYHEAPbI$_3$ ferroelectric device at different poling voltages following a poling sequence of "virgin" → 8 V for 30 s → −4 V for 30 s → −6 V for 30 s. (c) Variable EPSCs of *R*-CYHEAPbI$_3$ ferroelectric device with different Au-electrode diameters of 1 mm, 100 μm, and 50 μm. Write voltage (V_w) is 3 V with a duration of 500 μs, and read voltage (V_r) is 0.5 V. (d),(e) Varying resistances after positive and negative write voltage (V_w) with a pulse of 0.5 s. Read voltage (V_r) is 0.5 V, and read length is almost 20 s.

III. RESULTS AND DISCUSSION

The weight of the *R*-CYHEAPbI$_3$ synapse is emulated by the resistance of the ferroelectric diode, which is a function of the relative fraction of aligned ferroelectric domains [31]. External write-voltage pulses applied to the device are expected to modify the fraction of aligned domains, thus causing resistance to change [32]. Figure 2(b) shows the *I*-*V* curves of our Au/*R*-CYHEAPbI$_3$/Si device, with an Au-electrode diameter of 1 mm, after different write-voltage (V_w) pulses (Au electrode is the positive terminal) with a duration of 30 s. For each V_w, the following sequence is used: the virgin state (0 V) → first pulse (8 V) → second pulse (−4 V) → third pulse (−6 V). A large dynamic window of the forward current (at 0.5-V read voltage, V_r) of 2 orders of magnitude is observed. With the designed voltage-poling sequence, we observe that a positive voltage leads to a drop in resistance, while a negative voltage pulse gives a rise. Since our film is relatively thick beyond the tunneling regime, the transport behavior of our ferroelectric diode can be understood from a thermionic model involving potential barriers modified by ferroelectric polarization. The observation in Fig. 2(b) thus shows that voltage-tuned ferroelectric polarization can change the synaptic weight of our device. We adopt a pulsed V_w on the *R*-CYHEAPbI$_3$ synapses with three different electrode diameters of 1 mm, 100 μm, and 50 μm to study the synaptic characteristics. As shown in Fig. 2(c), a V_w of 3 V with a pulse duration of 500 μs as the presynaptic spikes applied to the Au electrode can bring the variable excitatory postsynaptic currents (EPSCs). The EPSCs of *R*-CYHEAPbI$_3$ synapses increase under a positive presynaptic spike (or V_w). Investigations of the voltage-pulse-dependent weight update at a constant-voltage duration per pulse are also conducted, with the results shown in Figs. 2(d) and 2(e), in which V_r is fixed at 0.5 V and six different voltage pulses are employed. It is shown that positive or negative V_w pulses with increasing voltage magnitudes and the same pulse duration of 0.5 s lead to varying degrees of change in resistance. When the magnitudes of positive or negative V_w are bigger than 2 V, the resistances of the ferroelectric diode can change significantly.

Figure 3(a) shows resistance-V_w hysteresis loops with the resistance measured at a V_r of 0.5 V. In characterizing the resistance–write-voltage loop, V_w pulses are continuously applied following the path of 0 V → 9.2 V → (−6.4 V) → 0 V. It is found that *R*-CYHEAPbI$_3$ synapses can switch between a

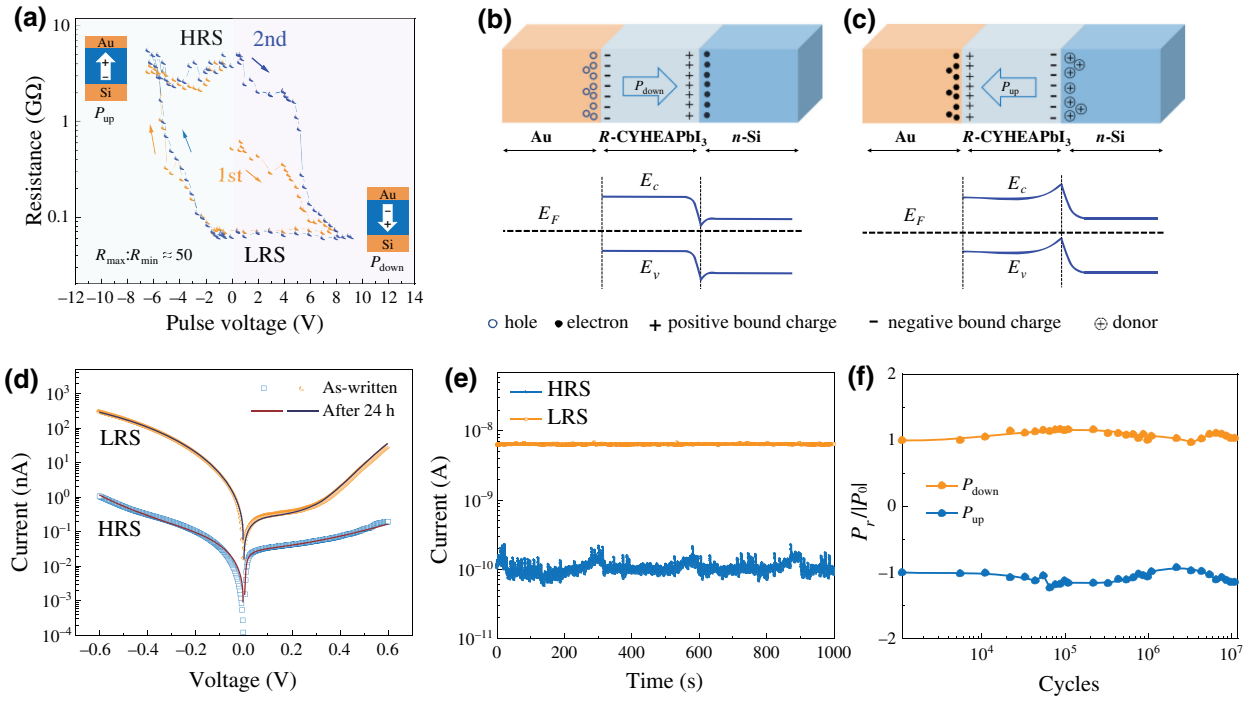

FIG. 3. Tunable resistance of two-terminal *R*-CYHEAPbI$_3$ synapses. (a) Resistance hysteresis loops versus pulse V_w (each pulse is 10 s). V_r is 0.5 V. Starting from the initial state of the *R*-CYHEAPbI$_3$ device (central orange point), two loops are collected. Schematics of polarization states are shown in the bottom right (P_{down}) and top left (P_{up}). Illustrations of ferroelectric-polarization-modified carrier distributions and band diagrams: (b) ferroelectric polarization points to *n*-Si interface (P_{down}) after applying positive V_w; (c) ferroelectric polarization points to Au electrode (P_{up}) after applying negative V_w. E_F, E_c, and E_v represent Fermi level, conduction-band minimum, and valence-band maximum, respectively. (d) Comparisons of *I*-*V* curves of as-written and after-24-h LRS and HRS. (e) Retention performance of synaptic devices at HRS and LRS with 1000-s-duration read. (f) Fatigue endurance tests of remanent polarization.

high-resistance state (HRS, $R_{max} \sim 3 \times 10^9$ Ω) and a low-resistance state (LRS, $R_{min} \sim 6 \times 10^7$ Ω) continuously. A higher V_w leads to a larger change of resistance, as implied by the slope of the resistance–write-voltage curves. When V_w is above 8 V or below −5.6 V, the resistance change pauses, suggesting that the polarization may reach its saturation value. Overall, the resistance change follows a multiple-state transition with a resistance span of almost 50 times.

Figures 3(b) and 3(c) illustrate the proposed resistance-switching mechanism. The observed resistance switching can be explained by the tuning of the height of the potential barrier and the width of the depletion region at the *R*-CYHEAPbI$_3$-electrode interface [33–35]. When current flows from Au to Si, the barrier height at the *R*-CYHEAPbI$_3$-electrode interface determines its value [32,34–36]. Specifically, after applying a positive V_w, some ferroelectric dipoles point to *n*-Si (P_{down}). Positive bound charges at the interface between *R*-CYHEAPbI$_3$ and *n*-Si result in a reduced barrier height [34,35]. In this case, under a small positive V_r, the device exhibits a relatively lower resistance than that before the positive write pulse is applied [Fig. 3(b)]. In contrast, when some of the dipoles are flipped towards the Au electrode (P_{up}) under negative V_w, as shown in Fig. 3(c), the negative ferroelectric bound charges at the interface between *R*-CYHEAPbI$_3$ and *n*-Si increase the barrier height. In this case, a higher resistance is expected.

As shown in Fig. 3(d), the LRS and HRS of the synaptic devices are obtained after applying a V_w of 10 and −6.4 V, respectively, with a duration of 30 s. The *I*-*V* characteristics of the device right after writing and after it is exposed to air for 24 h are almost identical, suggesting a good retention time of the analog states for our device. Figure 3(e) shows the retention performance of synaptic devices at the HRS and LRS, in which no obvious deterioration is found within the 1000-s-duration read. The R_{max}:R_{min} ratio of this synaptic device with the 100-nm-thick *R*-CYHEAPbI$_3$ film is close to 50. Furthermore, we fabricate two-terminal *R*-CYHEAPbI$_3$ synapses with two different thickness of 160 nm [Fig. S2(a) within the Supplemental Material [29]] and 60 nm [Fig. S2(b) within the Supplemental Material [29]] with R_{max}:R_{min} ratios of 33 and 65, respectively. The dependence of the R_{max}/R_{min} ratio on the film thickness can contribute to the relative percentile of the width of the depletion region over the whole film thickness [33–35]. The polarization switching of the *R*-CYHEAPbI$_3$ film is tested by using the positive up negative down (PUND) method (Experimental Section in the Supplemental Material [29]). After 10^7 bipolar-switching cycles, the remanent polarization remains almost the same as the initial value of the poled *R*-CYHEAPbI$_3$ film [Fig. 3(f), P_0 is the remanent polarization at the first poling cycle].

The STP and LTP are the basis synaptic functionalities executing neural computation [37,38]. Typical STP behaviors of our Au/*R*-CYHEAPbI$_3$/Si synapses can be obtained by applying small V_w pulses. As shown in Figs. S3(a) and S3(b) within the Supplemental Material [29] EPSCs are trigged by a small V_w of 1 V with a duration of 500 μs and the magnitude of the EPSC decays rapidly to the initial states, which indicates that only a temporal-enhanced connection exists between two adjacent neurons [39]. Figure 4(a) shows the characteristic of the PPF, which reflects the activity-dependent enhancement of the EPSC evoked by the second pulse [40]. The inset in Fig. 4(a) is the PPF performance with a pulse interval of 180 μs. The plasticity of the PPF is calculated as the increased proportion of the second peak current compared with the first peak current [37]. Under a paired pulse with a magnitude of 1.5 V and duration of 500 μs each, the plasticity of the PPF is near to zero, indicating that the influence of the first EPSC is effectively eliminated when stimuli with pulse intervals larger than 280 μs are applied. In neurobiology, STP can be converted into LTP by applying an enhanced magnitude or duration of external stimulation [11]. Figures S3(c) and S3(d) within the Supplemental Material [29] show increasing EPSCs under a V_w of 4 V with a duration of 500 μs, suggesting the characteristic of long-term memory in *R*-CYHEAPbI$_3$ synapses. Using the stimulus signals shown in Fig. S3 within the Supplemental Material [29], the calculated energy consumption per spike of *R*-CYHEAPbI$_3$ synapses with an Au-electrode diameter of 1 mm is 27 and 70 pJ, respectively, when conducting STP and LTP processing [2]. As the Au-electrode diameter decreases to 50 μm, the energy consumption per spike is 0.25 and 6.6 pJ for STP and LTP processing, respectively. The electrode-area dependence of energy consumption per synaptic operation suggests that one may further reduce the power consumption by reducing the electrode area.

STDP, as a form of Hebbian learning, is closely related to the information processing and synaptic characteristics [2,37,38]. Changes to the synaptic weight and the performance of long-term potentiation or depression depend on Δt, which is defined as the relative time interval of the pre- and postsynaptic spikes. To emulate the STDP functionality of *R*-CYHEAPbI$_3$ synapses, the Au electrode, as the presynaptic neurons, is connected to a multiplexer and the Si electrode is earthed [Fig. S4(a) in the Supplemental Material [29]]. The multiplexer is used to convert the time difference between pre- and postsynaptic spikes, and details of the circuitry and logic of the multiplexer can be found in Figs. S4(b) and S4(c) within the Supplemental Material [29] [6,41]. As shown in Fig. S4(b) within the Supplemental Material [29], the adopted asymmetric STDP is conducted with the principle that the voltage pulse with a duration of 500 μs is proportional to Δt. Figure 4(b) shows the measured nonvolatile modifications of the synaptic weight (the conductance of *R*-CYHEAPbI$_3$ synapses) with different initial resistance states. When

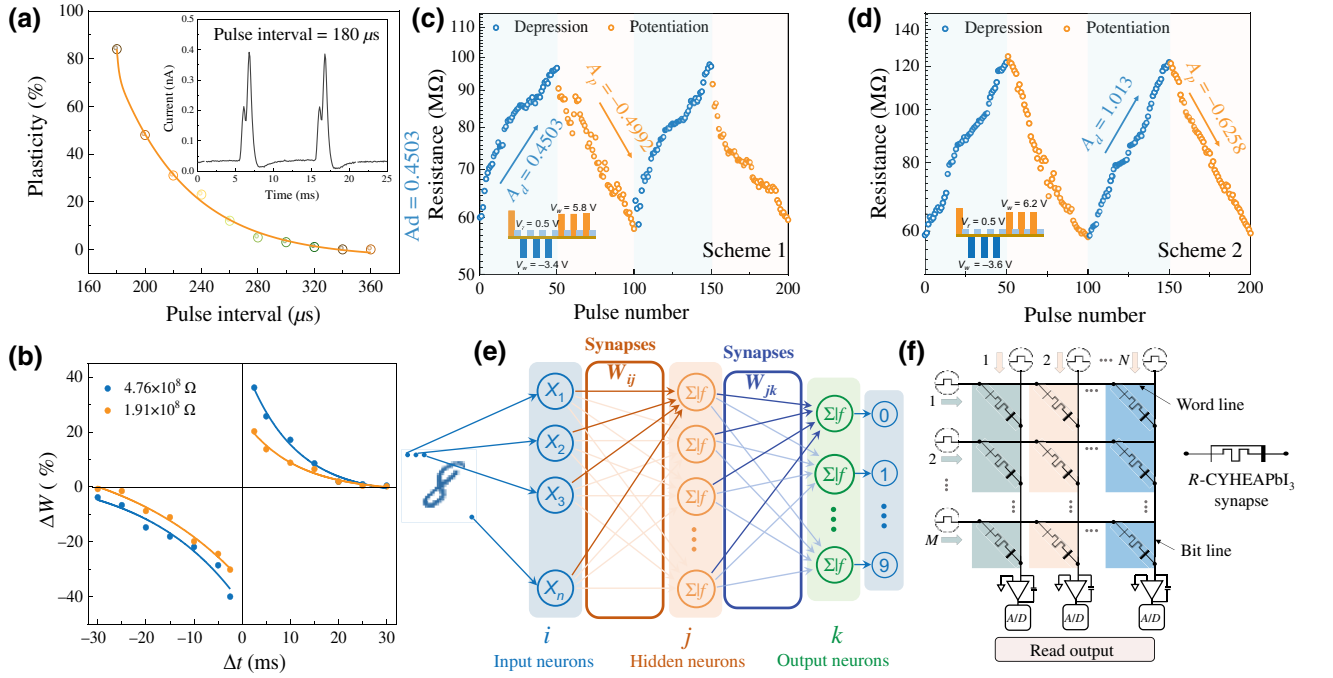

FIG. 4. Write-read operations of R-CYHEAPbI$_3$ synapses and the neural network. (a) PPF of R-CYHEAPbI$_3$ synapses under a paired pulse with a magnitude of 1.5 V and duration of 500 μs each. Inset is the PPF performance with a pulse interval of 180 μs. (b) STDP functionality of R-CYHEAPbI$_3$ synapses with initial resistances of 4.76×10^8 and 1.91×10^8 Ω. ΔW is the change ratio of conductance. Depressing and potentiating properties of R-CYHEAPbI$_3$ synapses with two different write schemes: (c) scheme 1 and (d) scheme 2. V_r and corresponding V_w with a pulse of 0.5 s are shown schematically in the bottom-left insets. Depressing and potentiating V_w are −3.4 and 5.8 V, respectively, for Scheme 1 and −3.6 and 6.2 V, respectively, for Scheme 2. V_r is 0.5 V and both schemes start from initial $R_{\min}$ state. $A_{d,p}$ represents the write linearity. (e) Schematic of our proposed two-layer neural network. $\mathbf{W}_{ij}$ and $\mathbf{W}_{jk}$ represent weight matrices. (f) Sigmoidal nonlinear activation function. (f) Our proposed crossbar structure with M input rows (word lines) and N output columns (bit lines) based on R-CYHEAPbI$_3$ synapses for performing analog matrix operations.

a postsynaptic spike is fired before a presynaptic spike ($\Delta t < 0$), a negative voltage pulse is applied to the Au electrode, leading to a synaptic depression, while synaptic potentiation occurs if $\Delta t > 0$. Moreover, with a shorter Δt, a larger change of the synaptic weight is obtained.

Figures 4(c) and 4(d) demonstrate synaptic potentiation and depression of LTP using R-CYHEAPbI$_3$ synapses. We adopt different write schemes: scheme 1 includes a depressing voltage of −3.4 V and a potentiating voltage of 5.8 V; scheme 2 includes a depressing voltage of −3.6 V and a potentiating voltage of 6.2 V; three other write schemes (3–5) can be seen in Fig. S5 within the Supplemental Material [29]. Each V_w pulse lasts for 0.5 s. Both write schemes 1 and 2 lead to 50 resistance states (V_r is 0.5 V). Following the definition of linearity of a synaptic device [14,42], we find that, using scheme 1, the linearity of depression, $A_{d,1}$, is 0.4503 and potentiation, $A_{p,1}$, is −0.4992. In write scheme 2, the linearity of depression, $A_{d,2}$, is 1.013 and potentiation, $A_{p,2}$, is −0.6258. A larger absolute value of $A_{d,p}$ implies a better linearity for potentiation or depression (Experimental Section in Supplemental Material [29]) [39,42]. Such a linearity value is comparable to some of the best-performing artificial synapses (see Table S1 within the Supplemental Material [29]). We also find that scheme 2 leads to a larger dynamic range, which is reasonable, as scheme 2 uses a higher write voltage [31].

To evaluate the potential of the R-CYHEAPbI$_3$ synapse in a neural network for learning tasks like pattern recognition, as shown in Figs. 4(e) and 4(f), we design R-CYHEAPbI$_3$ synapses in a two-layer neural network (one hidden layer) based on two crossbar arrays. In Fig. 4(e), $\mathbf{W}_{ij}$ and $\mathbf{W}_{jk}$ represent the weight matrices connecting the input layer to the hidden layer (the first crossbar array) and the hidden layer to the output layer (the second crossbar array), respectively. As illustrated in Fig. 4(f), the crossbar array with M input rows (word lines) and N output columns (bit lines) is used to carry out parallel read and write operations. Individual synapses ij and jk can be reached from the ith-word line and j th-bit line and j th-word line and kth-bit line, respectively [43]. With this, we conduct supervised learning with a back-propagation algorithm and sigmoidal nonlinear activation function (details in Fig. S6 within the Supplemental Material [29]) [43–45]. This artificial neural network is trained with two data sets: an 8 × 8-pixel-image version of

handwritten digits [46] and a 28 × 28-pixel-image version of handwritten digits [47]. The training and classification information associated with 8 × 8 and 28 × 28 image sets is summarized in Table S2 within the Supplemental Material [29]. A learning rate of $\eta = 0.1$ is used to train both image sets.

Figures 5(a)–5(f) show the weight patterns and distributions of synapses connecting the input layer to the hidden layer at different training epochs (for 8 × 8 image set) [48,49]. The corresponding matrix is 64 (input elements) × 36 (output elements). The weight-pattern and distribution evolution for the 28 × 28 image set are presented in Figs. S7 and S8 within the Supplemental Material [29]. The initial weights (0th epoch) of the *R*-CYHEAPbI$_3$ synapses are generated randomly [Fig. 5(a) and Fig. S7(a) within the Supplemental Material [29]]. To minimize the negative impact of synaptic nonlinearity and write (read) noise, and to prevent potential weight saturation, the weights of the *R*-CYHEAPbI$_3$ synapses are set to stay within 25% to 75% of the whole conductance range during training [43]. It can be seen that, after training, the weight-distribution profile exhibits multiple peaks spanning a relatively reasonable range, as shown in Figs. 5(e) and 5(f) and Fig. S8 within the Supplemental Material [29]. From the probability density of synaptic conductance [Figs. 5(d)–5(f) and Fig. S8 within the Supplemental Material [29]], we can see that the weights are updated rapidly after the first-few training epochs and then remain relatively stable. This indicates that highly efficient training is achieved within a few iterations.

Figure 5(g) shows that reasonable classification accuracies can be reached very rapidly during training. For example, for the 8 × 8 image set, after five epochs, for training scheme 1, the classification accuracy reaches 85.1%. For training scheme 2, it is 91.5%. The better performance of scheme 2 is likely to be due to its better synaptic linearity [1]. Figure 5(h) shows a similar observation, in which the training data set is the 28 × 28 image set. Compared with the classification accuracy of an ideal numeric from the floating-point-based neural-network performance [1,37], the classification accuracies of both schemes 1 and 2 are slightly lower for the 8 × 8 image set [43]. Figure S9(a) within the Supplemental Material [29] shows the classification accuracies of the 8 × 8 image set obtained using 0% to 100% and 25% to 75% of the weight ranges of schemes 1 and 2. It can be seen that the classification accuracies using 25% to 75% of the weight range indeed reach a higher value. Comparisons of the classification accuracies using schemes 1 to 2 can also prove that better linearity is helpful for achieving good computing results. A comparison of the performance of our *R*-CYHEAPbI$_3$ synapse with several typical memristive devices is shown in Table S1 within the Supplemental Material [29] [37,39,50–55]. From Table S1 within the

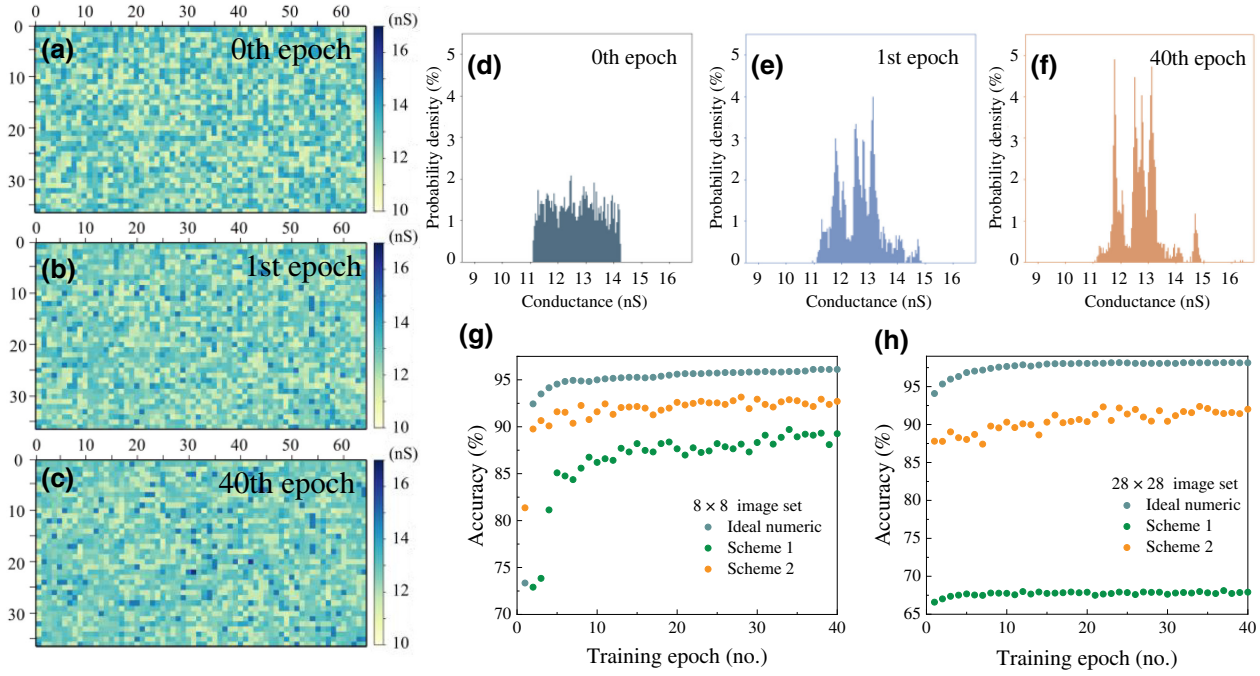

FIG. 5. Pattern recognition using the proposed neural network following a back-propagation algorithm. (a)–(f) Weight (conductance) distributions and corresponding probability-density plots of the first crossbar array (connecting the input layer to the hidden layer) during training with synaptic plasticity following the one in Fig. 4(b) (scheme 2): (a),(d) initial state (0th epoch); (b),(e) after the 1st training epoch; (c),(f) after the 40th training epoch. Each pixel in (a)–(c) represents the conductance of each *R*-CYHEAPbI$_3$ synapse in the first crossbar array. (g),(h) Classification accuracies versus training epochs for 8 × 8 and 28 × 28 image sets, respectively.

Supplemental Material [29], it can be seen that the energy consumption per synaptic operation for our vdW system is comparable to or better than that of several synaptic systems, making it a promising candidate for brainlike computing. Although the dynamic range of weights in our synapses is smaller than some of the former devices [14,37,50,52], the *R*-CYHEAPbI$_3$ device still exhibits a good linearity and small cycle-to-cycle variation, which seem to contribute more to receiving better accuracies.

IV. CONCLUSION

We propose and experimentally demonstrate a vdW halide-perovskite-based ferroelectric synapse. We show that individual devices exhibit a promising synaptic linearity and low cycle-to-cycle variation. By optimizing the voltage-pulse parameters, the *R*-CYHEAPbI$_3$ synapses can process with a switching speed within hundreds of microseconds and an energy consumption per spike at the picojoule level for STP and LTP operations. Crossbar-structured two-layer neural-network simulations based on *R*-CYHEAPbI$_3$ synapses with back-propagation algorithms show that our synaptic device and circuit can perform efficient learning and reach a reasonable classification accuracy (92%) with a low number of training epochs. Our work suggests the prospective potential of a ferroelectric vdW halide perovskite for energy-efficient information processing and computing.

Data and code are available from the corresponding authors upon reasonable request.

ACKNOWLEDGMENTS

Y.C. and C.S. acknowledge support from the China Scholarship Council, National Natural Science Foundation of China (Grant No. 61974107). J.S. and L.Z. acknowledge support from the National Science Foundation under Grant No. 1916652 and NYSTAR under Contract No. C180117. The authors would like to acknowledge Professor Sapan Agarwal (Research Scientist at Sandia National Laboratories), Professor Rongjie Lai, and Ms. Jiajia Yu (Department of Mathematics, Rensselaer Polytechnic Institute) for discussions about the neuromorphic algorithm, and Professor Qidong Tai and Dr. Xiang Zhang (Wuhan University) for the material growth.

The authors declare no competing financial interest.

[1] E. J. Fuller, S. T. Keene, A. Melianas, Z. Wang, S. Agarwal, Y. Li, Y. Tuchman, C. D. James, M. J. Marinella, and J. J. Yang, Parallel programming of an ionic floating-gate memory array for scalable neuromorphic computing, Science **364**, 570 (2019).

[2] C. Ge, G. Li, Q. L. Zhou, J. Y. Du, E. J. Guo, M. He, C. Wang, G. Z. Yang, and K. J. Jin, Gating-induced reversible H_xVO_2 phase transformations for neuromorphic computing, Nano Energy **67**, 104268 (2020).

[3] I. Boybat, M. Le Gallo, S. Nandakumar, T. Moraitis, T. Parnell, T. Tuma, B. Rajendran, Y. Leblebici, A. Sebastian, and E. Eleftheriou, Neuromorphic computing with multi-memristive synapses, Nat. Commun. **9**, 1 (2018).

[4] S. D. Ha, J. Shi, Y. Meroz, L. Mahadevan, and S. Ramanathan, Neuromimetic Circuits with Synaptic Devices Based on Strongly Correlated Electron Systems, Phys. Rev. Appl. **2**, 064003 (2014).

[5] J. Shi, Y. Zhou, and S. Ramanathan, Colossal resistance switching and band gap modulation in a perovskite nickelate by electron doping, Nat. Commun. **5**, 1 (2014).

[6] J. Shi, S. D. Ha, Y. Zhou, F. Schoofs, and S. Ramanathan, A correlated nickelate synaptic transistor, Nat. Commun. **4**, 1 (2013).

[7] M. J. Marinella, S. Agarwal, A. Hsia, I. Richter, R. Jacobs-Gedrim, J. Niroula, S. J. Plimpton, E. Ipek, and C. D. James, Multiscale co-design analysis of energy, latency, area, and accuracy of a ReRAM analog neural training accelerator, IEEE J. Emerg. Sel. Top. Circuits Syst. **8**, 86 (2018).

[8] J. T. Yang, C. Ge, J. Y. Du, H. Y. Huang, M. He, C. Wang, H. B. Lu, G. Z. Yang, and K. J. Jin, Artificial synapses emulated by an electrolyte-gated tungsten-oxide transistor, Adv. Mater. **30**, 1801548 (2018).

[9] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, The missing memristor found, Nature **453**, 80 (2008).

[10] G. W. Burr, R. M. Shelby, S. Sidler, C. Di Nolfo, J. Jang, I. Boybat, R. S. Shenoy, P. Narayanan, K. Virwani, and E. U. Giacometti, Experimental demonstration and tolerancing of a large-scale neural network (165000 synapses) using phase-change memory as the synaptic weight element, IEEE Trans. Electron Devices **62**, 3498 (2015).

[11] J. Zhu, T. Zhang, Y. Yang, and R. Huang, A comprehensive review on emerging artificial neuromorphic devices, Appl. Phys. Rev. **7**, 011312 (2020).

[12] S. Oh, H. Hwang, and I. Yoo, Ferroelectric materials for neuromorphic computing, Apl. Mater. **7**, 091109 (2019).

[13] Z. Wen and D. Wu, Ferroelectric tunnel junctions: Modulations on the potential barrier, Adv. Mater. **32**, 1904123 (2019).

[14] M. Jerry, P.-Y. Chen, J. Zhang, P. Sharma, K. Ni, S. Yu, and S. Datta, in *2017 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2017), Vol. 6, pp. 2.

[15] Y. Chen, Y. Zhou, F. Zhuge, B. Tian, M. Yan, Y. Li, Y. He, and X. S. Miao, Graphene–ferroelectric transistors as complementary synapses for supervised learning in spiking neural network, npj 2D Mater. Appl. **3**, 1 (2019).

[16] H. Li, R. Wang, S. Han, and Y. Zhou, Ferroelectric polymers for non-volatile memory devices: A review, Polym. Int. **69**, 533 (2020).

[17] I. Raifuku, Y. P. Chao, H. H. Chen, C. F. Lin, P. E. Lin, L. C. Shih, K. T. Chen, J. Y. Chen, J. S. Chen, and P. Chen, Halide perovskite for low-power consumption neuromorphic devices, EcoMat **3**, e12142 (2021).

[18] N. Pandech, T. Kongnok, N. Palakawong, S. Limpijumnong, W. R. Lambrecht, and S. Jungthawan, Effects of the van der Waals interactions on structural and electronic properties of $CH_3NH_3(Pb, Sn)(I, Br, Cl)_3$ halide perovskites, ACS Omega **5**, 25723 (2020).

[19] Y. Guo, W. A. Saidi, and Q. Wang, 2D halide perovskite-based van der Waals heterostructures: Contact evaluation and performance modulation, 2D Mater. **4**, 035009 (2017).

[20] J. Gong, H. Yu, X. Zhou, H. Wei, M. Ma, H. Han, S. Zhang, Y. Ni, Y. Li, and W. Xu, Lateral artificial synapses on hybrid perovskite platelets with modulated neuroplasticity, Adv. Funct. Mater. **30**, 2005413 (2020).

[21] J. Gong, H. Wei, Y. Ni, S. Zhang, Y. Du, and W. Xu, Methylammonium halide-doped perovskite artificial synapse for light-assisted environmental perception and learning, Mater. Today Phys. **21**, 100540 (2021).

[22] S. Chen and J. Huang, Recent advances in synaptic devices based on halide perovskite, ACS Appl. Electron. Mater. **2**, 1815 (2020).

[23] G. Roma, A. Marronnier, and J. Even, From latent ferroelectricity to hyperferroelectricity in alkali lead halide perovskites, Phys. Rev. Mater. **4**, 092402 (2020).

[24] H. Yu, J. Gong, H. Wei, W. Huang, and W. Xu, Mixed-halide perovskite for ultrasensitive two-terminal artificial synaptic devices, Mater. Chem. Front. **3**, 941 (2019).

[25] J. Gong, H. Yu, H. Wei, Y. Zheng, C. Yuan, M. Ma, H. Han, K. Guo, J. Xu, and W. Xu, An air-stable two-dimensional perovskite artificial synapse, Semicond. Sci. Technol. **35**, 104001 (2020).

[26] Y. Hu, F. Florio, Z. Chen, W. A. Phelan, M. A. Siegler, Z. Zhou, Y. Guo, R. Hawks, J. Jiang, and J. Feng, A chiral switchable photovoltaic ferroelectric 1D perovskite, Sci. Adv. **6**, eaay4213 (2020).

[27] K. Momma and F. Izumi, VESTA 3 for three-dimensional visualization of crystal, volumetric and morphology data, J. Appl. Crystallogr. **44**, 1272 (2011).

[28] L. You, Y. Zhang, S. Zhou, A. Chaturvedi, S. A. Morris, F. Liu, L. Chang, D. Ichinose, H. Funakubo, and W. Hu, Origin of giant negative piezoelectricity in a layered van der Waals ferroelectric, Sci. Adv. **5**, eaav3780 (2019).

[29] See the Supplemental Material at http://link.aps.org/supplemental/10.1103/PhysRevApplied.18.014014, which includes Refs. [14,26,27,37,39,42,46–55], for details of the Experimental Section, and the write linearity of *R*-CYHEAPbI$_3$ synapses.

[30] J. Choi, J. S. Han, K. Hong, S. Y. Kim, and H. W. Jang, Organic–inorganic hybrid halide perovskites for memories, transistors, and artificial synapses, Adv. Mater. **30**, 1704002 (2018).

[31] A. Chanthbouala, V. Garcia, R. O. Cherifi, K. Bouzehouane, S. Fusil, X. Moya, S. Xavier, H. Yamada, C. Deranlot, and N. D. Mathur, A ferroelectric memristor, Nat. Mater. **11**, 860 (2012).

[32] S. Boyn, J. Grollier, G. Lecerf, B. Xu, N. Locatelli, S. Fusil, S. Girod, C. Carrétéro, K. Garcia, and S. Xavier, Learning through ferroelectric domain dynamics in solid-state synapses, Nat. Commun. **8**, 1 (2017).

[33] R. Meyer and R. Waser, Hysteretic resistance concepts in ferroelectric thin films, J. Appl. Phys. **100**, 051611 (2006).

[34] Z. Hu, Q. Li, M. Li, Q. Wang, Y. Zhu, X. Liu, X. Zhao, Y. Liu, and S. Dong, Ferroelectric memristor based on Pt/$BiFeO_3$/Nb-doped $SrTiO_3$ heterostructure, Appl. Phys. Lett. **102**, 102901 (2013).

[35] Z. Wen, C. Li, D. Wu, A. Li, and N. Ming, Ferro electric-field-effect-enhanced electroresistance in metal/ferroelectric/semiconductor tunnel junctions, Nat. Mater. **12**, 617 (2013).

[36] L. Pintilie, in *Ferroelectrics - Physical Effects*, edited by M. Lallart (IntechOpen, London, 2011), p. 654.

[37] J. Li, C. Ge, J. Du, C. Wang, G. Yang, and K. Jin, Reproducible ultrathin ferroelectric domain switching for high-performance neuromorphic computing, Adv. Mater. **32**, 1905764 (2020).

[38] G. Q. Bi and M. M. Poo, Synaptic modification by correlated activity: Hebb's postulate revisited, Annu. Rev. Neurosci. **24**, 139 (2001).

[39] M. K. Kim and J. S. Lee, Ferroelectric analog synaptic transistors, Nano Lett. **19**, 2044 (2019).

[40] J. X. Bao, E. R. Kandel, and R. D. Hawkins, Involvement of pre- and postsynaptic mechanisms in posttetanic potentiation at Aplysia synapses, Science **275**, 969 (1997).

[41] Y. Nishitani, Y. Kaneko, M. Ueda, T. Morie, and E. Fujii, Three-terminal ferroelectric synapse device with concurrent learning function for artificial neural networks, J. Appl. Phys. **111**, 124108 (2012).

[42] P. Y. Chen, X. Peng, and S. Yu, NeuroSim: A circuit-level macro model for benchmarking neuro-inspired architectures in online learning, IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. **37**, 3067 (2018).

[43] S. Agarwal, S. J. Plimpton, D. R. Hughart, A. H. Hsia, I. Richter, J. A. Cox, C. D. James, and M. J. Marinella, in *2016 International Joint Conference on Neural Networks (IJCNN)* (2016), pp. 929.

[44] E. J. Fuller, F. E. Gabaly, F. Léonard, S. Agarwal, S. J. Plimpton, R. B. Jacobs-Gedrim, C. D. James, M. J. Marinella, and A. A. Talin, Li-ion synaptic transistor for low power analog computing, Adv. Mater. **29**, 1604310 (2017).

[45] Y. van de Burgt, E. Lubberman, E. J. Fuller, S. T. Keene, G. C. Faria, S. Agarwal, M. J. Marinella, A. A. Talin, and A. Salleo, A non-volatile organic electrochemical device as a low-voltage artificial synapse for neuromorphic computing, Nat. Mater. **16**, 414 (2017).

[46] K. Bache and M. Lichman, *UCI Machine Learning Repository* (University of California at Irvine, School of Information and Computer Science, Irvine, CA, USA, 2013).

[47] Y. LeCun, L. Bottou, and Y. Bengio, Haffner, Gradient-based learning applied to document recognition, Proc. IEEE **86**, 2278 (1998).

[48] J. Crodelle, D.W. McLaughlin, Idealized model of the developing visual cortex, bioRxiv (2020).

[49] P. Voosen, How AI detectives are cracking open the black box of deep learning, Science (2017).

[50] J. Woo, K. Moon, J. Song, S. Lee, M. Kwak, J. Park, and H. Hwang, Improved synaptic behavior under identical pulses using AlOx/HfO_2 bilayer RRAM array for neuromorphic systems, IEEE Electron Device Lett. **37**, 994 (2016).

[51] H. Mulaosmanovic, E. T. Breyer, T. Mikolajick, and S. Slesazeck, Recovery of cycling endurance failure in ferroelectric FETs by self-heating, IEEE Electron Device Lett. **40**, 216 (2018).

[52] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, Nanoscale memristor device as synapse in neuromorphic systems, Nano Lett. **10**, 1297 (2010).

[53] S. Oh, T. Kim, M. Kwak, J. Song, J. Woo, S. Jeon, I. K. Yoo, and H. Hwang, HfZrOx-based ferroelectric synapse

device with 32 levels of conductance states for neuromorphic applications, IEEE Electron Device Lett. **38**, 732 (2017).

[54] Y. Li, E. J. Fuller, S. Asapu, S. Agarwal, T. Kurita, J. J. Yang, and A. A. Talin, Low-voltage, CMOS-free synaptic memory based on Li_xTiO_2 redox transistors, ACS Appl. Mater. Interfaces **11**, 38982 (2019).

[55] S. Choi, J. Yang, and G. Wang, Emerging memristive artificial synapses and neurons for energy-efficient neuromorphic computing, Adv. Mater. **32**, 2004659 (2020).