Programmable Skyrmion Logic Gates Based on Skyrmion Tunneling

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Magnetic skyrmions are promising candidates as elementary nanoscale bits in logic-in-memory devices, intrinsically merging high-density memory and computing capabilities. Here we exploit the dynamics of skyrmions interacting with anisotropy energy barriers patterned by ion irradiation to design programmable logic gates. Using micromagnetic simulations with experimental parameters, we show that a fine tuning of the barrier height and width allows the selective tunneling of skyrmions between parallel nanotracks triggered by skyrmion-skyrmion interaction. This can be leveraged to design a skyrmion demultiplexer logic gate that works solely using skyrmions as logic inputs. By cascading and connecting demultiplexer gates with a specific topology, we develop a fully programmable logic gate capable of producing any possible logic output as a sum of all minterms generated by a given set of inputs without requiring any complex additional electric or magnetic interconversion. The proposed design is fully conservative and cascadable, enabling purely skyrmion-based logic-in-memory devices.

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I. INTRODUCTION

The information technology industry is currently facing major challenges related to power dissipation and energy consumption [1,2]. The conventional Moore's approach of CMOS technology is currently out of breadth: the continuously decreasing size of the MOS transistors in the logic and memory units leads to critical power dissipation and energy consumption issues. Another major bottleneck relates to the Von Neumann architecture, in which the constant transfer of data between the memory and computing units leads to a considerable cost in energy and limited bandwidth. In addition, since the current technologies use volatile on-chip memory modules, the static power consumption used to maintain the stored data is significant even if state-of-the-art low-power strategies are used. Recently, logic-in-memory architectures, merging nonvolatile memories and logic circuits, have attracted increased attention, as they are expected to realize ultralow power, higher bandwidth, and shorter interconnection delays. Such an architecture opens the way for "normally off" and "instant-on" computing with no "standby power" and wider memory bandwidth. This has led to the search for technologies that combine memory and computing capabilities in the same device.

Topological spin textures named magnetic skyrmions [3,4] have emerged recently as a promising candidate to act as the building blocks of logic-in-memory technologies that intrinsically merge high-density nonvolatile storage memories and logic operations. Magnetic skyrmions are local whirling of the magnetization. Their nanometric scale, topological protection, mutual repulsion, fast and low-power manipulation can be exploited to code data and perform computation at the nanoscale. Different types of logic devices based on skyrmions have been proposed in recent years [5–13]. The primary physical phenomenon driving these devices is the mutual repulsion of skyrmions resulting from the dipolar and exchange interactions. Skyrmions are also very sensitive to local variations of the magnetic properties, which can be exploited to design local potential wells that guide the skyrmion trajectory in logic circuits [14–30].

As the anisotropy can be modulated using a gate electric field, programmable skyrmion switches and routers controlled by gate voltage have been proposed, which can be utilized to perform Boolean logic as well as neuromorphic and stochastic computing [12,31]. However, such an approach is plagued by the need for densely packed gates with bulky electrical circuitries and multiple voltage-to-skyrmion signal interconversion stages, resulting in a prohibitively large energy and footprint cost.

A more promising approach lies in a local modulation of the magnetic parameters through engineering of the material. In particular, light He^+ ion irradiation is a powerful tool to tailor the magnetic properties of ultrathin films, via a gentle intermixing of the interfaces [32]. In ultrathin Pt/Co/MgO films, we have shown that it leads to a decrease of the magnetic anisotropy and Dzyaloshinkii-Moriya interaction [14]. This can be exploited to create

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and guide skyrmions in racetracks defined by ion irradiation, which acts as local potential wells for the skyrmions [14].

In this work, we investigate the interactions of skyrmions with anisotropy energy barriers and show that a fine tuning of the barrier height and width allows the selective tunneling of skyrmions between parallel nanotracks triggered by skyrmion-skyrmion interaction. This can be leveraged to design a skyrmion demultiplexer (dmux) logic gate that works solely using skyrmions as logic inputs. By cascading three demultiplexer logic gates, a fully programmable logic gate is proposed that allows the realization of any desired logic output from a set of given inputs. The developed logic design is fully conservative, i.e., no skyrmion is destroyed during the process and all skyrmions can be recovered at the end of the logic operation, which makes it suitable for conservative reversible logic. This also removes the need for continuous generation of skyrmions that is an energy expensive process. The developed logic design can significantly reduce the number of elementary logic operations required to perform complex arithmetic computations. Moreover, the proposed implementation also provides a modular design template for creating large-scale logic networks by repurposing dmux gates.

II. RESULTS AND DISCUSSION

A. Skyrmion dynamics in the presence of an energy barrier

In this section, we establish a basic understanding of the dynamics of a single skyrmion interacting with an energy barrier created by a sudden change in anisotropy and DMI induced by He^+ ion irradiation. We perform micromagnetic simulations with magnetic and transport parameters consistent with our prior experimental work (see Appendix A for details regarding the micromagnetic model and parameters) [14].

We consider an ultrathin film with a single skyrmion moving under the influence of spin-orbit torque (SOT). An energy barrier of width W and height ΔB_K is present in the system, located at $y = 0$. The barrier height ΔB_K is defined as the difference between the values of the effective anisotropy field of the barrier (nonirradiated) and the outer (irradiated) region, $\Delta B_K = B_{K,\mathrm{nonirr}} - B_{K,\mathrm{irr}}$. The skyrmion moves along an oblique direction at an angle of about 68° (skyrmion Hall angle) with the x axis due to the current flowing along the $+x$ direction (current density, $J = 5 \times 10^{10}$ A/m^2). Figure 1(a) shows the trajectories of the skyrmion for different values of the barrier height ΔB_K but with a fixed barrier width of $W = 12$ nm. The anisotropy of the outer region is fixed at $B_{K,\mathrm{irr}} = 7$ mT. We find that, for low ΔB_K, the skyrmion can pass through the energy barrier, while for large enough ΔB_K, the skyrmion does not pass through the barrier and eventually moves along the barrier (see $\Delta B_K = 65$ mT). Interestingly, when the skyrmion passes through the barrier, we observe that the trajectories are shifted along the x direction, with the magnitude of this shift being dependent on the value of ΔB_K. Similar behavior was also observed for skyrmions crossing energy steps [34,35]. The possibility of crossing the barrier also depends on the barrier width W. We show in Fig. 1(b) the trajectories of skyrmions for different W with a fixed barrier height of $\Delta B_K = 65$ mT. For low width ($W = 6$ nm), the skyrmion easily crosses the barrier, while for all other cases ($W = 12, 18$, and 24 nm), the skyrmion is blocked and moves along the barrier (see Video SV1 [33] within the Supplemental Material). Physically, this can be understood by considering the fact that, in the case of a narrow barrier, only a small portion of the

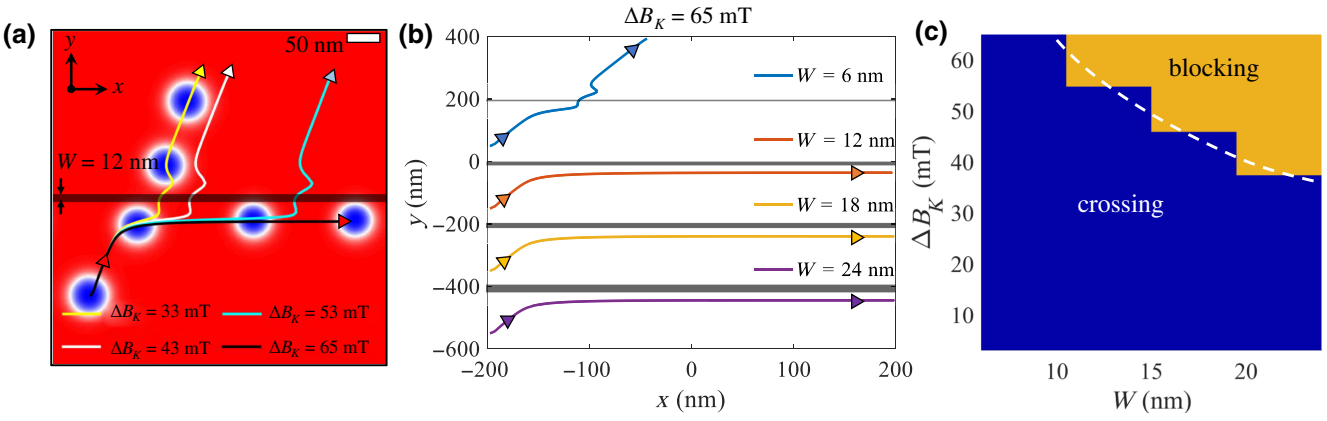

FIG. 1. (a) Trajectory of a skyrmion crossing an energy barrier created by a sharp change in anisotropy for different values of anisotropy difference ΔB_K at fixed barrier width $W = 12$ nm and injected current density of $J = 5 \times 10^{10}$ A/m^2. The total size of the system is 512×512 nm^2. (b) Trajectory of a skyrmion for different widths of the barrier, W, at a fixed $\Delta B_K = 65$ mT and current density $J = 5 \times 10^{10}$ A/m^2. (c) The ΔB_K-W map for $J = 5 \times 10^{10}$ A/m^2 indicating the set of parameter values for which the skyrmion can cross the barrier or is blocked by it. The dashed line is a guide to the eye, indicating the boundary between both regions.

skyrmion falls inside the energetically unfavorable barrier region during the crossing from the lower to the upper region. Thus, the energy increase due to the skyrmion moving inside the nonirradiated region is not very high and can be overcome by the force due to the skyrmion Hall effect. We perform similar simulations for a range of ΔB_K and W and present a corresponding map in Fig. 1(c) depicting the set of $\Delta B_K - W$ values for which the skyrmion can either cross the barrier (low ΔB_K and W) or be blocked by it (high ΔB_K and W). The boundary between both regimes depends on the injected current: for a higher value of the current density, we expect the boundary to shift toward higher ΔB_K and W, as the skyrmion has more energy to cross the energy barrier.

B. Skyrmion motion inside irradiated nanotracks

The possibility for a skyrmion to cross an energy barrier or not depending on the barrier parameters can be exploited to guide and control the skyrmion trajectory in tracks defined by ion irradiation. Figures 2(a) and 2(b) show the trajectory of a skyrmion in a nanotrack with lower anisotropy driven by a current density of $J = 5 \times 10^{10}$ A/m^2 and $J = 11 \times 10^{10}$ A/m^2, respectively. For a fixed ΔB_K, there exists a threshold current density beyond which the skyrmion cannot be confined inside the track. For our simulation parameters, a threshold $J_{\text{th}} = 10 \times 10^{10}$ A/m^2 is found. In the following, we use a current density of 5×10^{10} A/m^2 that is half of this threshold, such that the skyrmion stays confined in the track.

Next, we consider the motion of skyrmions in parallel nanotracks. To minimize the area of the device that is critical for energy consumption, it is necessary to densely pack many tracks. In Figs. 2(c) and 2(d), we show the motion of a skyrmion in two parallel tracks separated by a barrier of width $W = 12$ nm and $W = 6$ nm, respectively, for a current density of $J = 5 \times 10^{10}$ A/m^2. The results are similar to Fig. 1(b), indicating that there is a minimum barrier width (W_0) that has to be maintained to ensure that the skyrmion stays confined in the track. For our parameters, this minimum barrier width is $W_0 = 10$ nm. For the simulations in the subsequent sections, we maintain a gap width $W = 12$ nm that is larger than W_0. We note here that the state-of-the-art focused ion beam systems can easily produce sub-10 nm features using He^+ ions [36].

The crossing between parallel tracks can also be controlled by adding an additional channel of finite width between the two tracks [see Figs. 2(e) and 2(f)]. This channel has the same magnetic parameters as that of the irradiated nanotracks and it works as a tunnel between the upper and the lower tracks. For a channel width of 6 nm [Fig. 2(e)], we find that the trajectory of the skyrmion is unaffected. However, for a channel width of 12 nm [Fig. 2(f)], the skyrmion can enter the upper track after traversing through the channel. Thus, even though the channel width for Fig. 2(f) is nearly 5 times lower than the skyrmion diameter, it is still enough for the skyrmion to pass through. A similar situation in a physically milled nanotrack may not be achieved as the skyrmion would have to compress significantly to move through the channel during which it may be destroyed. This absence of any physical discontinuity in the system is an important feature of our simulations, preventing undesired destruction of the skyrmion at physical edges.

C. Skyrmion-based demultiplexer

The concepts of skyrmion movement within and passing between parallel nanotracks can be exploited to design a skyrmion-based dmux logic gate. A dmux gate is a logic gate that connects an incoming signal to one of the multiple

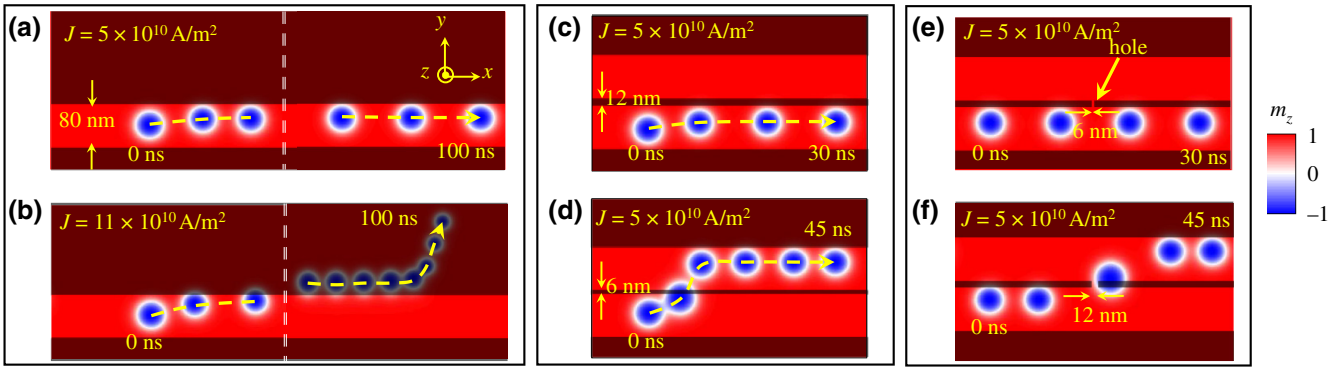

FIG. 2. Skyrmion motion in an 80-nm-wide nanotrack for current density (a) $J = 5 \times 10^{10}$ A/m^2 and (b) $J = 11 \times 10^{10}$ A/m^2. The dashed white lines on the track represent a discontinuity along the x scale that we use to show the motion for a longer timescale ($t = 0$–100 ns). The skyrmion has a diameter of about 57 nm. Skyrmion motion in two parallel nanotracks separated by a nonirradiated barrier region of width (c) $W = 12$ nm and (d) $W = 6$ nm, for a fixed current density of $J = 5 \times 10^{10}$ A/m^2. Skyrmion motion in two parallel nanotracks separated by a barrier region of width $W = 12$ nm, having an interconnecting channel of width (e) 6 nm and (f) 12 nm at the center of the barrier. Movies corresponding to cases (a)–(f) are shown in Video SV2 within the Supplemental Material [33].

output streams based on the value of the *selector* input. We here discuss a 1-to-2 dmux that takes a single *selector* (X_1) input ("0" or "1") and connects the incoming signal (G) to one of the two outputs (O_1 or O_2) [see Figs. 3(a) and 3(b)] In our device, the input "1" is represented by a single skyrmion, while the absence of a skyrmion will correspond to input "0." Two different dmux gate designs are presented, both of which are based on skyrmions moving inside parallel nanotracks but differ in their working principle. These two different dmux gates can be connected to build programmable logic gates, as will be shown later in Sec. II D.

1. Demultiplexer: type A

Figures 3(c) and 3(d) show the working principle of our first dmux gate design, named dmux *type A*. The width of each track is 80 nm with a barrier width $W = 12$ nm separating each track. The incoming skyrmion enters the system from the left-hand side of the T_1 track ("G" input) while the selector input (X_1) is in the T_0 track. A uniform dc current along the $\hat{x}$ direction ($J = 5 \times 10^{10}$ A/m^2) moves the skyrmion with a positive velocity v_x in the $\hat{x}$ direction as discussed previously. For the case where the selector input "X_1" is "0" [Fig. 3(c)], i.e., there is no skyrmion in the T_0 track, the skyrmion input "G" moves along the T_1 track, leading to the output $O_1 = 1$. The output O_2 remains "0" as no skyrmion is present in the corresponding track. Figure 3(d) shows the operation of dmux if the selector input is "1," i.e., a skyrmion is present in the T_0 track. This skyrmion in track T_0 cannot move along the $+x$ direction during the current injection as it is blocked by the energy barrier. When the skyrmion in track T_1 gets closer to the skyrmion in track T_0, which remains almost fixed due to the barrier, it experiences a repulsive force due to the skyrmion-skyrmion interaction. This repulsive force enhances the transverse force already acting on the skyrmion in track T_1 due to the skyrmion Hall effect. The resulting force is enough to push the moving skyrmion through the barrier between tracks T_1 and T_2, and this skyrmion ends its trajectory at output O_2. From the results in Figs. 3(c) and 3(d), we conclude that the overall functionality of dmux is achieved: the incoming skyrmion from the left of the T_1 track ("G") is guided to either the output O_1 or the output O_2 depending upon the presence of a skyrmion in the T_0 track (*selector* input). The outputs can be expressed as $O_1 = \overline{X_1}$ and $O_2 = X_1$ (for $G = 1$).

2. Demultiplexer: type B

In the design of dmux type A, the track for the *selector* input X_1 is below the track for the "G" input. In our programmable logic gate design, we also require a dmux gate in which the moving skyrmion ("G" input) is below the *selector* input (X_1). The principle of this dmux *type-B* design functionality is shown in Figs. 3(e) and 3(f). Similar to our previous design, we use irradiated tracks to confine the skyrmion; however, we remove track T_0 where the input X_1 was kept in dmux type A. Instead, we divide track T_2 into two parts by adding a vertical barrier of width $W = 12$ nm in the middle of the T_2 track. The input X_1 is now sent from the left of track T_2. Additionally, we

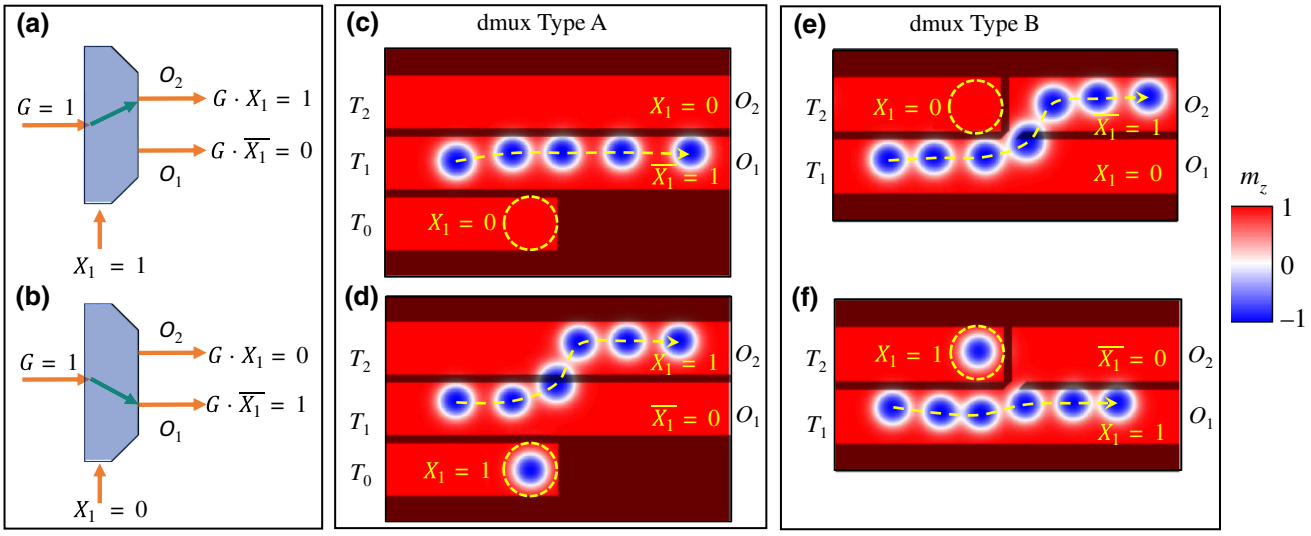

FIG. 3. Panels (a) and (b) show the schematic and operation of a 1-to-2 dmux gate that produces a 0(1) output at O_1 and a 1(0) output at O_2 if the selector input is $X_1 = 1(0)$. The input "G" is assumed to be fixed at "1." Panels (c) and (d) show the micromagnetic simulation of a skyrmion-based dmux gate where the incoming signal "G" is a skyrmion in track T_1. The selector input is a skyrmion (or no skyrmion) in track T_0. The current density is $J = 5 \times 10^{10}$ A/m^2. Panels (e) and (f) show the micromagnetic simulations of a different design implementation of skyrmion-based dmux with an additional channel in the barrier. For this case, the track for selector input is above the "G" input. Movies corresponding to (c)–(f) are shown in Video SV3 [33] within the Supplemental Material.

connect track T_1 with the right part of T_2 by introducing a small channel in the barrier, which allows a skyrmion moving in track T_1 to pass to track T_2. In Fig. 3(e), the incoming skyrmion enters from the left of the T_1 track and moves along the $+x$ direction. If there is no skyrmion in the upper track ($X_1 = 0$), the skyrmion will move towards the upper track T_2, tunneling through the interconnecting channel and will arrive at output O_2. However, if track T_2 has a skyrmion ($X_1 = 1$) [Fig. 3(f)], the skyrmion in track T_1 moves straight to the right end towards output O_1 due to the mutual repulsive force. Overall, as in the previous case, the dmux logic here is achieved as the skyrmion is guided to the right side at either output O_1 or output O_2 depending on the selector input (X_1). The output of dmux type B can be expressed as $O_1 = X_1$ and $O_2 = \overline{X_1}$ (for $G = 1$).

D. Programmable logic gate design using demultiplexers

Demultiplexers are extremely useful logic gates and can be connected in several different ways to perform a variety of logic operations. Such an implementation was discussed in Ref. [37] to achieve a programmable logic gate based on three dmux gates that can produce many logical combinations of the two input signals [see Fig. 4(a)]. For clarity, we split the entire operation into two stages. *Stage 1* involves two input bits X_1 and X_2 that are passed as selection inputs for different dmux gates. The operation flow is as follows. Input bit X_1 is passed to the first dmux gate (dmux1) that outputs X_1 and $\overline{X_1}$ for an incoming signal $G = 1$ (fixed and constant). The outputs of dmux1 act as the "G" input for the next gates dmux2 and dmux3. The selection input of both these gates is set using X_2. In the end, we obtain all four possible minterms with X_1 and X_2, namely $X_1.\overline{X_2}$, $X_1.X_2$, $\overline{X_1}.\overline{X_2}$, and $\overline{X_1}.X_2$ ("$\cdot$" represents logical AND operation).

In *stage 2*, switch gates $[a, b, c, d = (0, 1)]$ are used on each of the four output bits coming from dmux2 and dmux3 that are then added to obtain the final output: $Y = a(X_1.\overline{X_2}) + b(X_1.X_2) + c(\overline{X_1}.\overline{X_2}) + d(\overline{X_1}.X_2)$. By setting the $[a, b, c, d]$ values, any logical operation on X_1 and X_2 can be achieved.

Designing this programmable gate with skyrmion-based dmux gates involves that (i) the input X_2 (a skyrmion) must be conserved (stored) or duplicated and pass through both dmux2 and dmux3 gates and (ii) the output of the first dmux gate has to reach the input of the next dmux gate (cascading) without altering its value. We first focus on *stage 1* of this logic circuit and propose a design in Fig. 4(b), which is based on the previously described dmux type-A and type-B gates. The tracks in dmux2 and dmux3 that carry the selection input (track T_2) are merged to avoid the need for duplication of input X_2. This is possible only if we use the type-A design for dmux2 and type-B design for dmux3, as shown in Fig. 4(b). This merging also reduces the total number of required tracks, reducing the total area of the device, which further minimizes the energy consumption for the operation.

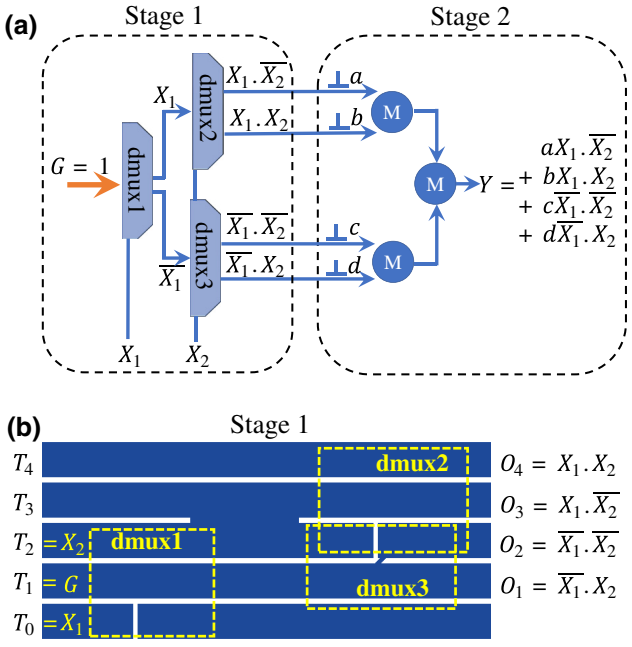

FIG. 4. (a) Schematic of a programmable logic gate design utilizing three dmux gates. (b) The design of programmable logic (stage 1) using two dmux type-A logic gates (dmux1 and dmux2) and one dmux type-B logic gate (dmux3).

1. Performing logic operations (stage 1)

Figure 5 shows the operation of our programmable logic gate design proposed in Fig. 4(b) using micromagnetic simulations. Here, we assume that the inputs X_1 and X_2 are already correctly placed in tracks T_0 and T_2 at their respective positions. The exact protocol to place these inputs is discussed in Appendix B. For the case of $X_1 = 1$ and $X_2 = 0$ [Fig. 5(a)], the skyrmion input "G" enters through track T_1 and is pushed to track T_2 due to the repulsion from the skyrmion in track T_0 (input X_1). The skyrmion then passes through the large opening in the barrier into track T_3. In track T_3, the skyrmion keeps moving straight (along the $+x$ direction) and is obtained at the output end O_3. For the case of $X_1 = 0$ and $X_2 = 1$ [Fig. 5(b)], the skyrmion enters through track T_1 and initially moves straight without facing any repulsion (as input X_1 is "0"). The skyrmion then experiences repulsion from the skyrmion in track T_2 (input X_2). Because of this repulsion, the moving skyrmion cannot tunnel through the channel between tracks T_1 and T_2 and is forced to move in the same track T_1, to finally exit through the output end O_1. For inputs $X_1 = 1$ and $X_2 = 1$ [Fig. 5(c)], the input skyrmion "G" follows the same pattern as in Fig. 5(a) till it reaches track T_3. While moving in track T_3, it is repelled from the skyrmion input X_2 lying in

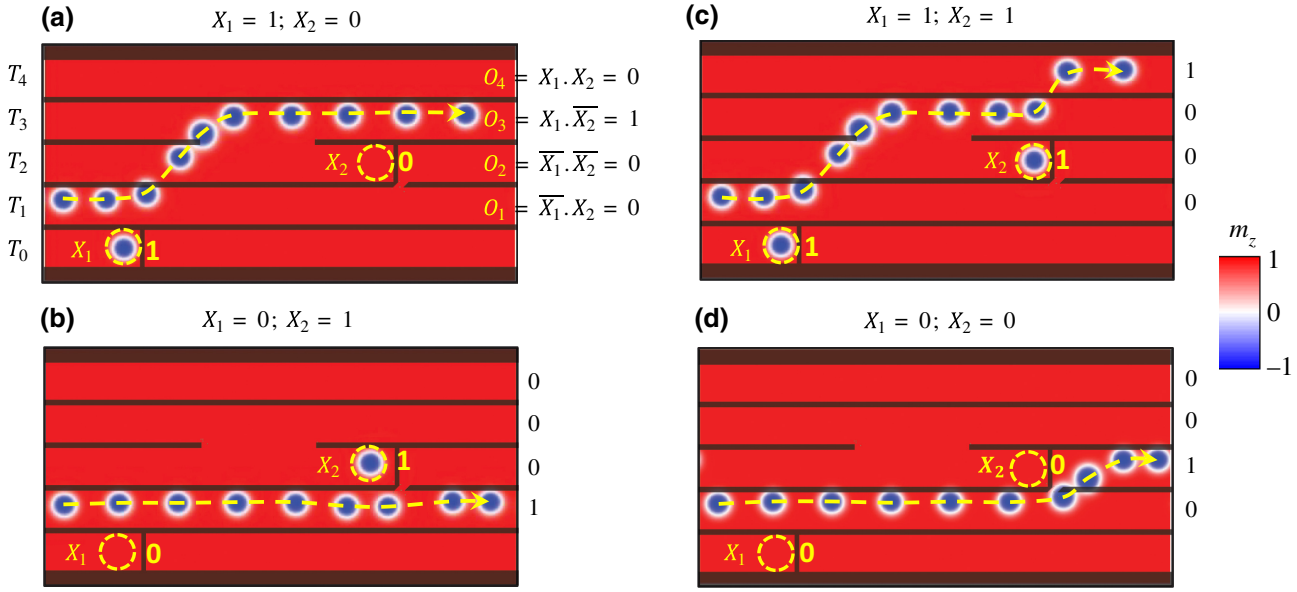

FIG. 5. Micromagnetic simulation of the programmable logic stage 1, showing the trajectory of the skyrmion for various input cases. Depending on the inputs X_1 and X_2, the skyrmion "G" entering through track T_1 reaches one of the outputs O_1–O_4. Note that, for each set of inputs X_1 and X_2, only one of the output tracks (O_1–O_4) has a skyrmion ("1") and the rest are "0."

track T_2 that pushes it to the uppermost track T_4, i.e., output O_4 (see also Video SV4 [33] within the Supplemental Material). Lastly, for the case of $X_1 = 0$ and $X_2 = 0$, the input skyrmion "G" in track T_1 moves straight along the track till it reaches the interconnecting channel between tracks T_1 and T_2. After tunneling through the channel to the T_2 track, the skyrmion then reaches the O_2 output. Using the previous expressions for type-A and type-B dmux gates, we can write the mathematical notation for each of the output gates $O_1 - O_4$ as $O_1 = (\overline{X_1}.X_2)$, $O_2 = (\overline{X_1}.\overline{X_2})$, $O_3 = (X_1.\overline{X_2})$, and $O_4 = (X_1.X_2)$. These outputs can now be combined in the stage-2 operation of the logic circuit for obtaining the desired operation, as discussed in the next section.

2. Combining outputs (stage 2)

Stage 2 of Fig. 4(a) involves passing the four outputs from stage 1 through an *on-off* gate and combining them afterward. These *on-off* gates can simply be constructed as tracks with or without an energy barrier in the track that prevents or allows the skyrmion to pass. Note that the programmability in this design is limited to modifying the tracks to obtain any desired logic functionality that is known at the time of device fabrication. However, a dynamically reconfigurable design can also be achieved by replacing these barriers with voltage-controlled gates that can modify the magnetic anisotropy locally and can thus reconfigure the logic functionality even after fabrication. The output obtained after each of these gates is finally merged to obtain the final output Y. This merging is relatively easy to implement in our design by simply adding another track at an angle to the parallel tracks, combining all four output tracks (O_1–O_4). For faster skyrmion motion, the angle between the new track and the four parallel tracks is kept at 68°, which is the same as the skyrmion Hall angle. The full design is shown in Fig. 6(a) where the regions G_a–G_d represent the gates and the final output Y is obtained from the uppermost track. It may be noted here that, for any combination of inputs X_1 and X_2, only one of the outputs O_1–O_4 contains a skyrmion ("1") and the rest are empty ("0"). Therefore, there is no possibility of multiple skyrmions arriving from two different tracks and interacting with each other during the merging operation through the nonparallel track.

To demonstrate the working principle of this design using micromagnetic simulations, we use the expression for the XOR gate as an example of our desired output. Other logic functionalities can also be obtained by changing the values of parameters $[a, b, c, d]$ as given in Table I. The XOR gate is mathematically represented as $Y = X_1.\overline{X_2} + \overline{X_1}.X_2$. To implement the XOR logic operation, only the gates G_a and G_c work as energy barriers (nonirradiated regions) in tracks corresponding to O_4 and O_2. The micromagnetic simulations for all four combinations of inputs X_1 and X_2 are shown in Figs. 6(b)–6(e). For the cases $X_1 = 1$, $X_2 = 0$ [Fig. 6(b)] and $X_1 = 0$, $X_2 = 1$ [Fig. 6(c); see also Video SV5 [33] within the Supplemental Material], the output skyrmion of stage 1 proceeds to the uppermost output track, giving the final output $Y = 1$. For the cases of $X_1 = 1, X_2 = 1$ [Fig. 6(d)] and $X_1 = 0, X_2 = 0$ [Fig. 6(e)], the output from stage 1 is received in O_4

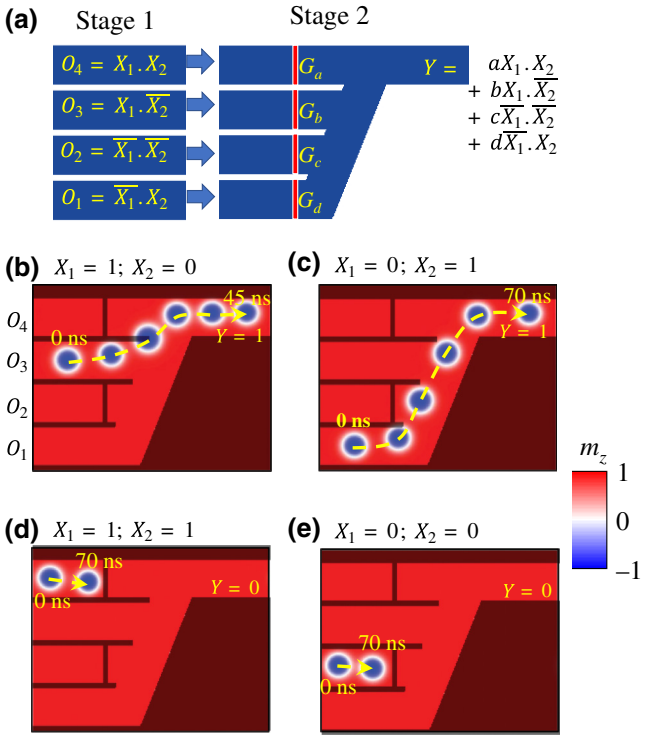

FIG. 6. (a) Schematic of the stage-2 design of the programmable logic gate shown in Fig. 4(a) using irradiated nanotracks. The inputs of stage 2 are the outputs from the stage-1 operation shown in Fig. 5. Gates G_a–G_d control the final output Y. Panels (b)–(e) show the micromagnetic simulations of the stage-2 operation in programmable logic for achieving the output of a XOR gate for different input cases. Gates G_a and G_c are used (nonirradiated regions) to perform the required logic operation: $Y = X_1.\overline{X_2} + \overline{X_1}.X_2$.

and O_2, respectively, both of which are blocked by the energy barriers. Thus, the final output for both these cases is $Y = 0$.

3. Operational characteristics

For the material parameters and dimensions used in the micromagnetic simulations, the operation time for the designed gate varies from 76–120 ns for stage 1 and 45–70 ns for stage 2 with a current of 0.1 mA that corresponds to a maximum energy dissipation of 238 fJ (stage 1 plus stage 2) by Joule heating. Note that the magnetic and transport parameters of the material stacks are extracted from proof-of-concept experiments, which are not designed for logic gate implementations. Faster operations with lower energy can be easily achieved by designing the logic gates with magnetic materials with lower damping, larger spin-orbit torques, higher anisotropy in the nonirradiated track, and lower device dimensions. For instance, by considering materials with 10 nm skyrmions, a magnetic damping of 0.05, and assuming that the lateral dimensions decreased by a factor 5 due to smaller skyrmion size, a total operation time of 6.3 ns with a current of 20 μA and an energy dissipation of 0.32 fJ is anticipated for $J = 5 \times 10^{10}$ A/m^2. Note that these values do not include the delay and energy dissipated in the addressing transistors and contact lines. These figures should be compared with the energy dissipation and delay in interconnects for the data to reach the CMOS logic in a conventional Von Neumann architecture, which is typically of the order of the picojoule for a 1 mm interconnect, combined with the write time in SRAM cache memory, around the nanosecond. Thus, we expect a drastic decrease in the energy consumption as compared to a standard Von Neumann architecture.

TABLE I. Values of parameters (a, b, c, d) for obtaining different logic operations. The output is represented by $Y = a(X_1.X_2) + b(X_1.\overline{X_2}) + c(\overline{X_1}.\overline{X_2}) + d(\overline{X_1}.X_2)$.

Logic gate	a	b	c	d
AND	1	0	0	0
OR	1	1	0	1
XOR	0	1	0	1
NAND	0	1	1	1
NOR	0	0	1	0
XNOR	1	0	1	0

III. CONCLUSIONS

To conclude, we have proposed a programmable logic gate design based on skyrmion-skyrmion interactions. The gate exploits the skyrmion guiding and selective crossing of energy barrier designed by local patterning of the magnetic parameters, which can be realized using light ion irradiation. The gate is conservative and cascadable and, since it relies purely on skyrmion interactions, does not require complex electric or magnetic interconversion gates. Since skyrmions can be used at nanoscale to represent elementary bits, the proposed gate could form the basis of logic-in-memory devices that intrinsically merge high-density memory and computing capabilities.

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APPENDIX A: MICROMAGNETIC SIMULATIONS

The simulations are performed in a micromagnetic framework by numerically solving the Landau-Lifshitz-Gilbert (LLG) equation using the open-source MUMAX[3]

package [38]. We consider a stack composed of ferromagnetic (FM) and heavy metal (HM) ultrathin films. Because of the spin-orbit interaction at the FM-HM interface, a spin current flows in the perpendicular ($+\hat{z}$) direction through the FM if a charge current is injected in the in-plane $+\hat{x}$ direction in the HM. The direction of polarization of the electrons $\mathbf{e}_p$ is along the $-\hat{y}$ direction, i.e., orthogonal to the direction of flow of charge current as well as the flow of spin current. We include the additional torque on the FM due to this spin current using the Slonczewski model:

$$\frac{d\mathbf{m}}{dt} = -\gamma(\mathbf{m}\times\mathbf{B}_{\text{eff}}) + \alpha\left(\mathbf{m}\times\frac{d\mathbf{m}}{dt}\right) - \mathcal{T}[\mathbf{m}\times(\mathbf{m}\times\mathbf{e}_p) + \epsilon'(\mathbf{m}\times\mathbf{e}_p)],$$
$$\mathcal{T} = \frac{\hbar\theta_H J}{2|e|M_S d}.$$

Here, $\mathbf{m}$ is the normalized local magnetic moment, γ is the gyromagnetic ratio of the electron, α is the Gilbert damping constant, $\mathcal{T}$ represents the strength of spin-orbit torque, J is the charge current through the HM flowing in the $+\hat{x}$ direction, $|e|$ is the electronic charge, M_S is the saturation magnetization, and d is the thickness of the ferromagnetic film. We use $\theta_H = 0.1$ as the spin Hall angle and $\epsilon' = 0.015$ as the ratio of fieldlike to dampinglike SOT torque. Here $\mathbf{B}_{\text{eff}}$ is the effective field that includes contributions from the external field ($\mathbf{B}_{\text{ext}}$), the magnetostatic interactions ($\mathbf{B}_m$), the exchange interactions ($\mathbf{B}_{\text{exch}}$), the perpendicular magnetic anisotropy ($\mathbf{B}_{\text{an}}$), and Dzyaloshinskii-Moriya interaction ($\mathbf{B}_{\text{DMI}}$).

To achieve realistic predictions, we use the material parameters corresponding to our previous experimental work on skyrmion confinement in He irradiated nanotracks [14] given in Table II with an external field of $\mathbf{B}_{\text{ext}} = 33$ mT $\hat{z}$. Note that we obtain the value of the effective anisotropy field (B_K) from experiments that can be translated to the uniaxial anisotropy constant using the expression $K = B_K M_S/2 + \mu_0 M_S^2/2$. The total area of the simulated system in stage 1 is 1024×512 nm^2 with 0.9 nm FM thickness. The area of stage-2 design is 512×512 nm^2. The resistivity of the HM (Pt in our case) is 30Ω μm from experimental measurements. For solving the LLG equation, we discretize the entire FM into cuboidal cells of $2 \times 2 \times 0.9$ nm^3 and use the fourth-order Runge-Kutta method with an adaptive time step.

TABLE II. Simulation parameters.

Parameter	Irradiated	Nonirradiated
M_S (MA/m)	1.32	1.32
$\mu_0 B_K$ (mT)	7	72
$\lvert D\rvert$ (mJ/m^2)	1.082	1.122
A (pJ/m)	16	16
α	0.3	0.3

APPENDIX B: SETTING AND RECOVERING INPUTS

In order to perform the operations shown in Fig. 5, inputs X_1 and X_2 have to be set at proper positions. We mention below the protocol followed to achieve this. The input skyrmion X_2 is sent through track T_1 at time $t = 0$. The injected current is $J = 5 \times 10^{10}$ A/m^2. The skyrmion then moves along track T_1 to the right. At $t = 40$ ns, we increase the current to $J = 10 \times 10^{10}$ A/m^2 [see Fig. 7(a)]. For this value of the current, the skyrmion can pass through the energy barrier. Hence, the skyrmion moves from track T_1 to track T_2. The current is again reduced back to $J = 5 \times 10^{10}$ A/m^2 at $t = 50$ ns once the skyrmion has already entered track T_2. At this point, the skyrmion corresponding to input X_1 is also injected from the track T_0. After another $t = 30$ ns with $J = 5 \times 10^{10}$ A/m^2, both the inputs are placed at their respective positions. We then proceed to perform the logic operations shown in Fig. 5. Once the operation is finished, to recover the skyrmion, we simply use a current density with negative polarity $J = -5 \times 10^{10}$ A/m^2 for 50 ns. The skyrmion input X_1 is collected back from track T_0 and skyrmion input X_2 can be collected from track T_2. The motion of skyrmion input X_2 during the entire SET and RECOVER cycle is shown in Fig. 7(b).

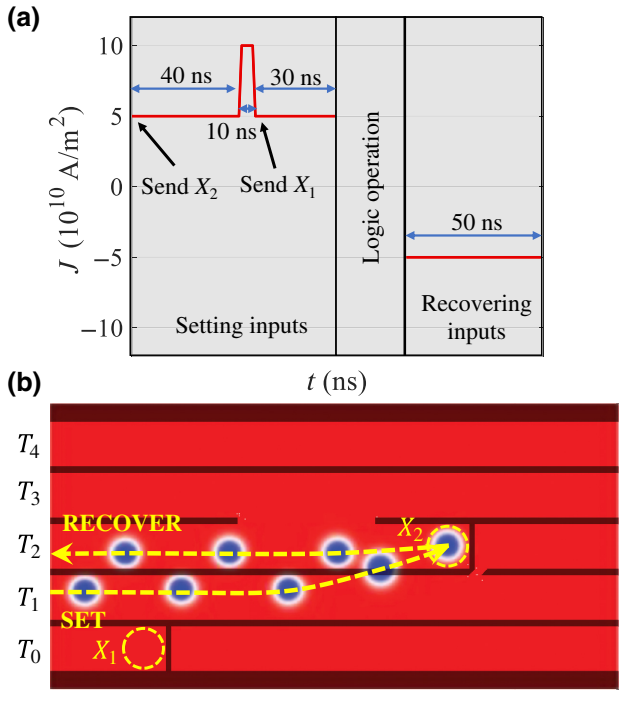

FIG. 7. (a) Set of current pulses used to set the inputs X_1 and X_2 at their corresponding positions. (b) Motion of the skyrmion input X_2 during a full SET and RECOVER cycle.

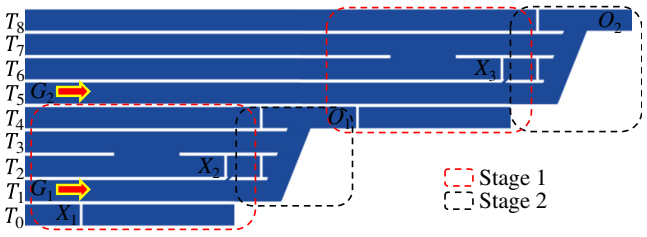

FIG. 8. Schematic of two cascaded logic gates (each with a stage-1 and stage-2 operation) for performing $(X_1 \oplus X_2) \oplus X_3$.

APPENDIX C: SCALABILITY VIA CASCADING

The designed logic gates can be combined to make large-scale networks via cascading. In Fig. 8, we show a schematic of two cascaded logic gates, each having their own stage-1 and stage-2 components. Inputs X_1, X_2, and X_3 will be set by sending them through tracks T_0, T_1, and T_5, respectively. Fixed input G_1 is then sent through track T_1 to perform the first logic operation $(O_1 = X_1 \oplus X_2)$ followed by sending G_2 through track T_5 to perform the second logic operation $(O_2 = O_1 \oplus X_3)$. At the end of the operation, inputs X_1, X_2, X_3 and outputs O_1 (also an input for the second operation), O_2 can be retrieved through tracks T_0, T_2, T_6 and T_1, T_5, respectively, by sending a negative polarity current.

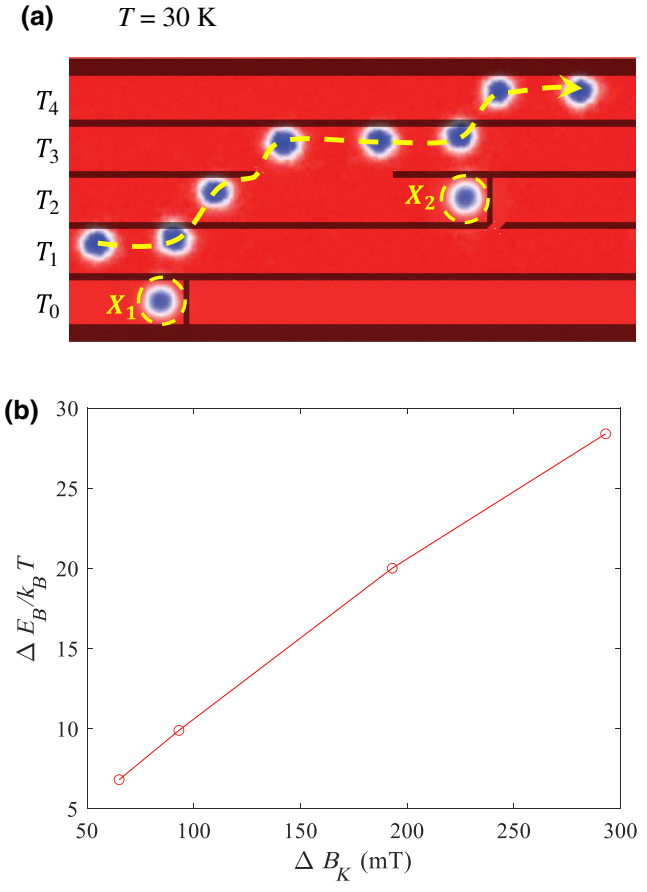

FIG. 9. (a) Micromagnetic simulation of the programmable logic stage 1 at $T = 30$ K showing the trajectory of the skyrmion for inputs $X_1 = 1$ and $X_2 = 1$. (b) Energy barrier as a function of barrier height, ΔB_K.

APPENDIX D: EFFECT OF THERMAL NOISE

In our simulations, we use the material parameters that are experimentally measured at room temperature. Therefore, we automatically account for the effect of finite temperature on material parameters (reduced A, B_K, D, and M_S). Nevertheless, in Fig. 9(a), we show the simulation of stage 1 for inputs $X_1 = 1$ and $X_2 = 1$ with stochastic noise corresponding to $T = 30$ K, obtaining a correct logic operation. Note that the quantitative value of temperature used in these simulations may not correspond to real temperatures due to (i) double calculation of thermal effect due to the use of stochastic noise as well as room-temperature parameters, (ii) limitations of the micromagnetic approach (dependence of the thermal field on simulation cell size), and (iii) the absence of statistical data (ideally several simulation runs with the same parameters but different initial seeds should be performed, but this is computationally prohibitive due to long simulation times).

We also calculate the energy of the skyrmion as a function of position from our micromagnetic model. For the parameters used in the main text ($W = 12$ nm and $\Delta B_K = 65$ mT), we obtain a barrier energy of about $7k_BT$. Assuming an attempt frequency of 1 GHz, the retention time of the skyrmion is about 1 μs, which is about 5 times the operation time for the designed logic gate. Moreover, the energy barrier and the retention time can be easily enhanced by increasing ΔB_K, as shown in Fig. 9(b).

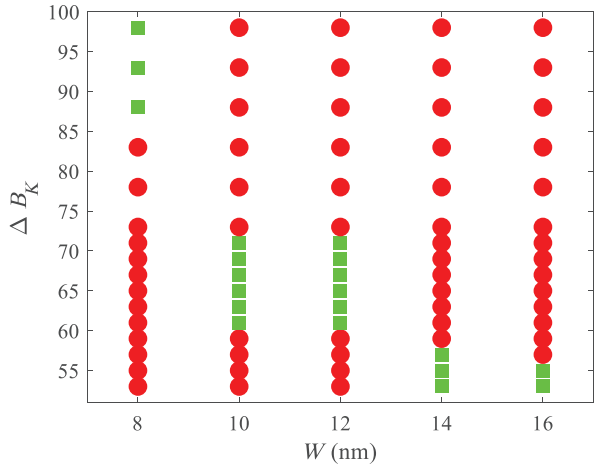

FIG. 10. Map showing the values of barrier widths W and heights ΔB_K for which a correct (green squares) or incorrect (red circles) logic output is obtained for dmux type A.

APPENDIX E: TOLERANCE WITH RESPECT TO THE VARIATION OF W AND ΔB_K

We carried out simulations for the dmux type-A logic gate for varying barrier widths W and heights ΔB_K. The obtained results are shown in Fig. 10. The green squares and red circles represent a correct and incorrect logic operation, respectively. In general, the dmux type-A logic gate works for a range of W and ΔB_K values. For fixed $W =$ 12 nm, the logic operation is correctly performed in the range $\Delta B_K = 61$–71 mT, allowing about 15% of variation in ΔB_K. Higher (lower) barrier widths can also be used to design the logic gate, provided that the barrier height is decreased (increased) accordingly.

[1] T. N. Theis and H.-S. P. Wong, The end of Moore's law: A new beginning for information technology, Comput. Sci. Eng. **19**, 41 (2017).

[2] V. Zhirnov, R. Cavin, J. Hutchby, and G. Bourianoff, Limits to binary logic switch scaling - a gedanken model, Proc. IEEE **91**, 1934 (2003).

[3] N. Nagaosa and Y. Tokura, Topological properties and dynamics of magnetic skyrmions, Nat. Nanotech. **8**, 899 (2013).

[4] A. Fert, N. Reyren, and V. Cros, Magnetic skyrmions: Advances in physics and potential applications, Nat. Rev. Mater. **2**, 17031 (2017).

[5] X. Zhang, M. Ezawa, and Y. Zhou, Magnetic skyrmion logic gates: Conversion, duplication and merging of skyrmions, Sci. Rep. **5**, 1 (2015).

[6] X. Xing, P. W. Pong, and Y. Zhou, Skyrmion domain wall collision and domain wall-gated skyrmion logic, Phys. Rev. B **94**, 054408 (2016).

[7] Z. He, S. Angizi, and D. Fan, Current-induced dynamics of multiple skyrmions with domain-wall pair and skyrmion-based majority gate design, IEEE Magn. Lett. **8**, 1 (2017).

[8] S. Luo, M. Song, X. Li, Y. Zhang, J. Hong, X. Yang, X. Zou, N. Xu, and L. You, Reconfigurable skyrmion logic gates, Nano Lett. **18**, 1180 (2018).

[9] Z. Zhang, Y. Zhu, Y. Zhang, K. Zhang, J. Nan, Z. Zheng, Y. Zhang, and W. Zhao, Skyrmion-based ultra-low power electric-field-controlled reconfigurable (super) logic gate, IEEE Electron Device Lett. **40**, 1984 (2019).

[10] M. Chauwin, X. Hu, F. Garcia-Sanchez, N. Betrabet, A. Paler, C. Moutafis, and J. S. Friedman, Skyrmion logic system for large-scale reversible computation, Phys. Rev. Appl. **12**, 064053 (2019).

[11] M. Song, M. G. Park, S. Ko, S. K. Jang, M. Je, and K.-J. Kim, Logic device based on skyrmion annihilation, IEEE Trans. Electron Devices **68**, 1939 (2021).

[12] H. Zhang, D. Zhu, W. Kang, Y. Zhang, and W. Zhao, Stochastic Computing Implemented by Skyrmionic Logic Devices, Phys. Rev. Appl. **13**, 054049 (2020).

[13] L. Gnoli, F. Riente, M. Vacca, M. Ruo Roch, and M. Graziano, Skyrmion logic-in-memory architecture for maximum/minimum search, Electronics **10**, 155 (2021).

[14] R. Juge, K. Bairagi, K. G. Rana, J. Vogel, M. Sall, D. Mailly, V. T. Pham, Q. Zhang, N. Sisodia, and M. Foerster *et al.*, Helium ions put magnetic skyrmions on the track, Nano Lett. **21**, 2989 (2021).

[15] M. Song, K.-W. Moon, S. Yang, C. Hwang, and K.-J. Kim, Guiding of dynamic skyrmions using chiral magnetic domain wall, Appl. Phys. Express **13**, 063002 (2020).

[16] I. Purnama, W. L. Gan, D. W. Wong, and W. S. Lew, Guided current-induced skyrmion motion in 1D potential well, Sci. Rep. **5**, 10620 (2015).

[17] P. Lai, G. P. Zhao, H. Tang, N. Ran, S. Q. Wu, J. Xia, X. Zhang, and Y. Zhou, An improved racetrack structure for transporting a skyrmion, Sci. Rep. **7**, 45330 (2017).

[18] H. T. Fook, W. L. Gan, I. Purnama, and W. S. Lew, Mitigation of Magnus force in current-induced skyrmion dynamics, IEEE Trans. Magn. **51**, 1 (2015).

[19] D. Toscano, J. P. A. Mendonça, A. L. S. Miranda, C. I. L. de Araujo, F. Sato, P. Z. Coura, and S. A. Leonel, Suppression of the skyrmion Hall effect in planar nanomagnets by the magnetic properties engineering: Skyrmion transport on nanotracks with magnetic strips, J. Magn. Magn. Mater. **504**, 166655 (2020).

[20] S. Bhatti and S. N. Piramanayagam, Effect of Dzyaloshinskii–Moriya interaction energy confinement on current-driven dynamics of skyrmions, Phys. Status Solidi (rrl) **13**, 1900090 (2019).

[21] R. P. Loreto, X. Zhang, Y. Zhou, M. Ezawa, X. Liu, and C. I. L. de Araujo, Manipulation of magnetic skyrmions in a locally modified synthetic antiferromagnetic racetrack, J. Magn. Magn. Mater. **482**, 155 (2019).

[22] C. C. I. Ang, W. Gan, and W. S. Lew, Bilayer skyrmion dynamics on a magnetic anisotropy gradient, New J. Phys. **21**, 043006 (2019).

[23] J. Iwasaki, W. Koshibae, and N. Nagaosa, Colossal spin transfer torque effect on skyrmion along the edge, Nano Lett. **14**, 4432 (2014).

[24] P. Lai, G. P. Zhao, F. J. Morvan, S. Q. Wu, and N. Ran, Motion of skyrmions in well-separated two-lane racetracks, SPIN **07**, 1740006 (2017).

[25] X. Zhang, G. P. Zhao, H. Fangohr, J. P. Liu, W. X. Xia, J. Xia, and F. J. Morvan, Skyrmion-skyrmion and skyrmion-edge repulsions in skyrmion-based racetrack memory, Sci. Rep. **5**, 7643 (2015).

[26] Z. Yan, Y. Liu, Y. Guang, J. Feng, R. Lake, G. Yu, and X. Han, Robust Skyrmion Shift Device Through Engineering the Local Exchange-Bias Field, Phys. Rev. Appl. **14**, 044008 (2020).

[27] C. C. I. Ang, W. Gan, G. D. H. Wong, and W. S. Lew, Electrical Control of Skyrmion Density via Skyrmion-Stripe Transformation, Phys. Rev. Appl. **14**, 054048 (2020).

[28] M. V. Sapozhnikov, S. N. Vdovichev, O. L. Ermolaeva, N. S. Gusev, A. A. Fraerman, S. A. Gusev, and Y. V. Petrov, Artificial dense lattice of magnetic bubbles, Appl. Phys. Lett. **109**, 042406 (2016).

[29] D. Toscano, S. A. Leonel, P. Z. Coura, and F. Sato, Building traps for skyrmions by the incorporation of magnetic defects into nanomagnets: Pinning and scattering traps by magnetic properties engineering, J. Magn. Magn. Mater. **480**, 171 (2019).

[30] M. V. Sapozhnikov, O. V. Ermolaeva, E. V. Skorokhodov, N. S. Gusev, and M. N. Drozdov, Magnetic skyrmions in thickness-modulated films, Jetp Lett. **107**, 364 (2018).

[31] D. Pinna, F. Abreu Araujo, J.-V. Kim, V. Cros, D. Querlioz, P. Bessiere, J. Droulez, and J. Grollier, Skyrmion Gas Manipulation for Probabilistic Computing, Phys. Rev. Appl. **9**, 064018 (2018).

[32] C. Chappert, H. Bernas, J. Ferré, V. Kottler, J.-P. Jamet, Y. Chen, E. Cambril, T. Devolder, F. Rousseaux, V. Mathet, and H. Launois, Planar patterned magnetic media obtained by ion irradiation, Science **280**, 1919 (1998).

[33] See Supplemental Material at http://link.aps.org/supplemental/10.1103/PhysRevApplied.17.064035 for Videos SV1–SV5 depicting the motion of skyrmions corresponding to the cases shown in Fig. 1(a) (Video SV1), Fig. 2 (Video SV2), Fig. 3(c)–(f) (Video SV3), Fig. 5(c) (Video SV4), and Fig. 6(c) (Video SV5).

[34] R. M. Menezes, J. Mulkers, C. C. d. S. Silva, and M. V. Milošević, Deflection of ferromagnetic and antiferromagnetic skyrmions at heterochiral interfaces, Phys. Rev. B **99**, 104409 (2019).

[35] J. Castell-Queralt, L. González-Gómez, N. Del-Valle, A. Sanchez, and C. Navau, Accelerating, guiding, and compressing skyrmions by defect rails, Nanoscale **11**, 12589 (2019).

[36] S. M. Lewis, M. S. Hunt, G. A. DeRose, H. R. Alty, J. Li, A. Wertheim, L. De Rose, G. A. Timco, A. Scherer, and S. G. Yeates *et al.*, Plasma-etched pattern transfer of sub-10 nm structures using a metal–organic resist and helium ion beam lithography, Nano Lett. **19**, 6043 (2019).

[37] W. Kluge, Computation of switching functions using input-pattern-conserving magnetic-bubble manipulations, Electron. Lett. **8**, 313 (1972).

[38] A. Vansteenkiste, J. Leliaert, M. Dvornik, M. Helsen, F. Garcia-Sanchez, and B. Van Waeyenberge, The design and verification of MuMax3, AIP Adv. **4**, 107133 (2014).