High-Performance and Low-Power Transistors Based on Anisotropic Monolayer β-TeO_2

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Two-dimensional (2D) semiconductors offer a promising prospect for high-performance and energy-efficient devices especially in the sub-10-nm regime. Inspired by the successful fabrication of 2D β-TeO_2 and the high *on:off* ratio and high air stability of fabricated FETs [Zavabeti *et al.*, Nat. Electron. 4, 277 (2021)], we provide a comprehensive investigation of the electronic structure of monolayer β-TeO_2 and the device performance of sub-10-nm MOSFETs based on this material. The anisotropic electronic structure of monolayer β-TeO_2 plays a critical role in the anisotropy of transport properties for MOSFETs. We show that the 5.2-nm gate-length *n*-type MOSFET holds an ultrahigh *on*-state current exceeding 3700 μA/μm according to International Roadmap for Devices and Systems (IRDS) 2020 goals for high-performance devices, which is benefited by the highly anisotropic electron effective mass. Moreover, monolayer β-TeO_2 MOSFETs can fulfill the IRDS 2020 goals for both high-performance and low-power devices in terms of on-state current, subthreshold swing, delay time, and power-delay product. This study unveils monolayer β-TeO_2 as a promising candidate for ultrascaled devices in future nanoelectronics.

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I. INTRODUCTION

The continuous down-scaling demand of MOSFETs inspires the intensive exploration of the channel semiconductors in the past decades [1]. Two-dimensional (2D) semiconductors exhibit excellent electrostatic gate control ability and are capable of suppressing carrier scattering even though in the sub-10-nm regime because of their atomic scale thickness and dangling bond-free smooth surface [2–5]. Therefore, 2D semiconductors are expected to hold strong advantages as the candidate channel materials for ultrascaled MOSFETs. Motivated by the promising potential of 2D semiconductors, tremendous research efforts have been devoted to exploring the incorporation of 2D semiconductors as the channel of MOSFETs. Recent experiments have successfully demonstrated MOSFET operations of multiple 2D semiconductors, including MoS_2, InSe, Bi_2O_2Se, tellurene [6–18]. Recently, monolayer $MoSi_2N_4$ has also been actively explored as a candidate material for MOSFET applications due to their exceptional electrical properties and the presence of Ohmic metal contact with standard CMOS metal electrodes [17,19,20]. In addition, computational device modeling of sub-10-nm MOSFETs has also been carried out intensively in recent decades in order to search for 2D semiconductors and device architecture with exceptional performance figures of merit [21–26].

Among the emerging 2D semiconductors, 2D black phosphorene (BP) MOSFETs have been demonstrated to exhibit an *on:off* ratio on the order of 10^5 and the charge-carrier mobility can reach up to 1000 $cm^2\ V^{-1}\ s^{-1}$ [27–31]. Previous theoretical researches suggested that when the channel length is shortened to sub-10 nm, the high *on*-state currents (approximately 4000 μA/μm) and fast switching speed can also be achieved in BP MOSFETs [32,33]. Benefiting from the highly anisotropic band structure, BP MOSFETs are capable of delivering better device performance when compared to other 2D materials with nearly isotropic electronic properties, such as MoS_2 [34–36]. The anisotropic effective mass directly leads to the generation

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of high saturation current with steep subthreshold swing (SS), thus realizing a high *on*-state current [37,38]. However, BP is unstable in ambient atmosphere and the performance of MOSFETs suffers from severe degeneration. Therefore, the search of anisotropic 2D semiconductors with high stability and high device performance is an urgent task for the development of next-generation nanoelectronics.

2D β tellurium dioxide (β-TeO_2) is predicted to be an oxide semiconductor with highly anisotropic crystal and electronic structures with a wide band gap [39]. Recently, 2D β-TeO_2 nanosheets have been successfully synthesized through the surface oxidation of a eutectic mixture of tellurium and selenium [40]. The synthesized bilayer β-TeO_2 has a band gap of 3.7 eV, indicating its optical transparency within the visible light spectrum. In addition, the fabricated β-TeO_2 MOSFET is highly stable under ambient condition and exhibits a low SS and an *on:off* ratio exceeding 10^6. The hole carrier mobility reaches 232 $cm^2\ V^{-1}\ s^{-1}$ at room temperature and 6000 $cm^2\ V^{-1}\ s^{-1}$ at −50 °C. Despite the physical properties of 2D β-TeO_2 have been closely scrutinized, the transport properties of 2D β-TeO_2, especially its compatibility for ultrascaled nanoelectronics and the device performance limit of 2D β-TeO_2 MOSFETs, remain an open question thus far.

In this work, we investigate the electronic structure and ballistic transport properties of monolayer β-TeO_2 by combining the density-functional theory (DFT) with the nonequilibrium Green function (NEGF) method. The electronic transport properties of sub-10-nm gate-length MOSFETs are found to be highly anisotropic due to the anisotropic electronic structure of monolayer β-TeO_2. We demonstrate that *n*-type monolayer β-TeO_2 MOSFET with 5.2-nm gate length can sustain an ultrahigh *on*-state current up to 3750 $\mu A/\mu m$ due to the low electron effective mass along *y* direction, thus fulfilling the International Roadmap for Devices and Systems (IRDS) 2020 goals for high-performance (HP) devices [41]. The proposed monolayer β-TeO_2 MOSFETs can be further scaled down to 4.0 nm for HP applications and 5.2 nm for low-power (LP) applications, thus suggesting the versatility of 2D β-TeO_2 in meeting the demands of next-generation nanoelectronics. In addition, the *on*-state current, delay time, and power consumption are predicted to exceed most of the other 2D-material-based MOSFETs. These findings reveal the potential of monolayer β-TeO_2 MOSFETs as a strong contender in nanoelectronics, with outstanding performance in both the HP and LP device specifications of future technology nodes.

II. COMPUTATIONAL METHODS

The geometry optimization and electronic properties are carried out using the DFT package in the Atomistix ToolKit (ATK) 2020 version [42]. The DFT calculations are performed by the generalized gradient approximation in the form of Perdew-Burke-Ernzerh of realization using PseudoDojo potentials [43]. Monkhorst-Pack *k*-point mesh is used, with size $25 \times 25 \times 1$ for geometric optimization and $33 \times 33 \times 1$ for electronic property calculation [44]. The density mesh cutoff is set to 75 Hartree.

The device performance is simulated by combining the DFT and NEGF method in ATK 2020. The drain current I_{DS} is calculated based on the Landauer-Bűttiker formula [45,46]. I_{DS} at a given bias voltage V_b and gate voltage V_g is obtained by

$$I_{DS}(V_b, V_g) = \frac{2e}{h}\int_{-\infty}^{+\infty}\{T(E, V_b, V_g)[f_S(E-\mu_S) - f_D(E-\mu_D)]\}dE, \quad (1)$$

where $T(E,\ V_b,\ V_g)$, $f_{S/D}$, and $\mu_{S/D}$ are the transmission function, the Fermi-Dirac distribution functions for the source and drain, and the electrochemical potentials of the source and drain, respectively. And the difference value between μ_S and μ_D is equal to $e \times V_b$. The *k*-dependent transmission coefficient $T_{k\|}(E)$ is obtained by

$$T_{k\|}(E) = \mathrm{Tr}\{\Gamma^S_{k\|}(E)G_{k\|}(E)\Gamma^D_{k\|}(E)[G_{k\|}(E)]^\dagger\}, \quad (2)$$

where $\Gamma^{S/D}_{k\|}(E) = i[\Sigma^{S/D}_{k\|} - (\Sigma^{S/D}_{k\|})^\dagger]$ represents the broadening width deriving from source and drain in the form of self-energy $\Sigma^{S/D}_{k\|}$. $G_{k\|}(E)$ and $[G_{k\|}(E)]^\dagger$ are the retard and advanced Green function, respectively. The reciprocal lattice vector $k\ \|$ is perpendicular to the transport direction. The average of *k*-dependent transmission coefficient leads to the transmission function $T(E)$.

III. RESULTS AND DISCUSSION

We first discuss the optimized crystal structure and electronic properties of monolayer β-TeO_2, including band structure and effective mass. The anisotropic atomic structure of monolayer β-TeO_2 is shown in Fig. 1(a), with the optimized lattice parameters of $a = 5.44$ Å and $b = 5.76$ Å. The optimized lattice parameters agree with the results of previous theoretical calculations [39,47]. Monolayer β-TeO_2 possesses $P21/c$ symmetry (No. 14), containing four tellurium atoms and eight oxygen atoms in each unit cell. One tellurium atom is bonded to four neighboring oxygen atoms while one oxygen atom is bonded to two neighboring tellurium atoms. Figure 1(a) also shows the anisotropic atomic structure of monolayer β-TeO_2, which reveals the possible anisotropy of its electronic properties.

The band structure and effective mass of monolayer β-TeO_2 are then calculated, as shown in Fig. S1 within the Supplemental Material [48] and Fig. 1(b), respectively. The band gap is found to be 2.59 eV for monolayer β-TeO_2. The VBM is located at Γ point, while the

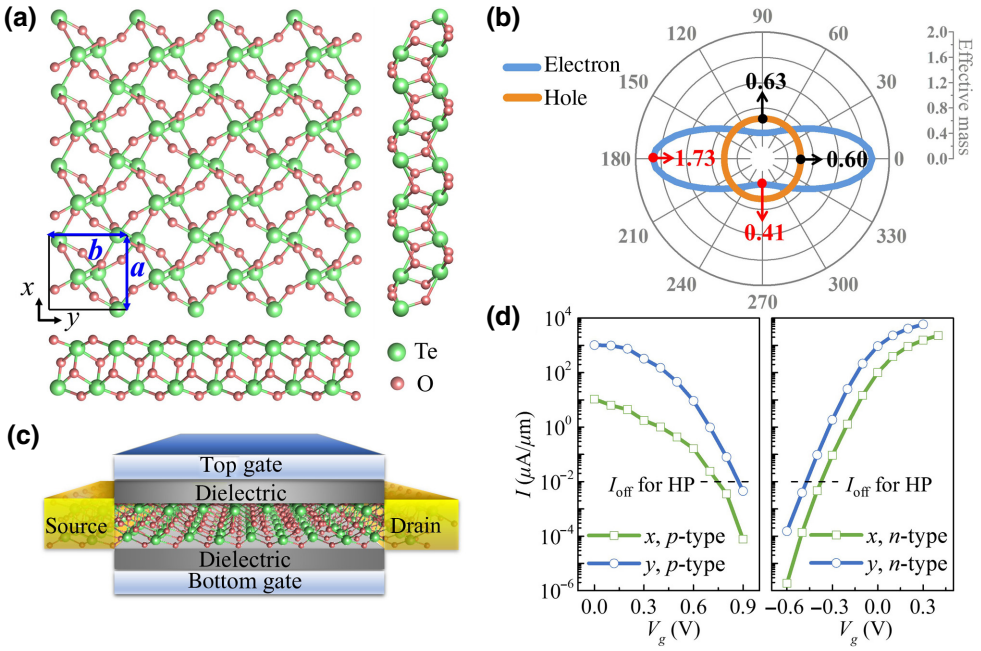

FIG. 1. (a) Top and two side views of monolayer β-TeO_2 structure. (b) Effective mass for electrons and holes of monolayer β-TeO_2. 0° and 90° angles represent the x and y directions, respectively. (c) Schematic illustration of the double-gated monolayer β-TeO_2 MOSFET. The dielectric constant of dielectric layer is $\varepsilon = 4.0$. The channel length is equal to the gate length (L_g). (d) Transfer characteristics of the p- and n-type monolayer β-TeO_2 MOSFETs, with $L_g = 5.4$ nm for the x direction (transport direction) and $L_g = 5.2$ nm for the y direction (transport direction). The drain source voltage is $V_{DS} = 0.65$ V, equal to the supply voltage (V_{DD}).

conduction-band minimum (CBM) is $0.06 \times 2\pi/a$ away from Γ point, which is very close to the Γ point. The monolayer β-TeO_2 is thus a nearly direct band-gap semiconductor. For the VBM, the band dispersions of monolayer β-TeO_2 along the x and y directions are almost identical. However, the band dispersions around the CBM along y direction are difficult to be determined directly from the band structure as shown in Fig. S1 within the Supplemental Material [48]. In order to clear illustrate the energy dispersions, we calculate the effective mass for electrons and holes along different directions in $x-y$ plane, as shown in Fig. 1(b). It can be clearly seen that the hole effective mass is nearly isotropic with 0.60 m_0 and 0.63 m_0 along the x direction and y direction, respectively. In contrast, the electron effective mass along the x direction is 1.73 m_0, which is significantly larger than the 0.41 m_0 along the y direction.

We next explore the device performance of p- and n-type monolayer β-TeO_2 MOSFETs, along x and y transport directions. The schematic drawing of the simulated MOSFET is shown in Fig. 1(c). The monolayer β-TeO_2 channel is sandwiched between top and bottom dielectric layers and metal gates. Highly doped monolayer β-TeO_2 is adopted as the source and drain of the device and it is assumed that the external metal electrodes form efficient Ohmic contacts with monolayer β-TeO_2 without the need of thermal charge injection over a contact Schottky barrier [49]. Different doping concentrations are investigated to optimize the device performance (see Figs. S2 and S3 within the Supplemental Material [48]). The optimized electrode doping concentration for the n-type MOSFET along the y direction is 6×10^{13} cm^{-2}, while the optimized doping concentration for the n-type MOSFET along the x direction and the p-type MOSFET along the x and y directions is 8×10^{13} cm^{-2}.

On-state current (I_{on}) is an important figure of merit that can be acquired from the transfer characteristics, which is evaluated at $V_{g,on} = V_{DS} + V_{g,off}$, where $V_{g,on}$ and $V_{g,off}$ represent the gate voltage of the *on* state and *off* state, respectively, and V_{DS} is the drain source voltage, which is equal to the V_b and supply voltage (V_{DD}). The transfer characteristics of p- and n-type monolayer β-TeO_2 MOSFETs with 5-nm gate length along x and y directions are shown in Fig. 1(d). The *off* -state current (I_{off}) is taken to be 0.01 μA/μm according to the IRDS 2020 goals for HP devices in 2028, marked as black dashed line in Fig. 1(d). The obtained I_{on} is summarized in Table I.

For the n-type MOSFETs with 5-nm gate length, the *on*-state current along the y direction reaches 3750 μA/μm, which is much higher than that along the x direction (1300 μA/μm), since the anisotropic electron effective mass is 0.41 m_0 along the y direction versus 1.73 m_0 along the x direction. The difference between the *on*-state currents along different transport directions can also be

TABLE I. The hole (h) and electron (e) effective mass of monolayer β-TeO_2, and the *on*-state current (I_{on}) of 5-nm gate-length monolayer β-TeO_2 MOSFETs along different transport directions.

	x, h	y, h	x, e	y, e
Effective mass (m_0)	0.60	0.63	1.73	0.41
	x, p type	y, p type	x, n type	y, n type
I_{on} (μA/μm)	7	615	1300	3750

identified from the transmission spectrum in the *on* state (see Fig. S4 within the Supplemental Material [48]). On the other hand, the unexpected *on*-state currents are observed for the p-type MOSFETs along the x and y directions. Although the hole effective mass in the VBM exhibits an isotropic characteristic, the *on*-state current along the x direction (7 μA/μm) is 2 orders of magnitude smaller than that along the y direction (615 μA/μm).

In order to understand the connection between the electronic band structure and device performance, the local band structure around the CBM and VBM of monolayer β-TeO_2 and the corresponding transmission coefficients of MOSFETs are computed, as shown in Figs. 2 and 3. As shown in Figs. 2(a) and 2(b), the energy dispersions of CBM along the x direction show a slight "M" shape with the minimum point located at X'' point, while the conduction band along y direction shows a sharper peak at X'' point. The transmission coefficients as a function of the transverse wave vectors reveal that the shape and the width of the *on*-state transmission coefficient window are sensitively dependent on the band dispersion near the CBM, as shown in Figs. 2(c) and 2(d) for the transport direction along the x and y direction, respectively. When the transport direction is along the x direction, the transmission coefficient versus transverse wave vector k_y in Fig. 2(c) has one hill, which is similar to the band dispersions along the y direction. When the transport is along the y direction, the transmission coefficient versus the transverse wave vector k_x exhibits an "M" shape profile, which is akin to the band dispersions along the x direction. Furthermore, the transmission coefficient versus k_x spans over a wider wave-vector window than that versus k_y, thus resulting in a higher *on*-state transport current when the MOSFET is operated along the y direction.

For hole transport mediated by the valence band of monolayer β-TeO_2, there is only one valley near VBM as located at the Γ point, as shown in Figs. 3(a) and 3(b). The band dispersions along the x and y directions are almost the same at the energy level larger than -1.45 eV. However, when the energy level is lower than -1.45 eV, a suddenly weaker band dispersion appears along the x direction, which is in stark contrast to that along the y direction. Correspondingly, the transmission coefficient versus k_y with x direction as the transport direction is significantly suppressed in comparison with that versus k_x with y direction as the transport direction in Fig. 3(c). Such contrasting transmission coefficient windows arise from the suddenly appeared flat band dispersion at -1.45 eV and explain the extremely low *on*-state current (only 7 μA/μm) of the x-directed MOSFET.

To further verify whether the holes at the -1.45 eV energy level contribute to the device performance, we investigate the valence-band structure, density of states (DOS), and hole concentration of high-doped monolayer β-TeO_2, as shown in Fig. S5 within the Supplemental Material [48]. The doping concentration is set to 8×10^{13} cm^{-2} because the injected carriers are provided by the highly doped monolayer β-TeO_2 source region. After the p-type doping, the VBM shifts up to 0.09 eV and the Fermi level lies below the valence band. At thermal equilibrium, the energy distribution function for holes is obtained by the Fermi-Dirac distribution $f_h(E)$ [50],

$$f_h(E) = 1 - \frac{1}{\exp((E - E_F)/kT) + 1}, \tag{3}$$

where E_F, k, and T represent the Fermi energy level, Boltzmann's constant, room temperature, respectively. The hole concentration is defined as [50]

$$p(E) = D_h(E) f_h(E), \tag{4}$$

where $D_h(E)$ represents the DOS for holes. The calculated hole concentration for highly doped monolayer β-TeO_2 is shown in Fig. S5(c) within the Supplemental Material [48]. As the holes around -0.07 eV at the flat band near VBM is within the energy-level range of the hole concentration, these holes with a large effective mass thus have a substantial impact on the device performance and have resulted in extremely low transmission coefficients and *on*-state current in the x-directed p-type MOSFET, as compared to the y-directed p-type MOSFET.

Considering that only the n-type monolayer β-TeO_2 MOSFETs along the y direction can fulfill the IRDS 2020 requirements, we further investigate the n-type configuration along the y direction with other sub-10-nm channel lengths. We aim to explore the ballistic performance upper limit of the monolayer β-TeO_2 MOSFETs, with no scattering events dominating the device performance. We first focus on HP devices. The electrode doping concentration is the same as that of 5.2 nm n-type monolayer β-TeO_2 MOSFET. The transfer characteristics are presented in Fig. 4(a) and the calculated figures of merit are summarized in Table SI within the Supplemental Material [48]. The leakage current increases with the decreasing channel length. When the channel is shorter than 4.0 nm, the leakage current is overly high and fails to meet the HP requirements due to the severe short channel effect. Hence, the channel length

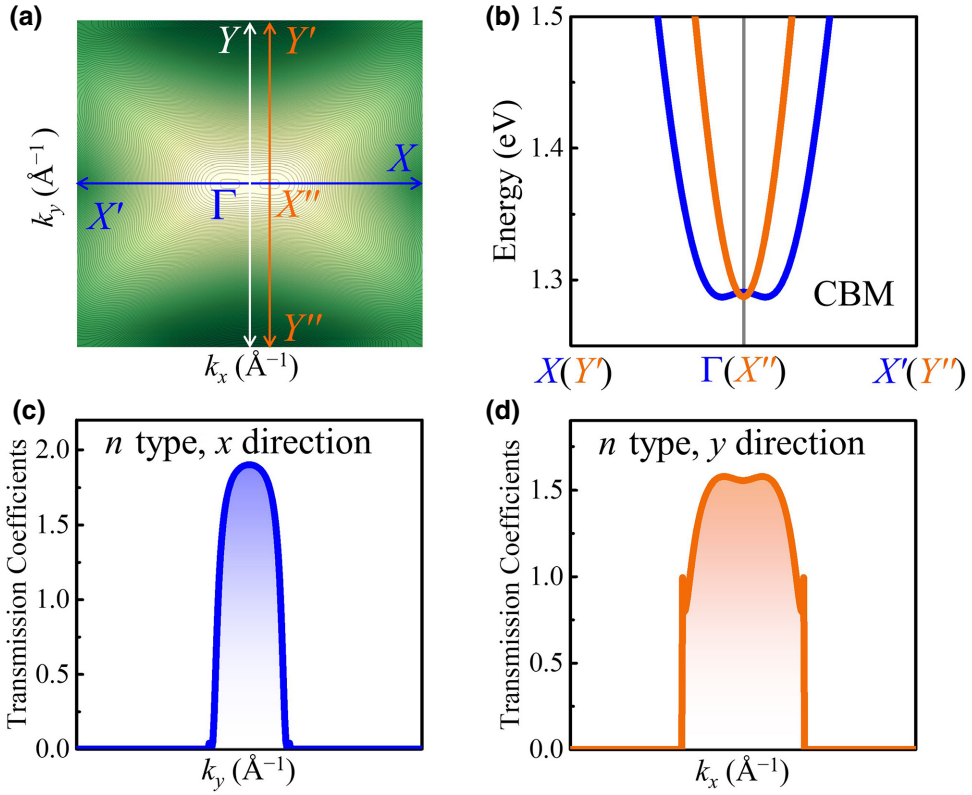

FIG. 2. The (a) energy contour plots of the lowest conduction band and (b) local conduction band around the Γ point in the first Brillouin zone of monolayer β-TeO_2. The transmission coefficients versus transverse wave vector (c) k_y and (d) k_x of 5-nm gate-length n-type monolayer β-TeO_2 MOSFETs with the transport direction along the x and y directions in the *on* state, respectively. The energy value corresponding to the maximum spectral current is the energy point of the transmission coefficient.

of 4.0 nm can be regarded as the theoretical limit for monolayer β-TeO_2 MOSFET with an *on*-state current of 2010 μA/μm. Notably, the MOSFETs with the channel length larger than 5.2 nm possess an *on*-state current higher than 3400 μA/μm.

Subthreshold swing (SS) is another key figure of merit to evaluate the gate electrostatic control ability of logic devices, which is defined as the gate voltage required to change the current by one order of magnitude. For the channel lengths ranging from 9.8 to 5.2 nm, the SS (i.e., 67–72 mV/dec) is close to the thermionic limit of 60 mV/dec and fulfills the IRDS 2020 requirements for HP devices in the 2028 horizon (i.e., SS < 75 mV/dec). The SS increases slowly with a shorter channel. When the channel is shorter than 5.2 nm, SS rises rapidly with a shorter channel, reaching 86 mV/dec for 4.6 nm channel and 98 mV/dec for 4.0 nm channel.

Considering that BP also has anisotropic electronic properties, we further compare the device performance of the monolayer β-TeO_2 MOSFETs with that of BP MOSFETs. High performance of MOSFETs needs both high saturation current (I_{sat}), low SS, and low leakage current. I_{sat} is proportional to the injection carrier velocity υ_{inj} at the source edge under ballistic transport [37,51]. Here, υ_{inj} along x direction as the transport direction can be expressed by [51]

$$\upsilon_{inj} \propto \left(\frac{N_s}{m_{DOS} \times m_x}\right)^{1/2}, \tag{5}$$

where m_{DOS} is the DOS effective mass [$m_{DOS} = (m_x \times m_y)^{1/2}$] and N_s is the surface carrier concentration. Low m_{DOS} and low m_x are effective in increasing υ_{inj} and I_{sat}. When m_x is large, υ_{inj} and I_{sat} are low, which limit the value of I_{on}. Therefore, the I_{on} of x-directed n-type monolayer β-TeO_2 MOSFET and the y-directed p-type BP MOSFET are limited due to the large effective masses, as shown in Table SII within the Supplemental Material [48]. In addition, because the band gap of monolayer β-TeO_2 is larger than that of black phosphorene, the I_{on} of x-directed n-type monolayer β-TeO_2 MOSFET is lower than that of the y-directed p-type BP MOSFET, which are 670 μA/μm and 2400 μA/μm, respectively.

However, the m_x of BP is too low, which increases the source-drain tunneling current and results in a strong *off* -state leakage, degrading SS and limiting I_{on}. Of note, the m_y of monolayer β-TeO_2 is suitable, which can support the small SS and simultaneously maintain a high I_{on}.

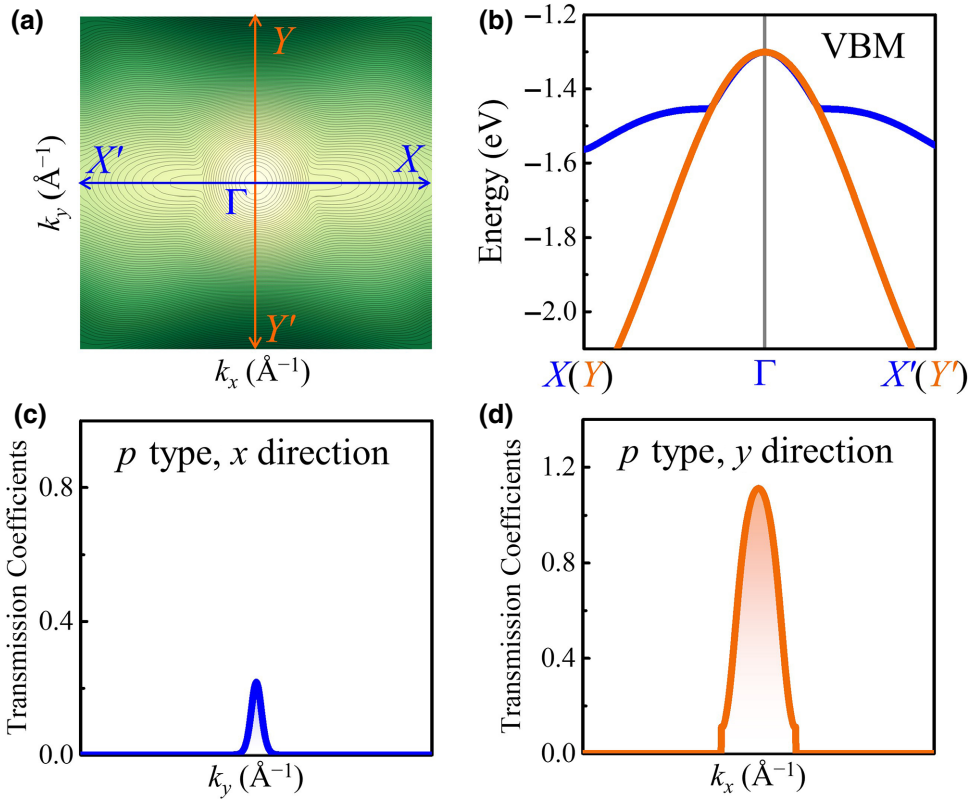

FIG. 3. The (a) energy contour plots of the highest valence band and (b) local valence band around the Γ point in the first Brillouin zone of monolayer β-TeO_2. The transmission coefficients versus transverse wave vector (c) k_y and (d) k_x of 5-nm gate-length p-type monolayer β-TeO_2 MOSFETs with the transport direction along the x and y directions in the *on* state, respectively. The energy value corresponding to the maximum spectral current is the energy point of the transmission coefficient.

In a word, although the electronic properties of monolayer β-TeO_2 and BP are all anisotropic, the suitable anisotropic effective masses of monolayer β-TeO_2 make it the better device performance.

Besides, we also compare the device performances of 2D β-TeO_2 with other 2D materials based on the standards of the International Technology Roadmap for Semiconductors (ITRS) 2013 [52]. According to the ITRS 2013

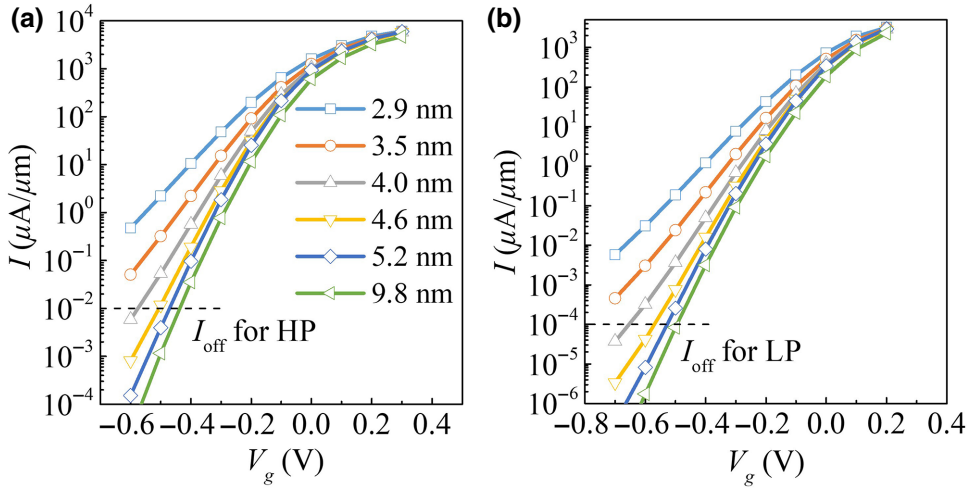

FIG. 4. Transfer characteristics of n-type monolayer β-TeO_2 MOSFETs along the y direction for (a) HP and (b) LP requirements according to IRDS 2020. The *off* -state current for HP and LP requirements is marked as black dashed line in (a), (b), respectively. The gate length of n-type monolayer β-TeO_2 MOSFETs along the y direction is equal to the channel length, which ranges from 2.9 to 9.8 nm.

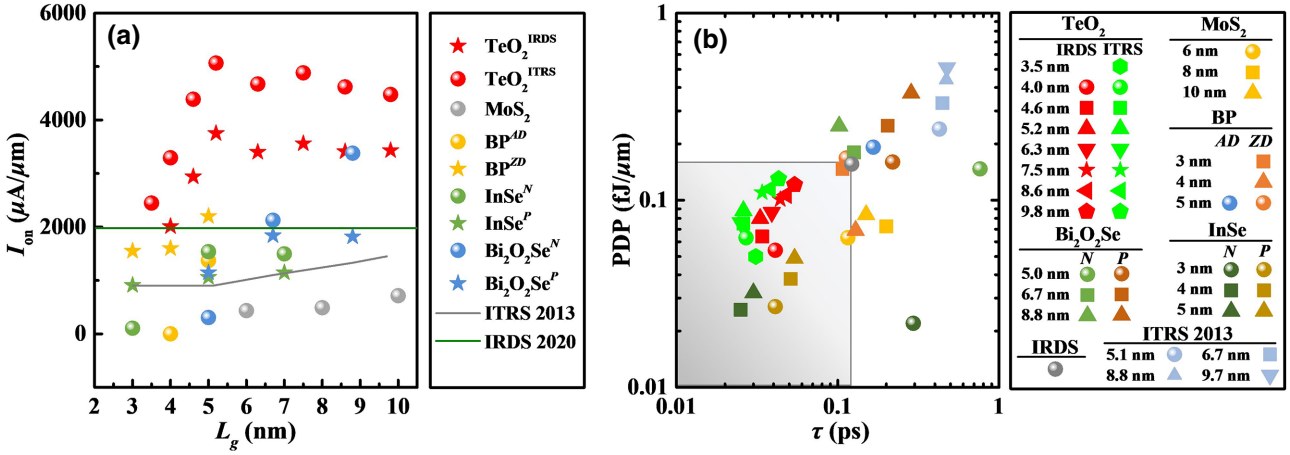

FIG. 5. The (a) *on*-state current (I_{on}), and (b) power-delay product versus delay time (τ) of *n*-type monolayer β-TeO_2 MOSFETs along *y* direction for HP requirements according to two different standards, IRDS 2020 for the year 2028 and ITRS 2013. The data for MOSFETs based on other 2D materials according to ITRS 2013 are shown for comparison [53–56]. The superscript "*AD*" and "*ZD*" represent that the transport directions of MOSFETs are along armchair and zigzag directions, respectively. The superscript "*N*" and "*P*" represent the *n*-type and *p*-type MOSFETs, respectively.

standards where the *off* -state current is fixed at 0.1 μA/μm, we summarize the figures of merit such as the *on*-state current and SS in Table SIII within the Supplemental Material [48]. Due to the higher *off* -state current standard of ITRS 2013, the *on*-state current of the *n*-type monolayer β-TeO_2 MOSFETs increases by more than 1000 μA/μm for the same channel length and the channel limit is shortened to 3.5 nm. The highest *on*-state current reaches 5140 μA/μm in the 5.2 nm gate-length monolayer β-TeO_2 MOSFETs. As shown in Fig. 5(a), for sub-10-nm nodes, monolayer β-TeO_2 MOSFETs possess a significantly higher *on*-state current than the MOSFETs based on other 2D materials, such as BP and Bi_2O_2Se [53–56], thus revealing the strong switchability of monolayer β-TeO_2 for logic devices.

Apart from the *on*-state current, the intrinsic gate delay time (τ) and the power-delay product (PDP) are another two key indicators for transistors. The intrinsic gate delay time τ describes the upper limit of the switching speed [32],

$$\tau = \frac{Q_{on} - Q_{off}}{I_{on}}, \tag{6}$$

where Q_{on} and Q_{off} are the charges in the channel region in the *on* and *off* state, respectively. PDP is the power consumption in one switching operation and is calculated by [32]

$$\mathrm{PDP} = V_{DS} I_{on} \tau = V_{DS}(Q_{on} - Q_{off}). \tag{7}$$

The PDP versus τ of *n*-type monolayer β-TeO_2 MOSFETs along *y* direction for HP requirements is shown in Fig. 5(b). According to IRDS 2020, sub-10-nm monolayer β-TeO_2 MOSFETs have a series of delay times ranging from 0.041 to 0.054 ps and PDP ranging from 0.054 fJ/μm to 0.121 fJ/μm. These data all satisfy the HP standards of IRDS 2020 in 2028 horizon, as denoted in the gray shaded region in Fig. 5(b). We then compare the τ and PDP with other 2D material MOSFETs. The standards are adopted in accordance with the ITRS 2013. The τ and PDP of monolayer β-TeO_2 MOSFETs are lower than those of the MOSFETs based on MoS_2, black phosphorene, Bi_2O_2Se. In addition, monolayer β-TeO_2 MOSFETs have a little higher PDP than 2D InSe MOSFETs, while their delay times are comparable. Overall, these results indicate the compelling potential of the monolayer β-TeO_2 MOSFETs as a channel material for ultrascaled HP MOSFETs.

In contrast to HP devices, LP devices require a lower *off* -state current to serve the purpose of saving static energy. For the LP device, the optimized doping concentration of electrodes for LP transistors is 4×10^{13} cm^{-2}. We note that the optimal doping concentrations are different for HP and LP devices due to their different operating requirements. Figure 4(b) shows the transfer characteristics of LP monolayer β-TeO_2 MOSFETs under different channel lengths. The *on*-state current for LP devices is evaluated with *off* -state current fixed at 1×10^{-4} μA/μm according to the IRDS requirements. The MOSFETs in the cases of $L_g > 5$ nm provide the higher *on*-state current than that in the IRDS requirements (see Table SIV within the Supplemental Material [48]). While HP transistors are more dependent on the superthreshold characteristics, the LP transistors rely more on the subthreshold characteristics [57]. LP monolayer β-TeO_2 MOSFETs display lower SS than HP, ranging from 67 to 64 mV/dec for the 5.2–9.8 nm channel. The small values of SS indicate the good device electrostatics of LP monolayer β-TeO_2 MOSFETs. Although the SS is lower than that of

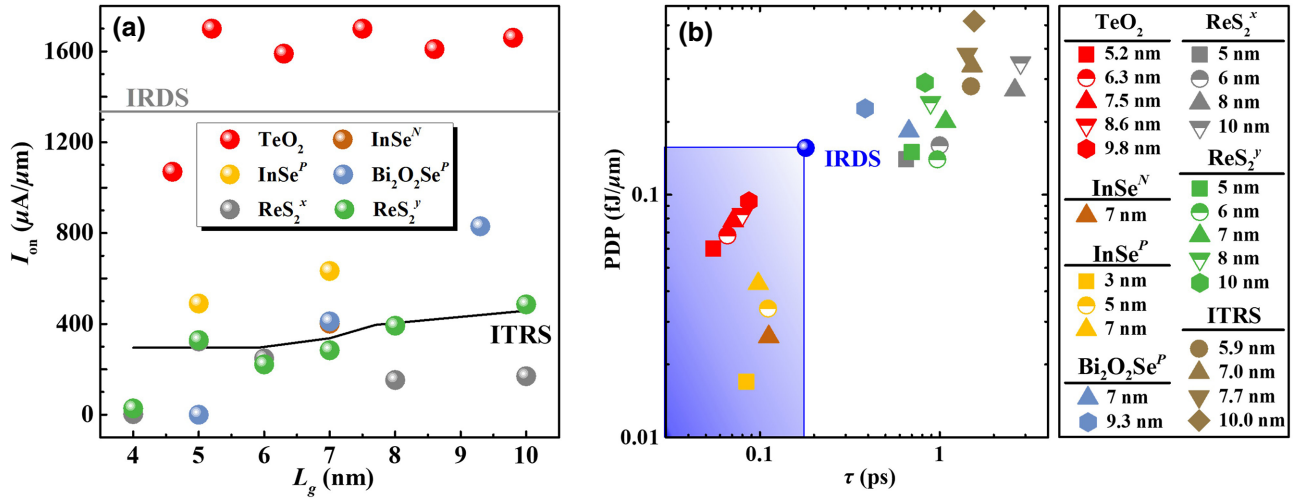

FIG. 6. The (a) *on*-state current (I_{on}), and (b) power-delay product versus delay time (τ) of *n*-type monolayer β-TeO_2 MOSFETs along *y* direction for LP requirements according to IRDS 2020 for the year 2028. The data for MOSFETs based on other 2D materials according to ITRS 2013 are shown for comparison [54,55,58]. The superscripts "*x*" and "*y*" represent that the transport directions of MOSFETs are along *x* and *y* directions, respectively.

monolayer $MoSi_2N_4$ MOSFETs, LP monolayer β-TeO_2 MOSFETs have higher *on*-state currents [17]. Furthermore, the *on*-state currents of LP monolayer β-TeO_2 MOSFETs are higher than those of other 2D semiconductor LP MOSFETs as shown in Fig. 6(a), indicating a higher *on:off* ratio and operating speed.

We next evaluate whether the τ and PDP of *n*-type monolayer β-TeO_2 MOSFETs can satisfy the LP requirements of IRDS 2020. The calculated τ and PDP are shown in Fig. 6(b) and Table SIV within the Supplemental Material [48]. The τ and PDP gradually decrease as the channel length shortens, which are consistent with previous studies [58]. The τ (0.055–0.087 ps) and PDP (0.060–0.094 fJ/μm) fulfill the LP requirements of IRDS 2020 for all channel lengths down to 5.2 nm. In particular, the τ and PDP of monolayer β-TeO_2 MOSFETs are far lower than those of ReS_2 and Bi_2O_2Se MOSFETs in the sub-10-nm nodes. Compared with InSe MOSFETs, monolayer β-TeO_2 MOSFETs have a higher PDP but a shorter τ. The τ and PDP of monolayer β-TeO_2 MOSFETs are also comparable with those of monolayer $MoSi_2N_4$ MOSFETs [17]. The short intrinsic delay time and low power consumption thus further reveal the promising potential of monolayer β-TeO_2 MOSFETs for LP applications in digital circuits.

IV. CONCLUSIONS

In summary, we explore the electronic properties of monolayer β-TeO_2 and performance limits of sub-10-nm gate-length monolayer β-TeO_2 MOSFETs. Our results demonstrate that monolayer β-TeO_2 is a promising candidate for HP and LP devices. The anisotropic band dispersions near VBM and CBM lead to the anisotropic device performance of monolayer β-TeO_2 MOSFETs. The performance of the *n*-type monolayer β-TeO_2 MOSFETs along *y* direction meets the IRDS 2020 requirement in terms of *on*-state current, SS, delay time, and PDP. In particular, the *on*-state current can reach up to 3750 μA/μm due to the corresponding anisotropic effective mass. Combining its advantage of high air stability, monolayer β-TeO_2 is therefore a competitive air-stable channel material in the application of nanoelectronics and transparent logic devices [31].

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