(La,Ba)SnO_3-based Thin-Film Transistors: Large-Signal Model and Scaling Projections

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Perovskite oxides are extremely interesting for their possible use in high-mobility thin-film transistors (TFTs) suitable for high-performance large-area circuits. Here we present a semianalytical model of a recently fabricated TFT based on La-$BaSnO_3$, and explore the possibilities for technology optimization and the intrinsic potential of the device concept for applications in transparent and flexible electronics. We show that La-$BaSnO_3$ TFTs can outperform existing TFT device technologies through a detailed benchmarking exercise, and that these devices can be promising for display electronics and for a broader range of applications.

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I. INTRODUCTION

Pervasive electronics is the umbrella term we use to recognize the embedding of sensors and actuators, displays, logic and even cognitive capabilities in everyday objects, in the environment and in living organisms, with form factors that go beyond the classical board-based electronic system. This requires electronic systems that naturally merge with the host environment, for example, by being transparent, by being applicable to curved and irregular surfaces, or by being flexible.

Thin-film transistors can fulfill the requirements of both bendability and transparency to the visible light, and have naturally emerged as the basic building blocks in this area. The opportunity to fabricate these devices through low-cost process flows broadens the spectrum of possible applications, that includes but is not limited to conformal active-matrix displays [1], radiofrequency identification transponders [2], transparent smart surfaces and solar cells [3].

The leading transparent TFT technology currently uses amorphous indium gallium zinc oxide (*a*-IGZO) as the channel material, which can provide, at the same time, relatively high mobility of around 10 $cm^2\ V^{-1}\ s^{-1}$ and good scaling properties [4,5]. On the downside, indium is expensive and suffers from a limited availability on the global market. Furthermore, the mobility achievable in *a*-IGZO films is too low to meet the ever-increasing performance requirements of TFT-based electronics.

To overcome these issues, new channel materials, based on earth-abundant elements and featuring higher intrinsic mobility, are actively investigated. In this context, lanthanum-doped barium stannate (La-$BaSnO_3$), a wide-band-gap semiconducting perovskite oxide, has recently attracted considerable interest. Thanks to a small electron effective mass, to a relatively weak coupling of electrons with polar-optical phonons and to a large dielectric permittivity, which results in an effective screening of charged impurities [6], thin films of La-$BaSnO_3$ exhibit room-temperature mobility as high as 183 $cm^2\ V^{-1}\ s^{-1}$ [7]. The growth of La-$BaSnO_3$ films on flexible substrates by using low-cost and low-thermal-budget processes suitable for mass production has already been demonstrated [8,9]. Furthermore, the La-$BaSnO_3$ optical band gap of more than 3 eV ensures a transmittance in the visible spectrum close to 90% [8].

Here, we consider the recently reported fabrication and characterization of a state-of-the-art, fully transparent La-$BaSnO_3$-based TFT [10], and we develop a semianalytical model able to accurately describe static and dynamic device operation. After validating the model against the experimental measurements, we move on by assessing the performance of the TFT for different possible applications and its evolution as a function of the geometrical scaling and of the improvement of the manufacturing techniques. Besides the standard use in driving displays, we also consider the application in digital and radiofrequency circuits, considering a recent research trend that has already led to the demonstration of TFT-based flexible microprocessors [11], analog-to-digital converters [12], memories [13], and near-field communication tags [14].

We find that La-$BaSnO_3$ TFTs show competitive performance with respect to both consolidated and newly

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proposed TFT technologies. Moreover, we show that considerable performance improvement is within reach by leveraging geometrical downscaling, reduction of trap states and contact resistance and, more specifically, by achieving in the TFT channel the high mobility demonstrated in unpatterned La-$BaSnO_3$ thin films.

The rest of the paper is organized as follows. In Sec. II, we illustrate the physical model and the simulation approach; in Sec. III, we discuss the calibration of the model and we assess the performance of the device for the current and future technological stages; finally, in Sec. IV, we present our concluding remarks.

II. MODEL

A. Geometry and electrostatics

The architecture of the considered transistor is sketched in panel (a) of Fig. 1. The device has a La-$BaSnO_3$ channel of thickness t_{ch} and width W, deposited on an insulating substrate. The current is modulated by means of a metallic top gate, separated from the channel by an insulator of thickness t_{ox}. The length of the channel region under the gate is denoted by L_G. The transport direction is assumed along the x axis, while the confinement direction of the channel film is assumed along y. The electrostatics of the device is modeled within a top-of-the-barrier approximation [15], in which the dependence of the potential ψ at the top of the channel barrier on the potential enforced at the gate and at the contacts is described by means of capacitive couplings. We denote by C_{ox} and C_S, C_D the geometrical capacitance associated to the top gate and the parasitic capacitances associated to the source and drain contacts, respectively [see Fig. 1(b)]. Moreover, we denote by C_Q the quantum capacitance [16] in the channel at the position x_{top} where the top of the barrier is located, and by C_{it} the parasitic capacitance that models the electrostatic effect of interface trap states. Further details on the trap model are provided later in this section.

According to the stated approximations, the energy E_C of the edge of the conduction band at x_{top} can be expressed as [17]

$$\begin{aligned} E_C = -q\psi = &-\frac{C_{ox}}{C_\Sigma} qV_G + \frac{qn_s}{C_\Sigma} - \frac{C_D}{C_\Sigma} qV_{D'} \\ &- \frac{(C_S + C_{it})}{C_\Sigma} qV_{S'}, \\ C_\Sigma = &\, C_{ox} + C_S + C_D + C_{it}, \end{aligned} \tag{1}$$

where n_s is the electron density in the channel at x_{top}, q is the absolute value of the electron charge, and V_G is the voltage applied to the gate. $V_{S'}$ and $V_{D'}$ denote the intrinsic source and drain voltage, linked to their extrinsic counterparts V_D and V_S by

$$V_{D'} = V_D + I_D R_D, \tag{2}$$

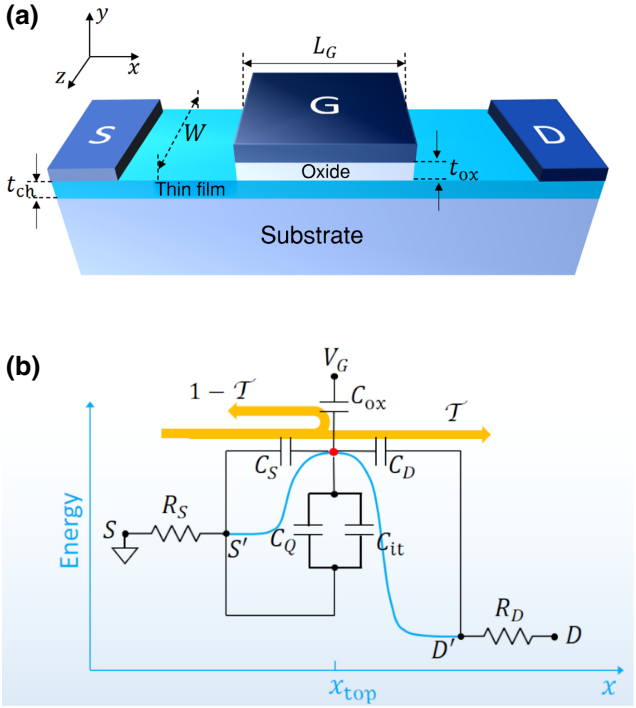

FIG. 1. (a) Sketch of the device. The layer labeled as "thin film" corresponds to the La-$BaSnO_3$ film. (b) Illustration of the circuit model of the device, including the capacitive and resistive effects, superimposed to the conduction-band-edge profile in the channel. C_{ox}, C_S, C_D, C_{it}, and C_Q denote the geometrical capacitance per unit area associated to the top gate, the parasitic capacitances associated to the source and drain contacts, the parasitic capacitance associated to the presence of trap states and the quantum capacitance, respectively. R_S and R_D denote the parasitic resistances associated to the source and drain contacts, respectively. The backscattering model for the transmission $\mathcal{T}$ is represented by the orange arrows. x_{top} denotes the position on the x axis where the top of the barrier (red dot) is located.

$$V_{S'} = V_S - I_D R_S. \tag{3}$$

In the previous equations, $R_S = R_D \equiv R_C$ indicate the contact resistance associated to the source and drain contacts [see Fig. 1(b)]. We model R_C as constant, thus neglecting any possible dependence on the gate voltage.

We notice that $C_Q = -\partial(qn_s)/\partial E_C$ does not explicitly appear in Eq. (1), since it is automatically taken into account by the dependence, enforced by the same equation, of the electron density at the top of the barrier on the potential.

B. Transport

The electron density is computed by combining the carrier fluxes coming from the source and drain contacts,

according to the following formula [18]:

$$n_s = \frac{q}{2}\sum_{i=0}^{N}\int_{-\infty}^{\infty} dE\, D_{2D,i}(E) \times \left[(2-\mathcal{T})\, f(E-E_{FS}+V_{S'}) + \mathcal{T} f(E-E_{FS}+V_{D'})\right], \tag{4}$$

where $\mathcal{T}$ is the transmission probability of electrons over the channel barrier, f is the Fermi-Dirac distribution, E_{FS} the Fermi level of the source contact,

$$D_{2D,i}(E) = g_v \frac{m^*}{\pi\hbar^2}\,\Theta(E-\epsilon_i)$$

is the two-dimensional (2D) density of states associated to the ith subband induced by the vertical confinement of the thin film [19], $\Theta(E)$ is the Heaviside function, $g_v = 1$ is the valley degeneracy, m^* is the isotropic effective mass, $\hbar$ the reduced Planck constant, and $\epsilon_i = \epsilon_i(E_C)$ denotes the onset energy of the ith subband. The integer N indicates the number of subbands included in the computation and is chosen large enough to guarantee stable results.

The current is computed by means of the Landauer formula [18],

$$I_D = \frac{q}{\pi\hbar}\sum_{i=0}^{N}\int_{-\infty}^{\infty} dE\, M(E,\epsilon_i) \times \mathcal{T}\left[f(E-E_{FS}+V_{S'}) + f(E-E_{FS}+V_{D'})\right]. \tag{5}$$

In Eq. (5), $M(E)$ denotes the mode distribution in the channel, defined as [18]

$$M(E) = W\frac{\pi\hbar}{2}\sum_{i=0}^{N}\langle v_{x,i}\rangle D_{2D,i}(E),$$

where

$$\langle v_{x,i}\rangle = \frac{2}{\pi}\sqrt{\frac{2(E-\epsilon_i)}{m^*}}$$

is the average injection velocity of electrons along the transport direction in the ith subband.

C. Transmission model

The transmission function is assumed of the form [15]

$$\mathcal{T}(E) = \frac{\lambda(E)}{\lambda(E)+l_c}, \tag{6}$$

where $\lambda(E)$ is the mean free path as a function of energy E, and l_c is the so-called critical length, which accounts for the dependence of the effective width of the barrier on V_G and on the drain-to-source bias V_D [20]. The reader is referred to the Appendix for further details.

D. Trap model

The parasitic capacitance per unit area associated to the presence of traps reads

$$C_{it} \equiv q\frac{dQ_{it}}{dE_C}, \tag{7}$$

where Q_{it} is the charge density per unit surface built up due to the filling of trap states.

The trap charge density can be expressed as

$$Q_{it} = q\int_{-\infty}^{\infty}\rho(E-E_C) f(E-E'_F)\, dE, \tag{8}$$

where $\rho(E)$ is the density of trap states per unit area and unit energy and E'_F is a quasi-Fermi-level with respect to which trapped electrons are assumed to be in equilibrium. We model $\rho(E)$ as a uniform distribution function of value D_{it} within an interval $[E_{min}, E_{max}]$ and zero outside:

$$\rho(E) = \begin{cases} D_{it} & E_{min} < E < E_{max} \\ 0 & \text{otherwise.} \end{cases} \tag{9}$$

The dependence of $\rho(E)$ on E_C accounts for the shift of the trap energy levels with the potential.

Following Ref. [21], we assume that trapped electrons are in equilibrium with the mobile electrons in the channel. For V_D larger than few tenths of volts, the latter can be considered approximately in equilibrium with the Fermi level of the source contact, since the injection of carrier from the drain contact is negligible. As a good approximation, we thus assume $E'_F \approx E_{FS}$. From Eqs. (7), (8), and (9), we finally obtain the following expression for C_{it}:

$$C_{it} \approx qD_{it}\left[f(E_C+E_{max}-E_{FS}) - f(E_C+E_{min}-E_{FS})\right]. \tag{10}$$

E. Numerical approach

Equations (1), (5), and (6) form a system of nonlinear implicit equations, in the unknowns E_C, $\mathcal{T}$, and I_D. We solve this system iteratively, by using a hybrid Broyden algorithm, as implemented in the package *fsolve* of the *scipy.optimize* Python library [22]. The algorithm runs until a relative difference smaller than 1.5×10^{-8} between the values of E_C, $\mathcal{T}$, and I_D at successive iterations is achieved.

III. PERFORMANCE ASSESSMENT AND PERSPECTIVES

A. Model calibration

In order to consider realistic values for the parameters of the model, we calibrate it on the measurements reported in Ref. [10] for a La-$BaSnO_3$-based TFT. The value of the

TABLE I. Main fitting parameters of the model. The columns "Calibration" and "Experiment" report the values assumed in simulations and those extracted from measurements [10], respectively.

Parameter	Calibration	Experiment
Contact resistance ($R_S + R_D$, kΩ μm)	7.0	5.1
Density of traps (D_{it}, eV^{-1} cm^{-2})	0.70×10^{12}	5.03×10^{12}
Electron mobility (μ, cm^2 V^{-1} s^{-1})	42	...

main fitting parameters is reported in Table I and compared with values estimated in Ref. [10]. For the channel length L_G and the geometrical gate capacitance C_{ox}, we assume the value extracted in Ref. [10] ($L_G = 295$ nm, $C_{ox} = 0.5$ μF cm^{-2}).

As the thickness of the La-$BaSnO_3$ channel of the reference device is 10 nm, the confinement effects are expected to be weak. Accordingly, we adopt the bulk value of the effective mass $m^* = 0.42$ m_0 [23]. In addition, in order to obtain more accurate results, we consider the presence of two-dimensional subbands instead of a pure three-dimensional density of states, as already stated in Sec. II B. Indeed, subbands arise each time a confinement is enforced, regardless of its strength, and, in the case at hand, some minor influence of the confinement-induced stepped shape of the density of states on transport can still be observed [19]. The charge density and the current are computed by including $N = 6$ subbands, which is checked to guarantee stable results for all the considered biases.

The gate insulator is assumed to be HfO_2, as in the prototype of Ref. [10].

The electron mobility in the La-$BaSnO_3$ channel, which enters the model through the transmission function (see Appendix), represents a further fitting parameter and has been estimated to be 42 cm^2 V^{-1} s^{-1}. The corresponding value of the peak field effect mobility is $\mu_{FE} = 17.5$ cm^2 V^{-1} s^{-1}, which is in agreement with the experimental value of 17.2 cm^2 V^{-1} s^{-1}. The parasitic capacitances C_S and C_D are assumed to be negligible and set to zero.

The experimental output characteristics in Ref. [10] do not show clear signatures of the presence of a gate-modulated Schottky barrier at the ITO/La-$BaSnO_3$ contacts. Particularly, the exponential behavior of the current at low V_D, typically associated to such a barrier, is not visible. In the spirit of developing a model with as few free parameters as possible in order to avoid overfitting, the value of contact resistances has been considered constant, as described in Sec. II A. The difference between the value assumed in simulations and the value inferred from measurements through a transmission-line model (see Table I) is well within the typical experimental uncertainty [24].

Due to the lack of any direct information on the distribution of traps over the energy, the value of E_{min} and E_{max} has been treated as free parameters of the model. Particularly, traps are assumed distributed over an energy window of $E_{max} - E_{min} = 2.7$ eV, fully contained within the La-$BaSnO_3$ band gap.

The comparison between a representative set of experimental data and the corresponding simulation results is shown in Fig. 2. The model is able to closely reproduce the transfer characteristics of the prototype, with a maximum deviation of approximately 0.8% over a V_G window of more than 7 V in the above-the-threshold region [panel (a)]. The small difference is likely related to a slight overestimation of the transmission at large gate overdrives. The deviations in the subthreshold region are due to the simplified approximation of uniform trap density, which results in a trade-off between matching the current in the weak inversion or in the deep subthreshold region. We choose to privilege the first option, as the weak inversion condition is more likely attained during the operation of transistors. This also requires the assumption of a smaller density of trap states with respect to the estimate in Ref. [10].

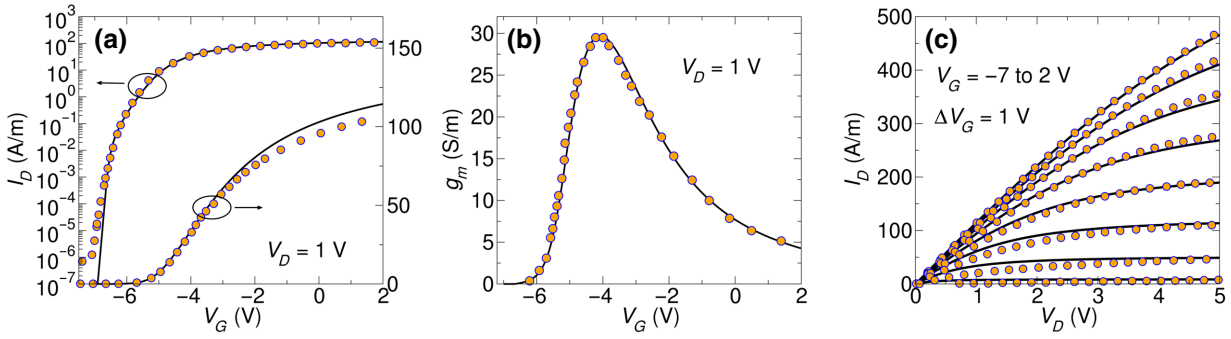

FIG. 2. Comparison between experimental data from Ref. [10] (circles) and simulations (lines). (a) Transfer characteristics at $V_D = 1$ V, (b) transconductance at $V_D = 1$ V, and (c) output characteristics of the transistor for V_G from −7 to 2 V in steps of 1 V.

The quality of the fit is further confirmed by the excellent agreement in terms of the transconductance as a function of V_G [panel (b)] and of the output characteristics, over a V_D window of 5 V [panel (c)].

B. Figures of merit and performance analysis

In this section we assess the performance of the device and we project them for future stages of the technological evolution of TFTs. We consider both a geometrical scaling and the improvement of the manufacturing processes, which could lead to a reduction of the value of the contact resistance and of the density of traps.

In order to provide a comprehensive analysis of device potential, we consider a set of figures of merit pertaining to different possible technological applications, for which TFTs have been envisaged or are already used. The device is studied in terms of the on current (I_{on}), of the intrinsic delay time (τ), of the power-delay product (PDP) and of the cut-off frequency (f_t).

The on current is a good indicator of the capability of the device in driving displays, the most common and already established at industry-level application of TFTs. τ and PDP more specifically refer to digital applications, while f_t is used to characterize the device for radiofrequency applications.

In order to provide a comparison with other proposed devices for the same source-to-drain bias, we consider in simulations $V_D = 1$ V and $V_D = 5$ V, two typical values for which measurements are available in the literature. I_{on}, τ, and PDP are evaluated by assuming a supply voltage V_{DD} (the highest voltage at which the gate can be raised) equal to V_D. Moreover, we set the current in the device off state to $I_{off} = 10^{-5}$ A/m, a value typically above the leakage currents in experiments and compatible with low-power applications.

In order to avoid short channel effects, we restrict ourselves to consider a set of geometrical parameters for which the ratio L_G/ℓ_n between the channel length and the so-called natural length $\ell_n \equiv \sqrt{\epsilon_{ch} t_{ch}/C_{ox}}$, where $\epsilon_{ch} = 20$ is the dielectric constant of La-$BaSnO_3$, is larger than 5. This value has been proposed as an empirical estimate of the minimum L_G/ℓ_n ratio for which a long-channel behavior is observable [25,26].

Finally, the minimum channel length considered is $L_G = 40$ nm. While this value appears far from the supermicron size of TFTs currently used in commercial applications, it is worth mentioning that no fundamental difficulties hinder the downscaling of TFTs and that devices with significantly shorter channels have already been demonstrated [27].

1. On current

I_{on} is computed as the current flowing in the device at $V_G = V_G^{off} + V_{DD}$, where V_G^{off} is the gate voltage at which $I_D = I_{off}$. In practice, V_G^{off} can be tuned to zero by choosing for the gate contact a metal with the proper work function.

In Fig. 3, the values of I_{on} obtained for different L_G and t_{ox} are plotted as a function of C_{ox}/L_G in the cases $V_{DD} = 1$ V and $V_{DD} = 5$ V. They are compared against a set of I_{on} values extracted from the literature (Refs. [28–63]), corresponding to TFTs with the channel made in different materials. The extraction of the values of I_{on} from other works has been performed directly from the transfer characteristics of the devices, according to the definition of I_{on} provided above. We notice that the difference in contact resistances and trap density between different prototypes can partially mask the intrinsic performance of devices. However, the proposed benchmark can still provide a good indication of the performance spectrum and of the maximum achieved performance of a given family of devices.

According to the available data, the device proves competitive with all the considered technologies, and, particularly, with the much more mature, mainstream *a*-IGZO technology.

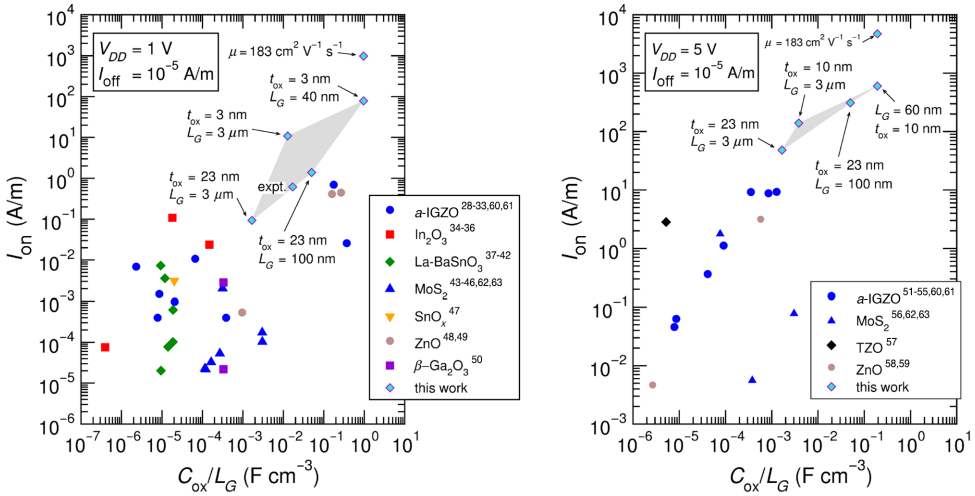

FIG. 3. I_{on} as a function of the ratio C_{ox}/L_G at $V_{DD} = 1$ V (left) and $V_{DD} = 5$ V (right). Symbols refer to transistors reported in the literature with channels realized in different materials and for which measurements at the same $V_D = V_{DD}$ are available. Refs. [28–63] in the legends refer to the papers from which the corresponding data are extracted. The label "expt." in the left panel indicates the point corresponding to the experimental configuration of Ref. [10].

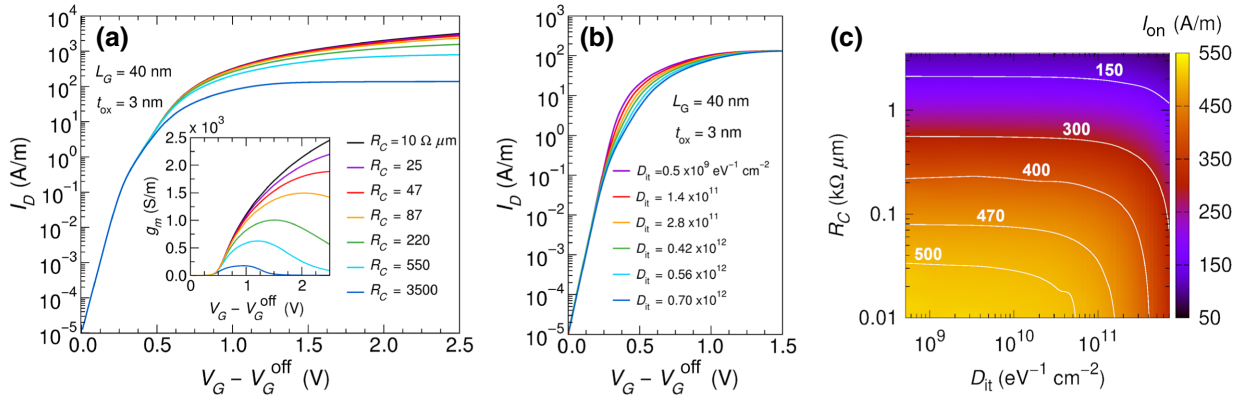

FIG. 4. (a) Transfer characteristics at $D_{it} = 0.70 \times 10^{12}$ eV^{-1} cm^{-2} and different values of R_C. Inset: transconductance extracted from the transfer characteristics in the main panel. (b) Transfer characteristics at $R_C = 3.5$ kΩ μm and for different values of D_{it}. (c) Colormap of the on current as a function of R_C and D_{it}. For all the panels, $L_G = 40$ nm, $t_{ox} = 3$ nm, and $V_D = V_{DD} = 1$ V.

The evolution of the transfer characteristics as the contact resistance and the density of traps are reduced below the calibration values of Table I is shown in Fig. 4 for $L_G = 40$ nm and $t_{ox} = 3$ nm. Panel (a) shows that the value of the contact resistance influences the transfer characteristics only above the threshold voltage. Particularly, a reduction of R_C results in an increase of the transconductance [inset of panel (a)], which, in turn, entails an increase of the current delivered by the transistor.

Reducing the density of traps mainly affects the subthreshold region of the transfer characteristics [panel (b)], by improving the subthreshold swing for $I_D \gtrsim 10^{-2}$ A/m. The combined effect of a reduction of both R_C and D_{it} on the on current can be evaluated from the colormap shown in panel (c). I_{on} begins to saturates at values in excess of 450 A/m, for $R_C < 150$ Ω μm and $D_{it} < 0.75 \times 10^{11}$ eV^{-1} cm^{-2}, which corresponds to an improvement of about one order of magnitude with respect to the case in which R_C and D_{it} are set to the calibration values.

2. Intrinsic delay time and power-delay product

τ and PDP are computed in a quasistatic approximation [64], according to the equations:

$$\tau = \frac{Q_{on} - Q_{off}}{I_{on}}, \tag{11}$$

$$\mathrm{PDP} = (Q_{on} - Q_{off}) V_{DD}, \tag{12}$$

where Q_{on} and Q_{off} are the total charge in the channel in the on and off states, respectively. Since our model is not able to account for the dynamic of carrier trapping and detrapping, which affect the considered figures of merit and likely preclude the use of these devices in high-speed digital and communication circuits, we refer to the optimistic scenario in which an improved fabrication technology is able to strongly suppress such trap concentration. Accordingly, we perform the simulations by assuming $D_{it} = 0$.

The colormaps in panels (a) and (b) of Fig. 5 show the behavior of τ and PDP when $t_{ox} = 3$ nm and R_C and L_G are reduced with respect to the calibration values of Table I.

τ can be reduced by decreasing both R_C and L_G. In the first case, the reduction is driven by the increase of I_{on} discussed in the previous section. In the second, it is also contributed by the decrease of $Q_{on} \approx C_{ox} L_G V_{DD}$. Downscaling L_G turns out to be by far the most effective option, resulting in an improvement of τ by about 2 orders of magnitude when L_G is reduced from 295 to 40 nm. Values of τ as small as 1.8 ps appear within reach of the considered TFT when the channel is scaled down to 40 nm, the contact resistance is reduced to 100 Ω μm and the effect of traps is negligible.

The value of PDP shows only a weak dependence on R_C. It is mainly controlled by L_G, which directly influences Q_{on} through the total geometrical gate capacitance, as already discussed in the case of the intrinsic delay time. PDP values of the order of 1 fJ/μm can in principle be obtained for $L_G = 40$ nm, corresponding to an improvement by a factor of approximately 7 with respect to $L_G = 295$ nm.

3. Cut-off frequency

The cut-off frequency is evaluated through the expression [64]

$$f_t = \max_{I_D}\left(\frac{1}{2\pi}\frac{\partial I_D}{\partial (q n_s)}\right) = \max_{I_D}\left(\frac{g_m}{2\pi C_G}\right), \tag{13}$$

where $C_G = \partial(q n_s)/\partial V_G$ is the total capacitance seen from the gate.

Panel (c) of Fig. 5 shows a colormap of the cut-off frequency in the L_G-R_C plane for $t_{ox} = 3$ nm and $V_D = 1$ V. The simulation is performed in the absence of traps, since the trapping and detrapping processes predominantly occur below or close to the threshold voltage and no appreciable dependence of f_t on D_{it} is expected.

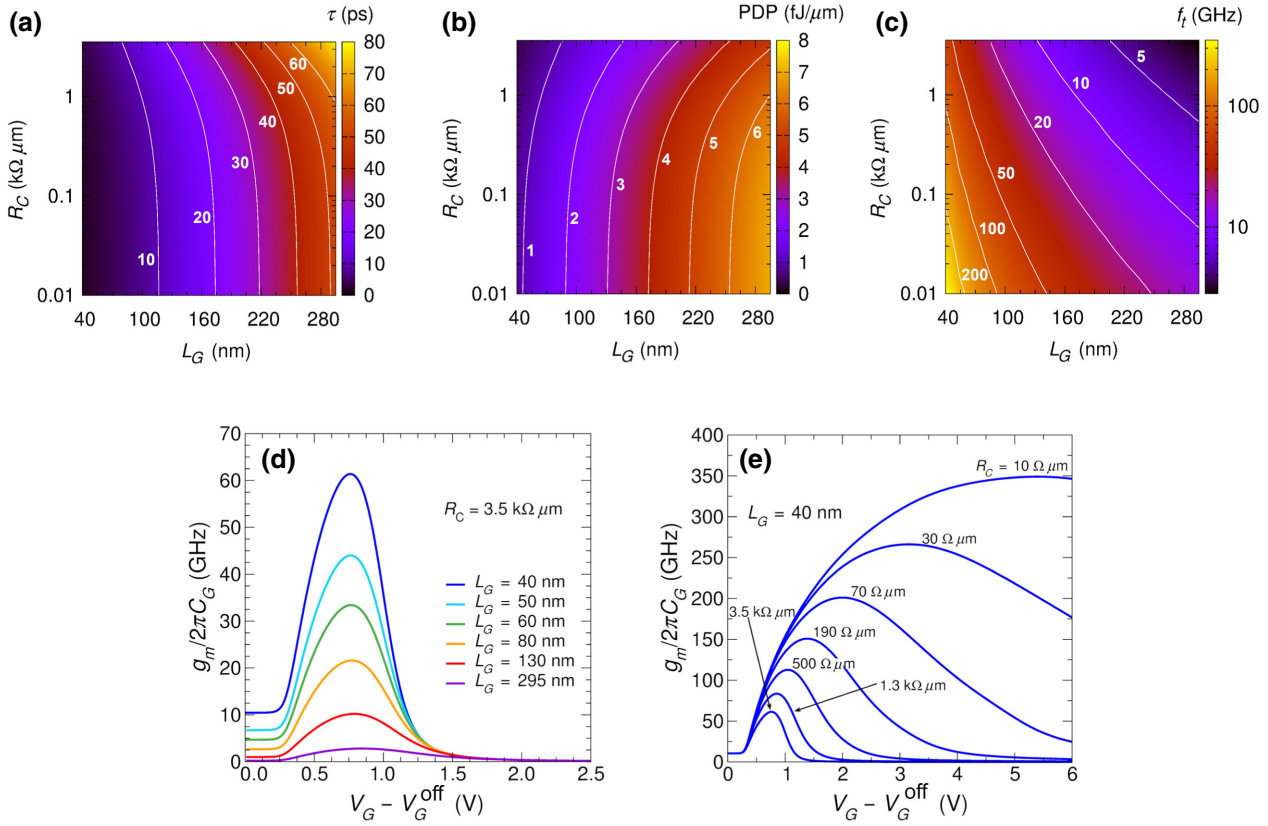

FIG. 5. Colormaps of (a) intrinsic delay time, (b) power-delay product, and (c) cut-off frequency as a function of R_C and L_G. (d) $g_m/2\pi C_G$ as a function of V_G at $R_C = 3.5$ kΩ μm and for different values of L_G. (e) $g_m/2\pi C_G$ as a function of V_G, at $L_G = 40$ nm and for different values of R_C. For all the panels $t_{ox} = 3$ nm, $D_{it} = 0$, and $V_D = V_{DD} = 1$ V.

f_t depends on R_C essentially through the transconductance, according to the rightmost side of Eq. (13). The increase of f_t as R_C is reduced just reflects the concomitant increase of the peak of g_m [cf. inset of Fig. 4(a)]. On the other hand, the increase of f_t for decreasing L_G derives both from an increase of g_m and from a reduction of the geometrical component of C_G. A cut-off frequency higher than 2 GHz appears achievable for all the considered channel lengths, provided that R_C is small enough. Instead, f_t beyond 100 GHz can only be obtained at channel lengths shorter than 90 nm.

Panels (d) and (e) of Fig. 5 illustrate the effect of the reduction of L_G and R_C on the behavior of $g_m/2\pi C_G$ as a function of V_G. It can be noticed that the gate overdrive voltage at which the peak of $g_m/2\pi C_G$ (namely f_t) occurs, has a very weak dependence on L_G. In contrast, as R_C decreases, a larger gate overdrive is needed in order to achieve the maximum $g_m/2\pi C_G$ and fully exploit the device potential for high-frequency applications.

IV. DISCUSSION AND CONCLUSION

Device modeling clearly shows that the performance of La-$BaSnO_3$-based TFTs is strongly limited by geometrical constraints and nonidealities, and that large improvements can be obtained if material quality is ameliorated (in terms of trap-density suppression and mobility enhancement), contact resistance is reduced and geometry is optimized. Suppression of trap density is needed to obtain competitive dynamical figures of merit. Geometry downscaling provides a most effective and all-encompassing approach to significantly improve both static and dynamic figures of merit, provided that short-channel effects are kept under control. On one hand, improvements of I_{on} by more than 2 orders of magnitude with respect to the values measured in the reference experimental prototype, appear achievable through a joint scaling of L_G and t_{ox}. On the other, a reduction of L_G from 295 to 40 nm results in an improvement by around one order of magnitude of all the considered dynamical figures of merit, even for an already highly scaled t_{ox} of 3 nm. Reducing the contact resistance to 100 Ω μm and below provides a further boost of a factor between 3 and 5 on I_{on} and f_t.

Further increasing the device performance beyond these limits requires an enhancement of channel mobility. This appears possible after improving the manufacturing processes, in the light of the higher mobility of 183 $cm^2\ V^{-1}\ s^{-1}$ already reported for unpatterned La-$BaSnO_3$ thin films [7]. The opportunity to benefit from such high mobility represents a distinct

TABLE II. Figures of merit computed by assuming $\mu_n = 183$ cm^2 V^{-1} s^{-1} and for the most scaled devices considered ($L_G = 40$ nm and $t_{ox} = 3$ nm for $V_{DD} = 1$ V, $L_G = 60$ nm and $t_{ox} = 10$ nm for $V_{DD} = 5$ V). The contact resistance and the density of traps are set to $R_C = 100$ Ω μm and $D_{it} = 0$, respectively.

Figure of merit	V_{DD} (V)	Value
I_{on} (A/m)	1	783
I_{on} (A/m)	5	4165
τ (ps)	1	0.88
PDP (fJ/μm)	1	0.69
f_t (GHz)	1	315

advantage of La-$BaSnO_3$-based TFTs with respect to the mainstream *a*-IGZO technology, for which achievable mobilities are limited to around 10 cm^2 V^{-1} s^{-1} [5]. For instance, by assuming for the mobility a value of $\mu_n = 183$ cm^2 V^{-1} s^{-1}, and assuming $R_C = 100$ Ω μm, I_{on} increases by more than one order of magnitude (up to approximately 800 A/m at $V_{DD} = 1$ V, $t_{ox} = 3$ nm, and $L_G = 40$ nm, and up to approximately 4.2×10^3 A/m at $V_{DD} = 5$ V, $t_{ox} = 10$ nm, and $L_G = 60$ nm) with respect to the value achieved by a pure geometrical scaling. (see Fig. 3). Concerning the dynamical figures of merit, values of 0.88 ps, 0.69 fJ/um, and 315 GHz can be estimated, in the same conditions, for τ, PDP, and f_t, respectively. These values, that could be expected close to the upper limit of achievable performance, are collected in Table II. They suggest that La-$BaSnO_3$-based TFTs are promising candidates for high-performance active display applications, and also to add sophisticated computation and communication capabilities to flexible or transparent electronic systems, such as radiofrequency communication capabilities in the GHz range, compatible with WiFi and Bluetooth protocols, or complex machine-learning capabilities for intelligent sensors, so far precluded to TFTs.

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APPENDIX

Following Ref. [65], in the expression of transmission,

$$\mathcal{T}(E) = \frac{\lambda(E)}{\lambda(E) + l_c},$$

we approximate $\lambda(E)$ with its average over the direction in the x-z plane and over the energy:

$$\langle\lambda\rangle = \frac{2kT\mu_n}{qv_T},$$

where μ_n is the electron mobility, k the Boltzmann constant, T the room temperature, and $v_T = \sqrt{2kT/q\pi m^*}$ is the thermal velocity. The critical length is modeled by assuming a drift-diffusion approximation of transport and a gradual channel approximation [66], according to the following expression [65]:

$$\ell_c = \frac{2L_G}{\left(\frac{V_1}{kT/q}\right)(1-\eta^2)}\left[\exp\left(\frac{V_1}{kT/q}(\eta-1)\right) \times \left(1-\eta\frac{V_1}{kT/q}\right) - \left(1-\frac{V_1}{kT/q}\right)\right], \quad \text{(A1)}$$

where

$$V_1 \equiv \frac{2qn_s/C_{ox}}{1+\sqrt{2qn_s/(C_{ox}L_G E_{crit})}},$$

and

$$\eta \equiv 1 - \frac{(V_{D'}/V_1)}{[1+(V_{D'}/V_1)^\beta]^{1/\beta}}.$$

In the equations for V_1 and η, $E_{crit} \equiv v_T/\mu_n$ is the critical electric field for velocity saturation, and β is an empirical parameter, which is set to 1 throughout the paper. The hypothesis of diffusive transport, requiring $L_G > \langle\lambda\rangle$, is checked to be fulfilled in all the cases considered in the paper.

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