Electrical Properties of Selective-Area-Grown Superconductor-Semiconductor Hybrid Structures on Silicon

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We present a superconductor-semiconductor materials system that is both scalable and monolithically integrated on a silicon substrate. It uses selective-area growth of Al-InAs hybrid structures on a planar III-V buffer layer, grown directly on a high-resistivity silicon substrate. We characterize the electrical properties of this materials system at millikelvin temperatures and observe a high average field-effect mobility of $\mu \approx 3200$ cm^2/Vs for the InAs channel and a hard induced superconducting gap. Josephson junctions exhibit a high interface transmission, $\mathcal{T} \approx 0.75$, a gate-voltage-tunable switching current with a product of critical current and normal state resistance, $I_C R_N \approx 83$ μV, and signatures of multiple Andreev reflections. These results pave the way for scalable and high-coherence gate-voltage-tunable transmon devices and other superconductor-semiconductor hybrids fabricated directly on silicon.

I. INTRODUCTION

Recent demonstrations of superconducting qubit systems with over 50 qubits place superconducting qubits as the most advanced approach to building a quantum computer [1]. However, practically useful fault-tolerant quantum computers may require several orders of magnitude more qubits, all operating with high fidelity at millikelvin temperatures [2]. This substantial challenge of scaling superconducting qubit systems motivates the exploration of materials platforms that might provide readily extensible approaches to qubit control [3]. In particular, recent work has demonstrated that semiconductor elements can be incorporated into superconducting systems to create superconducting qubits with gate-voltage-tunable Josephson junctions (JJs) [4–6]. This semiconductor-based JJ technology has the potential to enable superconducting qubits to naturally interface with ultralow-power cryogenic CMOS control [7].

So far, approaches to building semiconductor-based superconducting transmon qubits, known as gatemons, have either proven challenging to scale in the case of vapor-liquid-solid- (VLS) nanowire-based qubits [4] or

have had coherence times that are limited by losses in the underlying III-V substrate in the case of two-dimensional-electron-gas-based gatemons [5]. In this work, we present a materials system that brings together the salient features of these earlier approaches by using deterministic selective-area growth of Al-InAs hybrid structures [8] on a low-loss Si substrate. We study the electrical properties of this hybrid system with respect to the requirements for gatemon qubits. In particular, disorder both within the semiconductor JJ channel and at the superconductor-semiconductor interface can lead to subgap states that can act as an additional decoherence channel for the qubit [9,10]. We focus on the hybrid Al-InAs system as the basis for our semiconductor JJs. InAs supports high-mobility transport and the epitaxial combination of Al and InAs has been shown to form a high-quality high-transparency superconductor-semiconductor interface [9] along with the highest coherence gatemon devices [11,12]. We integrate these materials on a Si platform that has been shown to support high-coherence superconducting qubits [13,14] and offers compatibility with silicon CMOS technology.

In order to characterize our system, first, we extract mobilities for the semiconductor channel using field-effect-transistor (FET) devices. Next, we probe the superconductor-semiconductor interface quality through

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transport spectroscopy of normal-conductor–insulator–superconductor (N-I-S') junctions, where in this case the superconductor is the proximitized semiconductor (S'). Finally, we characterize the quality of JJs in our materials system by extracting the $I_C R_N$ product (where I_C and R_N are the JJ critical current and normal state resistance) and the junction transparency.

II. MATERIAL STACK AND DEVICES

Figure 1 shows the material stack that is studied in this work. It is grown on a 4° miscut (111)-Si substrate with resistivity $\rho > 1\,\mathrm{k\Omega}\,\mathrm{cm}$. To grow the high-quality InAs layer, GaAs/GaP/Si substrates consisting of buffer layers of approximately 50 nm of GaP and approximately 250 nm of GaAs are used. These buffers are deposited using metal-organic chemical-vapor deposition (MOCVD) techniques and are commercially available [15]. The GaP-on-Si buffer technique enables antiphase defect-free growth of III-V materials on nonpolar Si substrate [16]. The GaAs buffer serves multiple purposes. First, it reduces the lattice mismatch between the InAs and the Si (from 11.4% to 7.2%). Second, it provides a smooth and high-surface-quality virtual GaAs substrate on which high-quality in-plane InAs nanowires can be grown using selective-area growth (SAG) techniques [8]. Third, owing to its large band gap, it provides a good electrical isolation between the InAs nanowires and the Si substrate. The total thickness of the GaP/GaAs buffer stack is limited to approximately 300 nm to simplify integration of our superconductor-semiconductor materials system with any low-loss qubit circuit components that are fabricated directly on the underlying Si substrate.

We use SAG techniques [8] to grow InAs structures shaped as planar nanowires on the GaAs surface. Thin films of AlO_x and SiO_x are deposited on the wafer using atomic layer deposition and plasma-enhanced chemical-vapor deposition, respectively. Openings in these dielectric

layers are then defined by standard electron-beam lithography and selective etching of the SiO_x and AlO_x using reactive-ion etching and a wet-etch solution, respectively. The subsequent growth steps take place by molecular-beam epitaxy (MBE) in ultrahigh vacuum prepared with high-purity processes [17] and the semiconductor heterostructures are then grown selectively in the dielectric openings where the GaAs surface is exposed. The SAG heterostructure is designed to increase the interface quality between the GaAs and InAs layers in order to improve the overall InAs material quality. First, an Sb-dilute GaAs buffer layer with flat top facets is grown. This layer enables significant elastic strain relaxation of the InAs [8]. Then, a layer of $\mathrm{In}_{0.8}\mathrm{Ga}_{0.2}\mathrm{As}$ is grown to bridge the lattice mismatch to the InAs. To help prevent surface damage from subsequent device processing steps from impacting the transport characteristics, a top barrier layer of $\mathrm{In}_{0.8}\mathrm{Ga}_{0.2}\mathrm{As}$ is grown on the InAs. Finally, a blanket Al layer is deposited *in situ* [18] to ensure a high-quality interface between the Al and the semiconductor heterostructure. A false-colored scanning transmission electron microscope image of the top part of the material stack is shown in Fig. 1(b).

We fabricate three different types of devices to study the properties of our materials system: FETs, N-I-S' junctions, and superconductor-semiconductor-superconductor Josephson junctions (S-Sm-S JJs) (Fig. 2). All devices
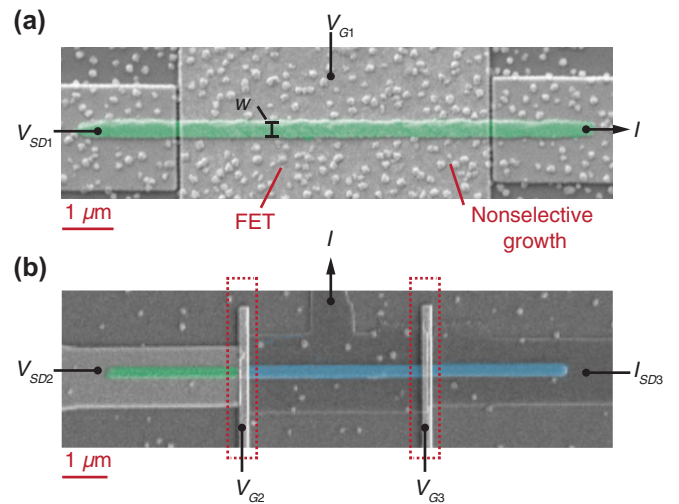
FIG. 2. False-colored scanning electron micrographs of the device types measured in this work. The false colors indicate nanowire segments with Al removed (green) and segments covered with Al (blue). (a) The field-effect transistor (FET) device. (b) The combined N-I-S' spectroscopy and S-Sm-S JJ device. The middle segment serves as ground for both N-I-S' spectroscopy and junction measurements. On some wafers, poor selectivity during SAG leads to material deposition on the oxide mask [19], which is visible as small grains in both SEMs.
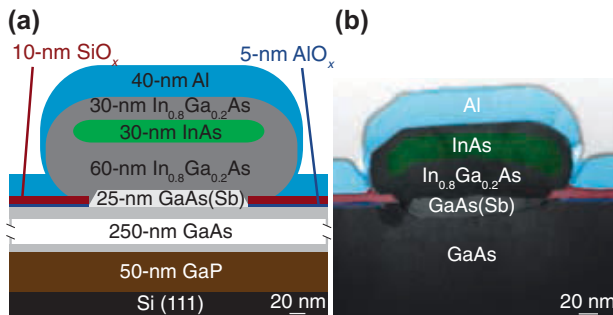
FIG. 1. (a) A schematic of the material stack. The InAs quantum well (green) is proximitized by the superconducting Al (blue). (b) A false-colored scanning transmission electron micrograph of the material stack.

are fabricated together on a single substrate. The substrate is then cleaved into two device dies, with one die containing all the FET devices and the other die containing all the superconducting devices, which are loaded separately for electrical measurements. *N-I-S'* and *S-Sm-S* JJ devices are used to study the superconductor-semiconductor hybrid system. They are fabricated in pairs using a single nanowire such that both devices share a common superconducting segment [Fig. 2(b)]. This is achieved by selectively etching the Al layer and depositing a normal-metal contact. The semiconducting segments are tuned by top gates, separated from the nanowire by gate dielectric.

The FET devices are used to study the material quality of the conducting InAs layer exclusively. To fabricate these devices, we use standard electron-beam lithography. In a first step, Al is removed from the nanowires by selective wet etching. Subsequently, contacts, gate dielectric, and a top gate are deposited. The length of the gated channel for all devices shown in this work is $L_{\mathrm{FET}} = 6 \ \mu$m. All measurements in this work are performed at 20 mK unless stated otherwise.

In this work, we study a total of 24 FET devices and six superconducting devices (see Table S1 of the Supplemental Material [20]). Appendix A contains additional device-fabrication details and further information about all the devices; in particular, the superconducting nanowires A, B, and C, which are studied in Secs. IV–VI.

III. FIELD-EFFECT MEASUREMENTS

A typical figure of merit for the quality of a semiconductor is the field-effect mobility, as it is limited by defects in the semiconductor, gate dielectric layers, and interfaces [21]. The field-effect mobility can be extracted from the transconductance dG/dV_{G1}, which we obtain from measurements of the differential conductance G as a function of the gate voltage V_{G1} for a total of 24 FET devices [similar to the one represented in Fig. 2(a)], using standard lock-in techniques. The measured nanowires were grown along the $[\bar{1}\bar{1}2]$, $[1\bar{1}0]$ directions of the underlying Si substrate and 45° in relation to them (Fig. 3 inset).

Figure 3 shows typical differential-conductance measurements sweeping V_{G1} in both positive and negative directions. Nanowires for all different orientations can be fully pinched off and show a small hysteresis of approximately 0.05 V, indicating high-quality interfaces between the electrically active InAs channel and the adjacent layers [8]. As depicted in Fig. 3, the mean field-effect mobility μ is extracted from a fit to the linear region of the conductance with the highest slope [22]. It can be estimated by

$$\left. \frac{dG}{dV_{G1}} \right|_{\max} = \frac{\mu C_G}{L_{\mathrm{FET}}^2}, \tag{1}$$
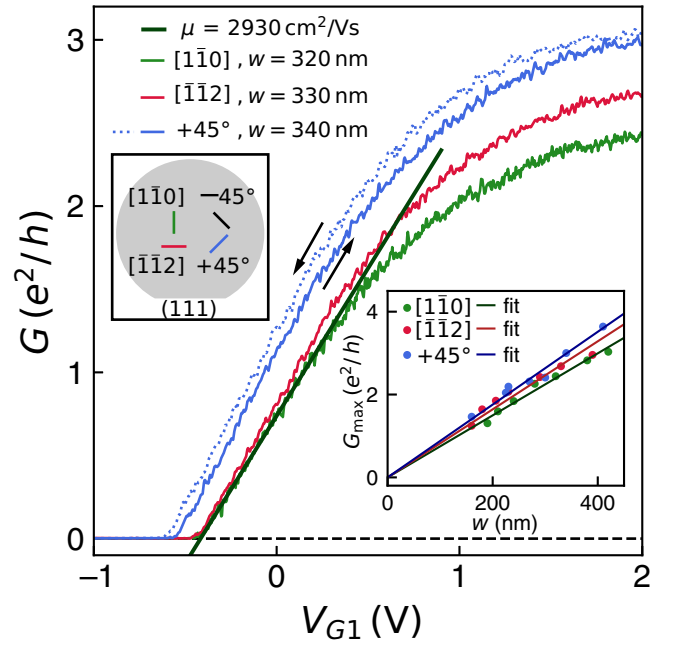

FIG. 3. The differential conductance G as a function of the gate voltage V_{G1} of an up and down sweep of a single nanowire (blue) and up sweeps of two nanowires with a different orientation and similar width w. A fit to the linear region of the green pinch-off curve is shown and used to determine the field-effect mobility according to Eq. (1). Upper left inset: a schematic showing the orientation of the nanowires relative to the major flat of the Si substrate. Lower right inset: the conductance in the fully open regime as a function of w. Solid lines indicate fits of the form $G_{\max} = g'w$, where g' is the conductance per unit width of the nanowires in the fully opened regime. All the data shown in this figure are corrected for a line resistance $R_{\mathrm{line}} = 4.9 \ \mathrm{k\Omega}$.

where $L_{\mathrm{FET}} = 6 \ \mu$m is the length of the gated channel and C_G is the gate capacitance, which is estimated from finite-element simulations (see Sec. I of the Supplemental Material [20]). The extracted averaged value for all devices is $\mu_{\mathrm{avg}} = (3200 \pm 300) \ \mathrm{cm}^2/\mathrm{Vs}$. Here, the uncertainty of the simulated capacitance is neglected and the given error is the statistical error of all measured devices, where up and down sweeps of the same device are considered to be two independent measurements. The value μ_{avg} is comparable but lower than values reported for InAs SAG nanowires grown directly on GaAs [8] and InAs VLS nanowires that are grown strain relaxation free [23,24]. Previous work has shown that the low-temperature field-effect mobility of undoped III-V nanowires is typically limited by crystal defects [23,25,26] or surface effects [24,25]. Further work will be needed to understand the dominant electron scattering mechanism in our material stack in order to further optimize the field-effect mobility. Based on the threshold voltages V_{th} and the volume of the conducting channel v_{ch} (Fig. 1), we estimate a mean carrier density at zero gate voltage using $n = C_G V_{\mathrm{th}}/(ev_{\mathrm{ch}})$. For the different nanowire

orientations, we estimate $n_{[1\bar{1}0]} = 3.0 \cdot 10^{17}\,\mathrm{cm}^{-3}$, $n_{[\bar{1}\bar{1}2]} = 3.4 \cdot 10^{17}\,\mathrm{cm}^{-3}$, and $n_{[+45°]} = 4.8 \cdot 10^{17}\,\mathrm{cm}^{-3}$. Nanowires rotated $+45°$ relative to the $[\bar{1}\bar{1}2]$ direction exhibit the highest charge-carrier density (the lowest V_{th}) and the highest conductance when the conducting channel is fully opened (for gate voltages $V_{G1} > 2$ V) (Fig. 3, lower inset).

IV. INDUCED SUPERCONDUCTING GAP

The quality of the superconductor-semiconductor interface has been shown to influence the hardness of the induced superconducting gap in a proximitized semiconductor [9]. To study the interface quality between the superconducting Al and InAs and the induced superconducting gap Δ^* in the InAs, we use the N-I-S' device introduced previously in Fig. 2(b) and fabricated on nanowire A. The device is measured with standard lock-in techniques with unused contacts left floating, so that the third segment on the nanowire does not affect the measurement. As shown in Fig. 4(a), we deplete the bare InAs segment by applying a negative gate voltage V_{G2} to create a tunnel barrier and measure the differential conductance G of the device as a function of the voltage bias V_{SD2}.

Figure 4(b) (red curve) shows a measurement in the tunneling regime. The conductance G is strongly suppressed between two symmetric peaks. The peak positions are independent of the gate voltage and indicate an induced
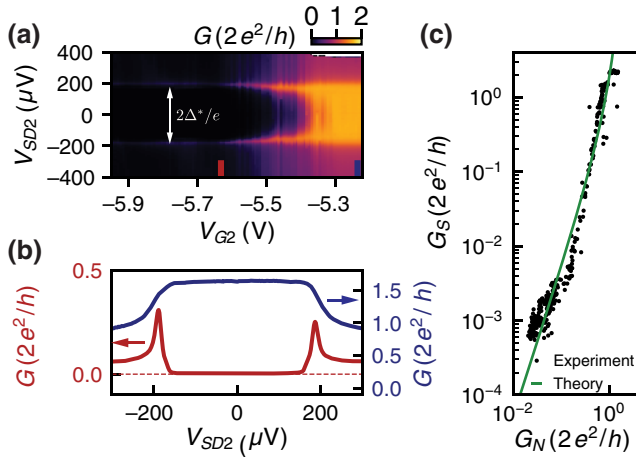

gap $\Delta^* \approx 190\ \mu\mathrm{eV}$ [see Fig. 4(a)]. At higher V_{G2} (a more open barrier), the subgap conductance G_S (measured at $V_{SD2} = 0$ V) is increased compared to the above-gap conductance G_N for $|V_{SD2}| \gtrsim 200\ \mu\mathrm{eV}$ (Fig. 4(b), blue curve). Both observations, the suppressed ($G_S \ll G_N$) and the enhanced zero-bias conductance ($G_S > G_N$), can be explained in the framework of the Blonder-Tinkham-Klapwijk (BTK) formalism [27]. This theory describes the charge transfer through a N-S interface by Andreev reflection using a single parameter, the dimensionless barrier parameter Z. The limit $Z = 0$ corresponds to a perfect interface where $G_S = 2G_N$ is expected as every charge carrier is Andreev reflected at the interface. The limit $Z \to \infty$ corresponds to a perfect tunnel barrier where the conductance is directly proportional to the density of states in the proximitized region. Thus, changing V_{G2} in the experiment corresponds to modifying the Z parameter. To further study the transport across the NS interface, we compare the experiment to

$$G_S = 2G_0 \frac{G_N^2}{(2G_0 - G_N)^2}, \qquad (2)$$

the theoretical prediction for a quantum point contact (QPC) with a single channel that correlates G_S to G_N [28] without any free parameters and with $G_0 = 2e^2/h$. The measurement is repeated on the same nanowire using a dc setup to measure small differential-conductance values ($G_S < 10^{-2}\ e^2/h$). Here, the differential resistance is obtained from calculating the numerical derivative of the dc data (see Sec. IIA of the Supplemental Material [20]). The result is shown in Fig. S4 of the Supplemental Material [20] and is used to construct Fig. 4(c). The experimental data follow the theoretical prediction [the green line in Fig. 4(c)]. We therefore conclude the presence of an induced hard superconducting gap in the InAs. The small deviation could be the manifestation of a nonzero normal scattering probability or the presence of multiple conducting channels with a transmission probability below 1. The presence of multiple conducting channels is evident in the plateau region (see Fig. S4d of the Supplemental Material [20]) with enhanced zero-bias conductance, G_N [$V_{G2} > -5.3$ V in Fig. 4(a)], which is not quantized at $2e^2/h$, contrary to the expectations for a single perfectly transmitting channel. While Eq. (2) is for the single-channel limit, it is commonly used to assess the hardness of the induced superconducting gap in hybrid systems [9,29].

V. NANOWIRE JOSEPHSON JUNCTIONS

We use the S-Sm-S JJ device [Fig. 2(b)] to study the JJ formed in the materials system. We characterize the junction by extracting several junction parameters, the switching current, I_{sw}, the retrapping current, I_R, the excess current I_{exc}, the normal state resistance R_N, and the superconducting gap Δ as a function of the gate voltage V_{G3} and

FIG. 4. (a) The differential conductance dI/dV of nanowire A as a function of the gate voltage V_{G2} and the source-drain voltage V_{SD}. (b) Vertical cuts in the tunneling regime (red) and in the open regime (blue) at the positions indicated by the colored rectangles in (a). The induced superconducting gap $\Delta^* \approx 190\ \mu\mathrm{eV}$ is estimated from the peak-to-peak distance in the tunneling regime. (c) The averaged differential conductance at zero source-drain voltage G_S versus the averaged differential conductance at finite source-drain voltage G_N (V_{SD2}) $= -0.53$ mV based on the data set in Fig. S4a of the Supplemental Material [20]. The green line is the theoretically predicted conductance in an Andreev-enhanced QPC with no fitting parameters [Eq. (2)].

temperature T. All parameters are extracted as shown in Fig. 5(a) for a typical I-V curve. The junction switches to a dissipative state at switching current I_{sw} as the bias current, I_{SD3}, is swept from zero. Sweeping I_{SD3} back toward zero, the junction switches back to the superconducting state at the retrapping current, I_R, visible as hysteretic behavior [Fig. 5(a), inset]. The normal state resistance,

R_N, and the excess current, I_{exc}, are extracted at high current bias, where $V_{SD3} > 2\Delta/e$ and the junction is driven into the normal conducting state. We estimate the superconducting gap, $\Delta \approx 200$ μeV, from the visible transition to the normal conducting state. This value is similar to the estimated induced superconducting gap of the S'-I-N device, $\Delta^* \approx 190$ μeV. The critical current is gate tunable, as demonstrated by Fig. 5(b), where the differential resistance dV/dI is shown as a function of the applied current I_{SD3} and the gate voltage V_{G3}. Furthermore, the I-V curves exhibit subgap features in the resistive state for $V_{SD3} < 2\Delta/e$ that result from multiple Andreev reflections (MARs) [30,31], discussed in the next section. Figure 5(c) shows the extracted junction parameters for nanowire B over a wide gate range from $V_{G3} = -0.3$ V, where the nanowire junction is almost closed ($I_{sw} \approx 0$ nA), to $V_{G3} = 1.5$ V, where the junction is fully opened. While $I_{sw}/I_R \approx 1.0$ in the closed regime, we find ratios $I_{sw}/I_R \approx 2.0$ for gate voltages around $V_{G3} = 1.5$ V, indicating that the nanowire junction may be underdamped [32]. This hysteresis may also be caused by self-heating of the junction when it exits the superconducting state [33].

To further characterize the JJ and its superconductor-semiconductor interface quality, we extract the product $I_{sw}R_N$ and the normalized excess current $eI_{exc}R_N/\Delta$ [30] [Fig. 5(d)]. Here, we use I_{sw} as a proxy for the critical current, I_C, noting that the measured switching current can be smaller than the actual critical current of the junction due to premature switching [32] or coupling to the electromagnetic environment [34]. The normalized excess current $eI_{exc}R_N/\Delta$ is used to estimate the BTK barrier parameter Z for N-S interface scattering [27] and is connected to the interface transmission $\mathcal{T} = (1 + Z^2)^{-1}$. Hence, a high value of $\mathcal{T}$ is an indication of a high superconductor-semiconductor interface quality. For $V_{G3} > 0.1$ V, we extract an averaged excess current $eI_{exc}R_N/\Delta = 0.99 \pm 0.15$ and estimate $Z = 0.58 \pm 0.06$ [35], leading to $\mathcal{T} = 0.75 \pm 0.04$. A high transparency is consistent with the enhanced zero-bias conductance observed with tunneling spectroscopy and with the relatively high value of the induced superconducting gap in the InAs compared to the Al gap [27,30]. For $V_{G3} < 0$ V, $I_{sw}R_N$ is reduced and the spread in $eI_{exc}R_N/\Delta$ increases. For $V_{G3} < -0.35$ V, negative and positive values for I_{exc} are extracted. Similar observations have previously been explained by quantum dots forming in the junction, which causes the transport to be dominated by an interplay between superconductivity and Coulomb interactions [36, 37]. The extracted average value $I_{sw}R_N = (83.3 \pm 5.8)\mu$V is significantly smaller than the theoretical value for a short diffusive junction $I_C R_N = 1.32\pi\Delta/2e \approx 415$ μV [38] but in good agreement with values previously measured in Al-InAs VLS nanowires [21,39–41] and other superconductor-semiconductor hybrid systems [34,42,43]. Similar to previous studies, the origin of a low-$I_{sw}R_N$
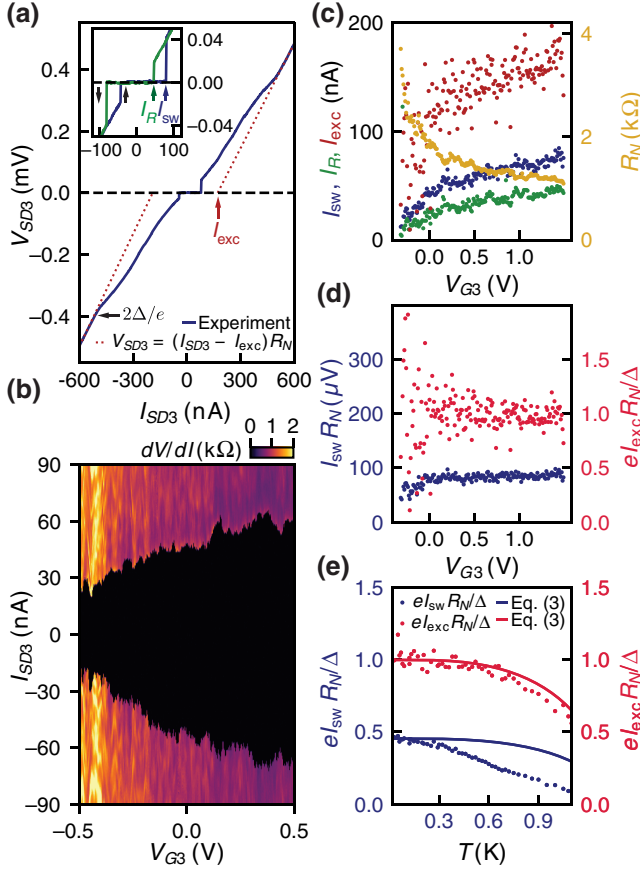
FIG. 5. (a) The measured voltage drop across the JJ V_{SD3} as a function of the applied current I_{SD3} for $V_{G3} = 1.5$ V for nanowire C. The normal-state resistance R_N and excess current I_{exc} are extracted by fitting to the normal state for voltages $V_{SD3} > 2\Delta/e$. From these measurements, we estimate $\Delta \approx 200$ μeV at $T = 20$ mK. The inset shows the region around the superconducting plateau with an up and down sweep of the current bias. The positions of the switching current I_{sw} and the retrapping current I_R are indicated by arrows. (b) The differential resistance dV/dI as a function of the applied current I_{SD3} and the gate voltage V_{G3} at $T = 20$ mK for nanowire C. (c) The extracted values for R_N, I_{exc}, I_{sw}, and I_R, extracted for nanowire B from the data set shown in the Supplemental Material [20]. (d) The $I_{sw}R_N$ product and the excess current I_{exc} multiplied by the ratio eR_N/Δ for $\Delta = 200$ μeV extracted from (c). (e) $eI_{exc}R_N/\Delta$ and $eI_{sw}R_N/\Delta$ as a function of the temperature T, calculated from data shown in Fig. S5 of the Supplemental Material [20]. The solid lines indicate the temperature dependence expected from BCS interpolation [Eq. (3)].

product in these structures is not well understood, due to insufficient knowledge of the electrodynamics and dissipation mechanisms in these junctions [38].

Next, we focus on the temperature dependence of the junction parameters. Figure 5(e) shows $eI_{sw}R_N$ and $eI_{exc}R_N$, both normalized by the gap Δ extracted at base temperature, as a function of the temperature for nanowire B at a fixed gate voltage $V_{G3} = 1.5$ V. The temperature dependence of the superconducting gap $\Delta(T)$ according to the BCS theory is also plotted against the experimental data, using the following interpolation formula [44]:

$$\Delta(T) = \Delta \tanh\left(1.74\sqrt{\frac{\Delta}{1.76 k_B T} - 1}\right), \qquad (3)$$

where we take $\Delta = 200$ μeV extracted at $T = 20$ mK. The good agreement for the excess current over the entire temperature range suggests that the excess current is dominated by Andreev reflections at the *S-N* interface, as has previously been observed for VLS InAs nanowires [39]. Similarly, we would expect the temperature dependence of $I_{sw}R_N$ to follow the temperature dependence of the superconducting gap, given that we estimate the junction to be in the short diffusive limit, $l_e \ll L \ll \xi_{diff}$, where l_e is mean free electron path, L is the junction length, and ξ_{diff} is the superconductor coherence length ([38]; see also Appendix B). The stronger reduction with temperature is qualitatively consistent with predictions for long diffusive *S-Sm-S* junctions ($\xi_{diff} \ll L$) [45,46], although similar behavior has previously been reported for InAs-based JJs with comparable lengths, critical currents, and mean free paths [39,47] .

VI. MULTIPLE ANDREEV REFLECTIONS

Subgap features in *I-V* curves of *S-Sm-S* junctions are often considered to be a manifestation of MAR processes and an indication of high overall junction transmission. Figure 6(a) shows the differential resistance averaged over a gate range 1.3 V $< V_{G3} <$ 1.5 V as a function of the voltage across the junction, V_{SD3}, for nanowire C. For highly transparent semiconducting junctions with a few conducting channels, MAR features are expected to be visible as peaks in the differential resistance at voltage drops $eV_m = 2\Delta/m$ [48–50], where m denotes the MAR order. The vertical lines in Fig. 6(a) indicate the peak positions for $\Delta = 200$ μeV and their corresponding MAR order m. From a fit to the extracted MAR positions, we obtain a superconducting gap $\Delta = (198 \pm 3)\mu$eV [Fig. 6(b)]. This value is in good agreement with the gap that we estimate from the transition to the normal conducting state [Fig. 5(a)].
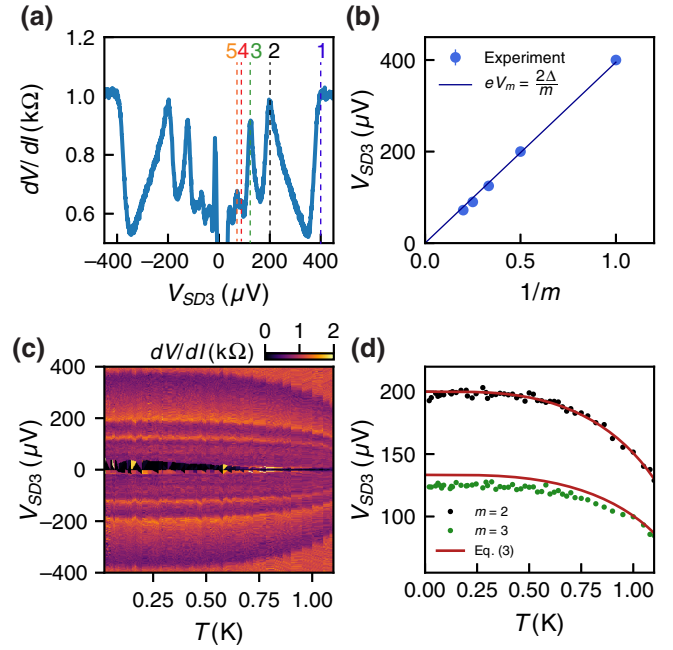

FIG. 6. (a) The averaged differential resistance dV/dI for 1.3 V $< V_{G2} <$ 1.5 V. The visible MAR peak positions for orders $m = 1$–5 are indicated by vertical dotted lines for nanowire C. (b) The fit to the MAR peak position yielding a superconducting gap $\Delta \approx 200$ μeV. (c) dV/dI as a function of the measured voltage drop across the JJ V_{SD} and sample temperature T. (d) The MAR peaks for $m = 2, 3$ as a function of the temperature. The red lines indicate the expected MAR peak positions based on $\Delta(T)$ [Eq. (3)] with $\Delta = 200$ μeV.

We plot the temperature dependence of the differential resistance in Fig. 6(c) to confirm the superconducting nature of the MAR features. The MAR peak positions are extracted and separately plotted in Fig. 6(d) for $m = 2, 3$. The red lines show the predicted MAR position for a BCS-like gap [Eq. (3)]. The experimental data shows good agreement with the BCS theory for $m = 2$. In the case $m = 3$, the data lie systematically below the predicted position over the entire temperature range. Similar results have been obtained in other superconductor-semiconductor structures [49,51]. The experimental data can potentially be better described by modeling the temperature dependence of the induced superconducting gap quantitatively, as in Ref. [49].

VII. DISCUSSION AND CONCLUSIONS

We characterize the different electrical properties of a superconductor-semiconductor materials system that uses selective-area-grown InAs with epitaxial Al on a silicon substrate. We find that the field-effect mobilities for the InAs channel are lower than but comparable with those of VLS nanowires, with the crucial advantage that the selective-area-grown structures are readily scalable. We

find a high-quality interface between the Al and InAs, as evidenced by an induced hard superconducting gap, high transparency of the JJs, and signatures of multiple Andreev reflections. The JJs exhibit a gate-tunable switching current with an $I_C R_N$ product lower than the superconducting gap of the Al but comparable to that of JJs fabricated from other superconductor-semiconductor structures. The reduced $I_C R_N$ product in this system and in similar systems is currently not well understood.

Our materials system is a potential platform for scalable and high-coherence gatemon devices. The hard superconducting gap and high junction transparency indicate the absence of disorder-related subgap states that can cause decoherence. The gate-tunable critical current of roughly 50 nA is sufficiently high to make gatemons with qubit frequencies up to around $6 - 8$ GHz for typical charging energies $E_C/h \sim 200 - 300$ MHz. The gatemon JJs could be fabricated on small mesa structures of the Al/III-V stack, while low-loss qubit capacitors and other readout and control components could be fabricated directly on the high-resistivity silicon substrate. Moreover, with further improvement, this materials system may also be suitable for other hybrid qubits, including protected superconducting qubits [52] and topological qubits [53].

ACKNOWLEDGMENTS

APPENDIX A: MATERIAL AND DEVICE FABRICATION

All three devices are fabricated on the same chip with standard electron-beam lithography techniques. In a first step, JJs are defined by selectively wet etching ($L \sim$ 120 nm)-long segments of the approximately 40-nm-thick Al film on the nanowires [Fig. 2(b)]. In a second step, Al is globally removed from the nanowires that are used for FET devices. Then, contacts are defined in a lift-off process. The chip is placed in an evaporation chamber and a 30-s argon-ion mill is performed *in situ* to ensure a low contact resistance followed by the evaporation of Ti(5 nm)/Au(150 nm). Next, 15 nm of HfO_x is deposited globally using atomic layer deposition as gate dielectric. For the final step, Ti(5 nm)/Au(150 nm) is evaporated to form top gates.

We fabricate a total of 28 FET devices, four of which do not work and are excluded from this study. We fabricate a total of seven superconducting devices, one of which does not work and is not included. The other six nanowires show similar figures of merit (see Table S1 of the Supplemental Material [20]). We present N-I-S' measurements for nanowire A, as it shows the cleanest spectroscopy data. We study $I_C R_N$ and I_{exc} on nanowire B, as we have the

most comprehensive data set for this wire. We study MAR features on nanowire C, as the most MAR peaks (up to order five) can be resolved.

APPENDIX B: COHERENCE LENGTH ESTIMATE

We estimate the coherence length based on the average charge-carrier density, n, and the field-effect mobility, μ, values estimated from the FET measurements (see Sec. III), considering only nanowires with the same orientation and width as nanowire B. First, we estimate the Fermi velocity, $v_F = \hbar v_F/m^*$, where we take the three-dimensional expression for the Fermi wave number, $k_F = (6n\pi^2)^{1/3}$, and use the bulk value for the effective electron mass in InAs $m^* = 0.026 m_e$ (where m_e is the free electron mass). This gives a Fermi velocity $v_F = 1.23 \times 10^6$ m/s, close to the bulk InAs value $v_{F,\text{bulk}} = 1.3 \times 10^6$ m/s. We estimate a mean free electron path $l_e = (\mu m^* v_F)/e \approx$ 60 nm that is shorter than the junction length $L \approx 120$ nm. The superconducting coherence length in this diffusive limit is then $\xi_{\text{diff}} \sim \sqrt{\hbar D/\Delta} = 290$ nm [38], where the diffusion constant $D = v_F l_e/3$. This implies that the junction is in the short diffusive limit ($l_e \ll L \ll \xi_{\text{diff}}$).

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