Nanomagnetic Self-Organizing Logic Gates

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The end of Moore's law for CMOS technology has prompted the search for low-power computing alternatives, resulting in promising approaches such as nanomagnetic logic. However, nanomagnetic logic is unable to solve a class of interesting problems efficiently, as it only allows for forward computing, due to the need for clocking and/or thermal annealing. Here, we introduce nanomagnetic *self-organizing* logic gates that can dynamically satisfy their logical proposition, irrespective of whether the signal is applied to the traditional input or output terminals, thus allowing for reversible computing. We present a design of a self-organizing NAND gate, the logically correct states of which are occupied equally in thermodynamical equilibrium, and illustrate its capabilities by implementing reversible Boolean circuitry to solve a two-bit factorization problem via numerical modeling. Our approach offers an alternative path to explore memcomputing, an unconventional computing paradigm the usefulness of which has already been demonstrated by solving a variety of hard combinatorial optimization problems.

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I. INTRODUCTION

Magnetic logic is a promising alternative to the standard complementary metal-oxide semiconductor (CMOS) technology. To date, this paradigm has brought us domain-wall logic [1,2], spintronic field-effect transistors [3,4], magnetic tunnel junctions [5,6], reprogrammable magnetic random access memory cells [7], and skyrmion logic devices [8]. Another promising approach is nanomagnetic logic (NML) [9–12], where nanomagnetic islands interact through their stray-field coupling. These interactions define the energy landscape of the islands and hence constrain the equilibrium orientation of their magnetization. By forcing the orientation of suitable "input" islands, one can impose an equilibrium configuration on an "output" island, which can be leveraged to realize logic operations. However, this approach suffers from the need for clocking [13,14] and/or thermal annealing [15,16], for which fast convergence to the ground state is not guaranteed, impeding their use for *reversible* logic operations. There, the entire logic circuit must relax to equilibrium as a whole, instead of through a cascade of local gate relaxations. These difficulties are a well-known general property of quenching problems [17] in complex effective-energy landscapes [18], where numerical solvers often employ cluster-flipping operations to induce a long-range order in their energy-minimization algorithms [19,20].

Despite several proofs of concept of such nanomagnetic logic [21–24], it is still unclear what the advantages are compared to the widespread CMOS designs that power the innumerable applications that we employ nowadays. In fact, it seems increasingly evident that "beyond CMOS" technology is not simply a matter of better devices. It also requires a fundamental rethinking of our computing paradigm, which, in turn, calls for novel ways in which logic operations are performed [25].

As an alternative, a type of *terminal-agnostic* logic has been suggested in Ref. [26], where a given gate can dynamically "self-organize" into its logically correct states, irrespective of whether the signal is applied to the traditional input terminals or the output terminals. These *self-organizing logic gates* (SOLGs) form the elementary building blocks of *digital memcomputing machines* [26]. These are machines that employ time nonlocality (memory) to simultaneously process and store information. Their usefulness has already been demonstrated by solving a variety of hard combinatorial optimization problems, including Boolean satisfiability (SAT), maximum

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satisfiability, integer linear programming, and even training of neural networks (for a brief review of these applications, see, e.g., Ref. [27]). The practical implementation of SOLGs suggested in Ref. [26] relies on resistive memories in addition to active devices, realizable with CMOS. Consequently, this design necessarily leads to an increased spatial footprint and suboptimal energy consumption, two important aspects of any future computing paradigm.

Here, we introduce a concept of SOLGs that, instead, employs stray-field-coupled nanomagnetic islands to perform terminal-agnostic logic: *nanomagnetic self-organizing logic* gates. In view of their design and mode of operation, we expect these systems to improve significantly over those suggested in Ref. [26], thus offering an alternative path to explore memcomputing.

Our strategy to build these gates relies on two main properties. First, we show that appropriately tailored stray-field interactions can enforce the logic proposition of the gate with equal population of all correct states, which is called *balancedness* [28]. Second, we employ *dynamic error suppression*, to limit the time spent in excursions between logically correct states as a result of thermal fluctuations. The combination of these two features makes these gates fundamentally different than stochastic gates, such as those proposed in Ref. [29].

We show that the combination of these two features is sufficient to implement a nanomagnetic SOLG, which can be used to construct reversible nanomagnetic SO circuits. This is demonstrated using a two-bit multiplier, which is capable of solving a simple factorization problem.

II. GATE DESIGN

A. Balanced gates

It is far from trivial to directly map a whole computational problem to an arrangement of nanomagnetic islands such that the corresponding energy landscape reflects the solution to the problem. Therefore, we focus on the design of the functionally complete NAND gate, from which *any* Boolean circuit can be constructed in a bottom-up approach [30]. This approach thus allows us to construct, e.g., a two-bit multiplier in a similar way to that used in CMOS-based logic circuits. However, to reduce the number of nanomagnetic islands that are needed to construct a certain circuit, it may be beneficial to use building blocks capable of inherently emulating more complex functionalities. For instance, an arrangement of nanomagnetic islands that directly mimics the behavior of a half-adder may consist of fewer islands than when the half-adder is constructed bottom-up with NAND gates. Finding such designs is, however, not a trivial task. It will therefore be left to future work, as minimizing the number of islands of a particular circuit is beyond the scope of this paper.

Irrespective of the hardware realization, for probabilistic logic to work, the gates need to be *balanced* [28], i.e., with equal probability for all logically correct states. To illustrate this necessity, we consider a theoretical unbalanced NAND gate only defined by its state probability distribution, as shown in the upper panel of Fig. 1(a). The upper panel of Fig. 1(b) shows the state probability distribution of a circuit built up out of three of these unbalanced gates. For the sake of simplicity, the connected terminals are assumed to always share the same logical value, i.e., either bit 0 or bit 1, which allows us to calculate the probability of a state as $P_{\text{circuit}}(A,B,C,D,O) \propto \sum_{i,j=0}^{i,j=1} P_{\text{gate}}(A,B,i)P_{\text{gate}}(i,C,j)P_{\text{gate}}(j,D,O)$. Even for a circuit as small as three gates, erroneous results arise due to the unbalancedness of the constituent gates: the least likely logically correct (horizontal blue line) and most likely logically incorrect state (horizontal red line) become indistinguishable. This is not the case when the circuit is assembled using balanced gates, as shown in the lower panel of Fig. 1.

Recently, a balanced NAND gate consisting of 19 nanomagnetic islands with in-plane magnetization has been designed, the three lowest-energy states of which present a fourfold degeneracy corresponding to the four NAND logic states [31]. This design, and any NML design that would be balanced following the definition given in Ref. [28], i.e., that the energies of all logic states are equal, has the drawback that it requires a slow and nontrivial annealing scheme to operate correctly, since its equal population is only achieved in the $T = 0\,\text{K}$ temperature limit. Therefore, we design a gate the logically correct states of which are occupied equally in thermodynamic equilibrium, i.e., also at a nonzero temperature.

B. Gate design

We consider gates consisting of nanomagnets that are magnetized out of plane and located on the same lattice plane. The nanomagnets have a cylindrical shape with a diameter of $d = 8.4$ nm and a thickness of $t = 6.5$ nm, i.e., sufficiently small to have a single-domain state, which allows us to use a macrospin approach. In thermodynamic equilibrium, the spins are either fixed or free to evolve according the stochastic Landau-Lifshitz-Gilbert (LLG) equation and the perpendicular-magnetization component of each island is interpreted as a logical 0 or 1, depending on its sign: $m_z < 0$ (bit 0); $m_z > 0$ (bit 1). However, to find a balanced gate, it is not computationally feasible to investigate every possible design by solving the full stochastic LLG equation. Therefore, in our search for a suitable gate design, we focus on solely evaluating the two-state behavior to find potential gate candidates. This analysis assumes that all free spins are in local equilibrium states $\mathbf{m}_i = (0, 0, \pm 1)$, for which the magnetocrystalline anisotropy energy is minimal. Using this two-state model, the requirement that the logically correct states must be occupied equally in thermodynamic equilibrium is met

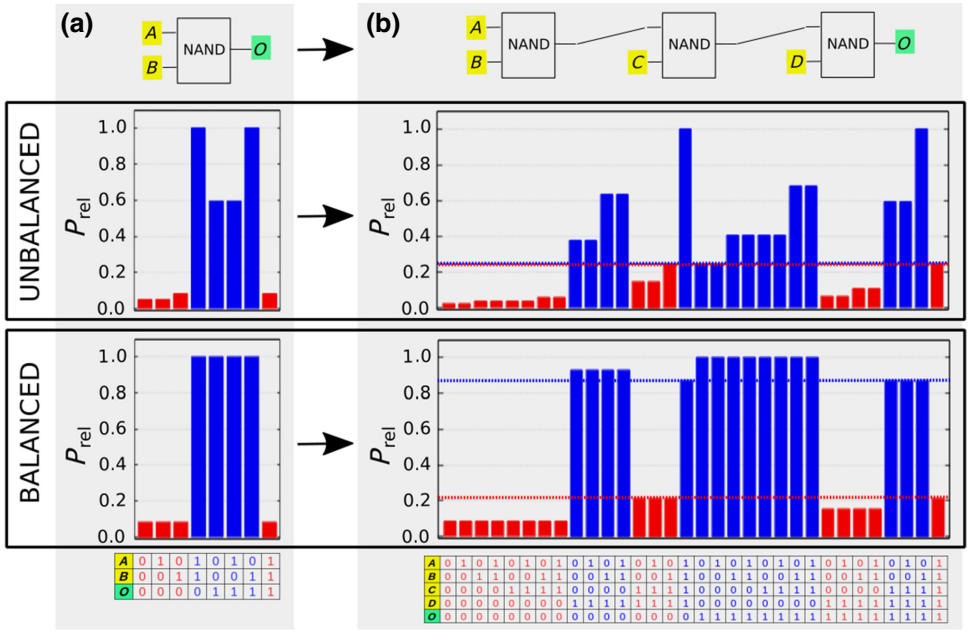

FIG. 1. The effect of balancedness on a logic circuit. (a) The Boltzmann probability distribution for a unbalanced and a balanced NAND gate. The relative probability P_{rel} is obtained by dividing the probabilities of all of the possible states by the probability of the most likely logical state. The inputs (marked in yellow) and the output (marked in green) are "free," i.e., they can take the logical values 0 and 1. (b) The Boltzmann probability distribution for three NAND gates in series, with free inputs and a free output. The terminals that are connected always share the same logical value. The horizontal red line indicates the probability of the most likely logically incorrect state, while the horizontal blue line indicates the probability of the least likely logical state. If the circuit consists of unbalanced gates (upper panel), some logically correct states are indistinguishable from the logically incorrect states. In contrast, the same circuit built up out of balanced gates does not suffer from this problem (lower panel).

when the relative Boltzmann probabilities of these states are equal. The Boltzmann probability of a spin-flip state σ_s is given by

$$P[\sigma_s] = \frac{\exp^{-\beta\epsilon(\sigma_s)}}{\Sigma_s \exp^{-\beta\epsilon(\sigma_s)}}, \tag{1}$$

where β is the inverse thermal energy and the normalizing denominator runs over all $2^{N_{\text{free}}}$ spin-flip states, with N_{free} being the number of free islands. The relative energy $\epsilon(\sigma_s)$ of a spin-flip state is determined by the sum of all pairwise stray-field interactions and can be written as

$$\epsilon(\sigma_s) = \Sigma_{i,j=1,\ldots,N} \left(\frac{\mu_0 M_S^2 V^2}{8\pi |\mathbf{r}_{i,j}|^3} \right) m_{i,z} m_{j,z}, \tag{2}$$

where N is the total number of nanomagnets (free and fixed). M_S, V, μ_0, and $\mathbf{r}_{ij}$ denote the saturation magnetization, the magnetic volume, the magnetic permeability of free space, and the pairwise distance vector $\mathbf{r}_{ij} \equiv \mathbf{r}_i - \mathbf{r}_j$ between islands i and j, respectively. A gate design is thus fully characterized by all pairwise distance vectors, which are adjusted together with the magnetic moment of the fixed nanomagnets in order to balance the gate.

The gate design presented in Fig. 2(a) displays the behavior of a balanced self-organizing NAND gate. It consists of four nanomagnetic islands: two inputs, one output, and a so-called fixed-bias island, with both inputs having equal distance to the output and to the fixed-bias island, which guarantees that the logically correct states 011 and 101 are balanced. The magnetization of the fixed-bias island is fixed at $m_z = -1$, e.g., with the aid of exchange bias [32]. The position of the bias island is such that the bias field it creates is twice as large on the output as on the inputs, which balances the logically correct states 001 and 110. Finally, to balance *all* logically correct states, the strength of the bias field, i.e., the magnetic moment of the bias island, is set properly.

The magnetic moment of the bias island and its distance to the output is determined by the angle between the inputs and the output. We choose this angle to be 120°, from which it follows that the distance should be equal to $2.41R$ and that the magnetic moment of the bias island should be 22.6 times as large as that of the inputs and output. The latter can be achieved by using a bias island with a larger diameter and thickness, possibly also made from a material with a high-saturation magnetization (e.g., iron or cobalt). The angle of 120° is chosen in order to trade off between logically incorrect states with high energy and having a

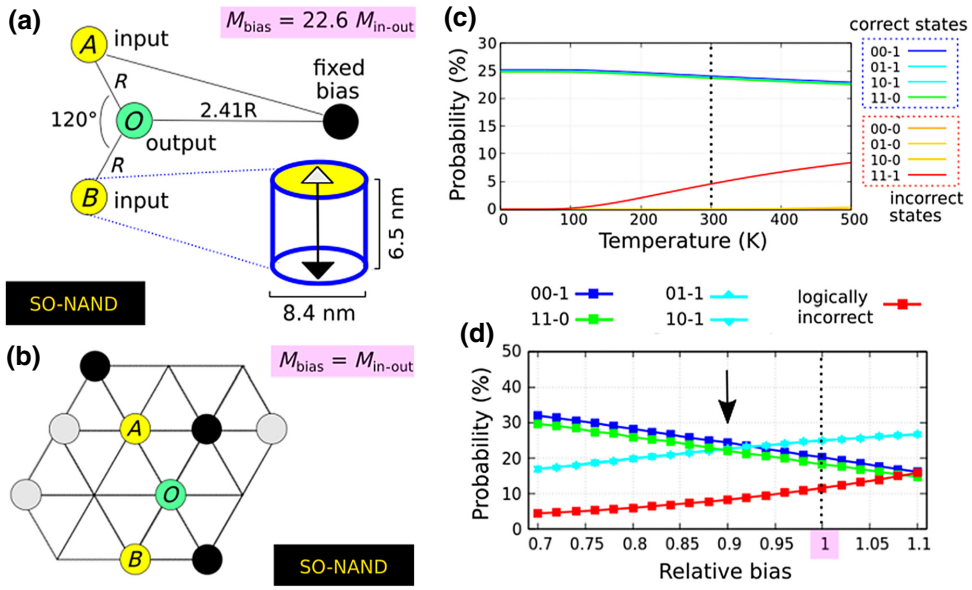

FIG. 2. The balancedness of the SO-NAND gate. (a) A balanced SO-NAND gate consisting of four nanomagnetic islands, schematically represented by circles. The input islands (marked "A" and "B") are shown in yellow and the output (marked "O") in green. The black circle represents a bias island with fixed magnetization $m_z = -1$ and with a magnetic moment that is 22.6 times as large as that of the input and output islands. $R = 11.34$ nm. (b) A balanced SO-NAND gate on a regular triangular grid, with multiple fixed-bias islands (black, $m_z = -1$; gray, $m_z = +1$). The magnetic moment of the bias islands is the same as that of the input and output islands, (c) Boltzmann probabilities based on the two-state model. Although the total probability of logically correct states decreases with increasing temperature, their individual probabilities remain matched as the thermal energy is varied. (d) The island macrospin dynamics are simulated at 300 K, as indicated by the vertical dashed line in panel (c). The likelihood of each logical state is shown for a varying relative magnetic moment of the fixed-bias island(s). To recover the balancedness, the bias island(s) should have a magnetic moment of only 90% (as indicated by the arrow) relative to the value obtained with the two-state model.

small value of $b = M_{\text{bias}}/(M_{\text{in-out}})$. The former increases the reliability of the gate, whereas the latter is beneficial from an experimental point of view.

Balanced gates are, however, still possible under the constraint of using only magnetic islands with identical magnetic moments, i.e., $b = 1$. Such a balanced SO-NAND geometry is presented in Fig. 2(b). It consists of two inputs, one output, and *multiple* bias islands that are placed on a regular triangular grid. Differing only in the way in which the bias fields are generated (i.e., either one large island or multiple smaller ones), the gate designs shown in Figs. 2(a) and 2(b) give rise to the same physical behavior (i.e., logical probabilities), thus allowing us to refer to both as "our gate."

To demonstrate the balancedness of our gate, we plot the Boltzmann probabilities as a function of the temperature for the eight possible metastable states in Fig. 2(c), corresponding to the input and output islands magnetized (anti)parallel to their uniaxial anisotropy axis, i.e., $m_z = \pm 1$. The probabilities are calculated using the two-state model [see Eqs. (1) and (2)] with saturation magnetization $M_S = 1000$ kA/m, magnetic volume $V = \pi d^2 t/4 = 360$ nm^3, and $R = 11.34$ nm. Thus, our design is optimal both with respect to the difference in probability between logically correct states and their total probability, although the latter decreases with increasing temperature.

C. Dynamical behavior

To investigate the out-of-equilibrium behavior of the gate in nanomagnetic logic, we replace the two-state model by a more realistic dynamical macrospin model that takes thermal fluctuations into account and use the macrospin simulation tool VINAMAX [33] to solve the stochastic LLG equation

$$\dot{\mathbf{m}} = -\gamma \mathbf{m} \times \left[\frac{\nabla_{\mathbf{m}} E(\mathbf{m})}{\mu_0 M_S V} + \mathbf{H}_{\text{therm}} \right] + \alpha(\mathbf{m} \times \dot{\mathbf{m}}), \quad (3)$$

where $\dot{\mathbf{m}}$ is the time derivative of the normalized magnetization, γ is the gyromagnetic ratio, α is the unitless Gilbert-damping constant, and $\mathbf{H}_{\text{therm}}$ the stochastic thermal field. The damping constant is set at $\alpha = 0.4$, similar to the values reported for thin Co/Pt multilayers and films [34–36]. In Eq. (3), $E(\mathbf{m})$ denotes the magnetic free energy of the ensemble, which is given by the combination of uniaxial magnetocrystalline anisotropy of each nanomagnet

plus the sum of all pairwise stray-field interactions:

$$E(\mathbf{m}) = \sum_i \left[-KV(\mathbf{m}_i \cdot \mathbf{u})^2 - \frac{\mu_0 M_S^2 V^2}{8\pi} \times \sum_{j \neq i} \left(\frac{3(\mathbf{m}_i \cdot \mathbf{r}_{ij})(\mathbf{m}_j \cdot \mathbf{r}_{ij})}{|\mathbf{r}_{ij}|^5} - \frac{\mathbf{m}_i \cdot \mathbf{m}_j}{|\mathbf{r}_{ij}|^3} \right) \right]. \quad (4)$$

The easy axis, $\mathbf{u}$, coincides with the $\hat{\mathbf{z}}$ axis and the magnetocrystalline anisotropy strength is set at $K = 60$ kJ/m^3. We use the same values for M_S, V, and R as before and simulate at $T = 300$ K (room temperature). These parameters correspond to a ratio of the switching energy barrier to k_BT of 5.2, such that the resulting thermal switching dynamics play on time scales that allow the collection of sufficient statistics about the state probability distribution within a reasonable computation time. These statistics are obtained by checking the logical state of the system each 10 ps during a period of 4–40 ms (depending on the size of the system). For the sake of simplicity, we always use an initial state in which the magnetization of all free islands is set at $m_z = -1$. However, the simulated time is sufficiently long to ensure that the results are independent of the initial state and represent the probabilities in thermodynamic equilibrium.

In this dynamical macrospin model, the magnetization of an island can deviate from the easy axis, although the z axis remains the preferential orientation. However, the additional degrees of freedom negatively impact the balancedness of the gate due to the enlarged phase space. As shown in Fig. 2(d), the balancedness can be recovered by tuning the magnetic moment of the bias island(s). It turns out that the bias island(s) should have a magnetic moment of only 90% (as indicated by the arrow) relative to the value obtained with the two-state model. Figure 3 shows that this tuning is robust with respect to variations in temperature and material parameters, as a 20% change in the damping, temperature, or uniaxial anisotropy constant of our system only results in a 2% change of the required bias to recover the balancedness.

The proposed geometry is challenging to robustly manufacture experimentally with the currently available lithographic techniques. However, our approach can be extended to larger length scales without affecting the results, as long as the ratio of the switching energy barrier to k_BT is kept constant (i.e., at 5.2), which can be achieved by, e.g., lowering the saturation magnetization. The same argument can also be applied to issues pertaining to the tuning of time scales discussed in the rest of the study. By altering the size of the islands one also tunes their mean switching time, thus globally rescaling the gate operation speeds. Nonetheless, we perform

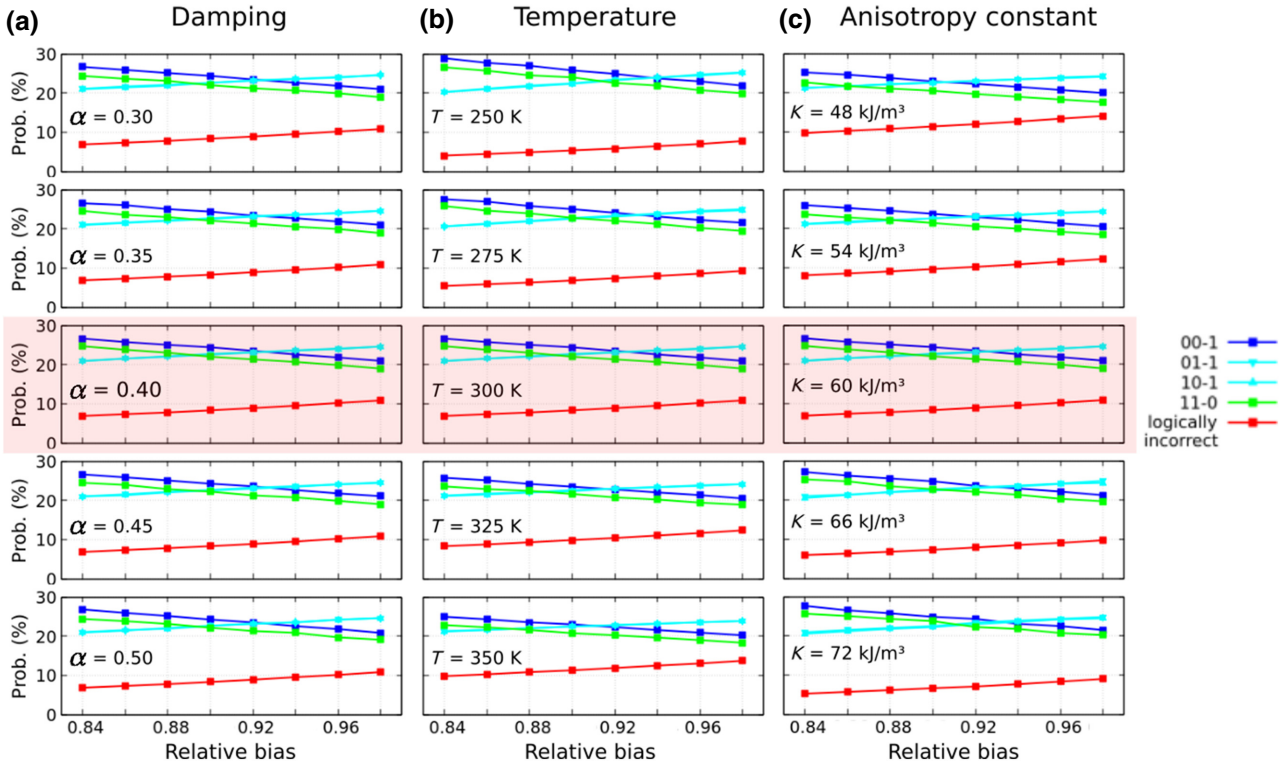

FIG. 3. The probabilities of the logical states, obtained with a dynamical macrospin approach using different relative bias strengths for varying (a) damping, (b) temperature, and (c) anisotropy constant. The highlighted region corresponds to the simulation parameters used throughout this work.

additional simulations to assess the robustness of our SO-NAND gate against variations in the island size and find that it still works reliably when the magnetic volume of the input and output islands is drawn from a Gaussian distribution with a standard deviation of 5% of the mean value of 360 nm^3. This reliability can be partially attributed to the applied dynamic-error-suppression scheme (see below).

III. DYNAMIC ERROR SUPPRESSION

A. Concept

Although the arrangement of nanomagnetic islands that we present above gives rise to a single balanced SO-NAND gate, the size of circuits that can be constructed using such a gate is limited by the fact that even a small (per gate) probability of logical incorrectness tends to propagate and grow within the context of a larger circuit. To overcome this issue, we introduce a *dynamic-error-suppression* (DES) scheme, which suppresses the incorrect states while preserving the balancedness of the gate. Here, a DES scheme refers to an *external* agent, e.g., a spin-polarized current, which is applied to improve the logically correct behavior of a gate or circuit and for which an additional power source is required.

The DES scheme, visualized in Fig. 4, is implemented in the model by periodically checking the logical correctness of each gate after a time τ_{DES}. If the gate is found to be in a logically incorrect state, an additional biasing field is applied on each input and output island for a duration of τ_{on}. This τ_{on} is chosen as a small fraction of the average switching time of the biased gate: $\tau_{\mathrm{on}} = 0.05\tau_{\mathrm{switch}}$. For our parameters, $\tau_{\mathrm{on}} = 10$ ps and $\tau_{\mathrm{switch}} = 200$ ps, as it takes our NAND gate on average 200 ps to switch from the logically incorrect 111 state to a logically correct state when the error suppression (ES) fields are fully applied, i.e., when all m_z are fixed at $m_z = +1$ in Eqs. (5):

$$B^A_{\mathrm{ES}} = -(0.080\ \mathrm{T})\left[m^B_z/(\sqrt{3})^3 + m^C_z\right], \tag{5a}$$

$$B^B_{\mathrm{ES}} = -(0.080\ \mathrm{T})\left[m^A_z/(\sqrt{3})^3 + m^C_z\right], \tag{5b}$$

$$B^C_{\mathrm{ES}} = -(0.080\ \mathrm{T})\left[m^A_z + m^B_z\right] + B_{\mathrm{add}}. \tag{5c}$$

The superscripts A and B refer to the input islands and C refers to the output island. m_z denotes the instantaneous magnetization along the easy axis and $B_{\mathrm{add}} = +0.049$ T for a NAND gate. The factor $(\sqrt{3})^3$ takes into account that the magnetostatic interaction between the input islands is weaker due to the larger distance between these islands [see Fig. 2(a)]. For a coupling between two islands, which is used for assembling circuits, the ES fields are set at

$$B^D_{\mathrm{ES}} = +(0.080\ \mathrm{T})\ m^E_z, \tag{6a}$$

$$B^E_{\mathrm{ES}} = +(0.080\ \mathrm{T})\ m^D_z \tag{6b}$$

to promote the fact that the magnetization of islands D and E points in the same direction.

These ES fields help us to escape from an incorrect metastable state while still allowing the gate to explore different states. The rate at which this DES scheme is applied, $\tau_{\mathrm{DES}}/\tau_{\mathrm{on}}$, is tuned in order to find a trade-off between the time for which the gate remains in a logically correct state and allowing the gate from accessing the full configuration space.

The most important aspect of the DES scheme is that it acts *locally* at the level of each individual gate and the individual couplings, so that all gates in the circuit *independently* suppress their respective logical errors, without requiring information about the state of the entire system. This local DES scheme acts similarly to the dynamic

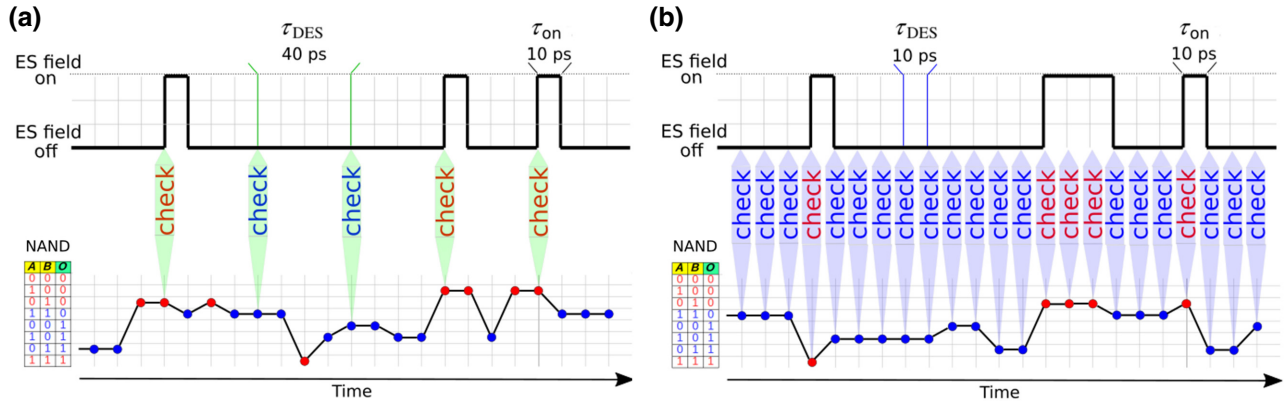

FIG. 4. A schematic representation of the dynamic-error-suppression (DES) scheme. The logical correctness of the gate is periodically checked, i.e., after a time τ_{DES}. If the gate is found to be in a logically incorrect state, an additional biasing field is applied on each input and output island for a duration of τ_{on}. (a) $\tau_{\mathrm{DES}} = 4\ \tau_{\mathrm{on}}$. (b) $\tau_{\mathrm{DES}} = \tau_{\mathrm{on}}$.

correction module (DCM) of a self-organizing gate that is used in conventional memcomputing machines [26]. There, the DCM of a certain gate reads the state of all of its terminals (voltages) and injects a correction signal on each terminal (current with appropriate sign) until the gate satisfies its logical proposition. The correction signal only depends on the state of the gate, i.e., on local information. However, in our present DES scheme, we allow for some degree of thermal fluctuations to help explore new states, while in the original DCM, no such fluctuations are present.

B. Physical implementation

Such a DES scheme could be physically implemented by adding an extra hardware layer to the magnetic gate. The state of the nanomagnets can be read out through a magnetic tunnel junction (MTJ) and forward logic can be used to detect the incorrect state and drive a correction signal in the form of a spin-polarized current to help the incorrectly aligned magnets to switch to a logically correct state. A lower-power alternative could by realized by making use of voltage-controlled magnetic anisotropy (VCMA) [37,38] to increase the switching probability of the logically incorrect island during τ_{DES}.

Estimation of the power requirements of such a DES scheme is hard at this stage, as no hardware realizations have been evaluated. On top of the forward CMOS logic, the major power consumption is in the readout of the state. Considering a MTJ-based state detection similar to those used in p-bit implementation [39] with a 1-ns probe current pulse, the detection of all three elements in one NAND gate would require about 10 fJ. The biasing of the elements using the spin-transfer torque would require 1 or 2 orders of magnitude more power but when a VCMA-based biasing is used, the dissipation is only dynamic. With the considered geometry of one island having a capacity of about 10^{-19} F, the dynamic losses are negligible.

C. Comparison with p-bit logic

Whereas our local DES scheme may be reminiscent of the biasing used in p-bit logic inversion [40], for p-bit operation, the time-varying current through each superparamagnetic tunnel junction (SMTJ) depends on the *global* state of all the logical bits in the system. Without the application of globally determined spin currents, however, no logically correct behavior would be observed, as the SMTJ elements are not coupled through stray-field interactions or in any other way that imposes logical behavior, in contrast to nanomagnetic islands. Thus, p-bit logic only works due to a power-consuming external agent (i.e., error suppression) that allows spin currents to flow through the SMTJ elements. Stated differently, the p-bit logical functionality is *entirely* embedded within the error suppression and requires *global* information. This is in sharp contrast to our approach, which only periodically suppresses logically incorrect states—which are rare anyway, as a result of the magnetostatic interactions—using only *local* information. For an individual gate, this is typically only applied for less than 1% of the time.

It is important to note that the time between two consecutive switches, anywhere in the system, decreases with increasing system size as $\tau_{\mathrm{switch}} \propto \tau_{\mathrm{SMTJ}}/N$, where τ_{SMTJ} is the natural switching time of an individual unbiased SMTJ and N is the number of SMTJ elements. This is because the switching probability of any one free SMTJ element can be roughly considered Poisson distributed with mean switching time τ_{SMTJ}/N. Thus, the intermediate operation of magnetoresistive state read, followed by digital elaboration of the biasing current intensities and their application, must take place on a time scale $\tau_{\mathrm{bias}} \ll \tau_{\mathrm{SMTJ}}/N$ to ensure proper performance. Consequently, the p-bit logic inversion is hard to scale, as τ_{bias} will reach the experimental limit for growing system size. One can, of course, engineer the SMTJ elements to have increasingly slower natural switching times with a growing system but this comes at the cost of having a longer total operation time to find the solution of the N-bit function that one wants to invert, as it takes a Boltzmann machine $\tau_{\mathrm{tot}} \propto \tau_{\mathrm{SMTJ}}(2^N/N)$ to stochastically sample all of the possible configurations.

In contrast to p-bit logic, the time scale on which our *local* DES scheme is applied is not proportional to $1/N$, because the strength of the ES field exerted on a certain island does not depend on the magnetic state of all N islands but only on the local state of the islands that belong to the same gate or intergate coupling. Hence, the time scale of our DES scheme is limited by $\tau_{\mathrm{switch}} \propto \tau_{\mathrm{island}}/N_{\mathrm{NAND}}$, where τ_{island} is the natural switching time of an individual unbiased island and N_{NAND} is the number of islands of which a NAND gate consists. This limit remains *constant* irrespective of the total circuit size, allowing us to build circuits of any size.

The difference between a global and a local DES scheme also manifests itself in the knowledge we must have about the solution of the targeted problem. A global DES scheme implies that there is an overhead system capable of determining the correct result of the *entire* problem, which allows us to bias the system out of incorrect states. As a consequence, tackling a different problem requires us to redesign the entire global DES scheme. In contrast, for a local DES scheme, it suffices that we know what the logically correct state of a single (NAND) gate—or whichever fundamental constituent gates are used—is or are, regardless of the complexity of the targeted problem.

IV. CIRCUITS

Now, we focus on how to assemble circuits using our SO-NAND gate, the state probability distribution of which is shown in Fig. 5(a) for several ratios of $\tau_{\mathrm{DES}}/\tau_{\mathrm{on}}$. Because

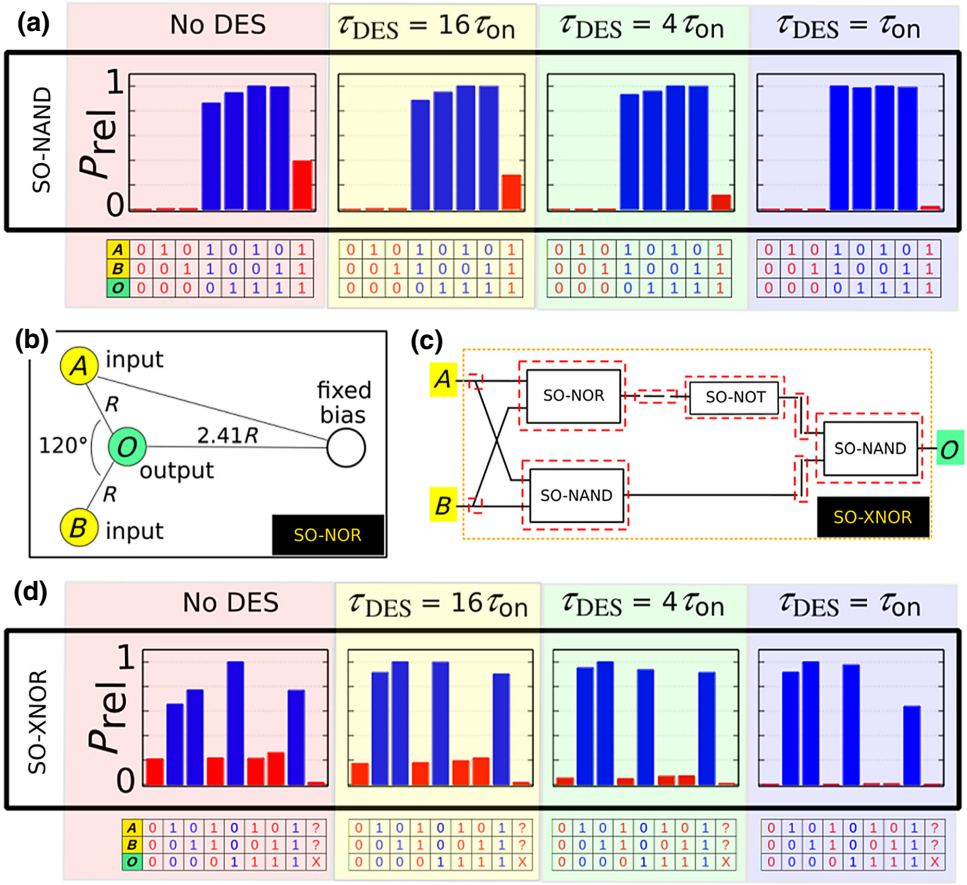

FIG. 5. The performance of the SO-NAND gate and the SO-XNOR gate with dynamic error suppression (DES). (a) The state probability distributions of a SO-NAND gate for different DES check times, τ_{DES}. The relative probability P_{rel} is obtained by dividing the probabilities of all of the possible states by the probability of the most likely logical state. (b) The SO-NOR gate is realized with the same geometry as the balanced SO-NAND gate, the only difference being the reversed magnetization of the fixed-bias island. (c) A schematic representation of a SO-XNOR gate. (d) The state probability distributions of a SO-XNOR gate for different τ_{DES}. The symbol "?" means that input islands A or input islands B are not logically consistent. All logically inconsistent states are aggregated into the X state (X stands for 0 or 1).

of the inversion symmetry between the truth tables of a NAND gate and a NOR gate, the same geometry behaves as a balanced SO-NOR gate when the magnetization of the fixed-bias island is reversed [as shown in Fig. 5(b)] and when we additionally set $B_{add} = -0.049$ T in Eq. (5c). This symmetry allows us to use this same design to realize a circuit with the functionality of an SO-XNOR gate, which can be constructed by making use of SO-NAND and SO-NOR gates and a SO-NOT gate as shown in Fig. 5(c). The SO-NOT gate simply consists of two adjacent nanomagnetic islands, for which the minimum energy state corresponds to an antialignment of their magnetization. The interactions between different gates are neglected, except for the islands that are part of the same coupling. These islands are magnetically coupled to align their magnetization. Aside from the DES biasing of individual gates, we introduce a modified DES scheme for such couplings, as detailed above. The probability distributions of the SO-XNOR gate are shown in Fig. 5(d).

We now demonstrate the use of our nanomagnetic SOLG in more complex logic circuits. In Fig. 7, we present a self-organizing two-bit multiplier (SO 2BM). A bottom-up approach is employed to construct the SO 2BM, relying on a SO-NAND and a SO-NOT gate to build a SO-AND gate and using the SO-XNOR design just introduced [see Fig. 5(c)]. In the simulations, all gates are treated as quasi-independent building blocks, meaning that islands of different gates only interact magnetostatically if they belong to the same coupling. In simulations, it is therefore unnecessary to consider the relative positions of different gates, thus avoiding the need for complicated geometries.

As an example of a reverse computation, the four output islands of the SO 2BM, labeled from a to d, are fixed to represent specific numbers to be factorized (0, 1, 2, 3, 4, 6, or 9). For example, number "6" translates to $a = 0$, $b = 1$, $c = 1$, and $d = 0$, where a, b, c, and d correspond to a bit value of 1, 2, 4, and 8, respectively. This state can be set by fixing $m_z^a = -1$, $m_z^b = +1$, $m_z^c = +1$, and $m_z^d = -1$, respectively. The fixing of the magnetization of these output islands can achieved, e.g., with the aid of exchange bias [32]. However, the balancedness of a gate with a fixed output has to be recovered in order to account for the change in phase space, as compared to the free operating mode, where the magnetization of each island can deviate from its easy axis. To obtain this goal, the magnetic moment of the bias island(s) should be tuned differently. For a SO-NAND gate the output of which is fixed at bit 1, this tuning results in a value of the relative bias equal of 1.04 (instead of 0.90), as shown in Fig. 6(a). We use the same tuning for a NAND gate with an output fixed at bit 0, although the requirement of being balanced is met by definition, as there is only one logically correct state, namely the 110 state.

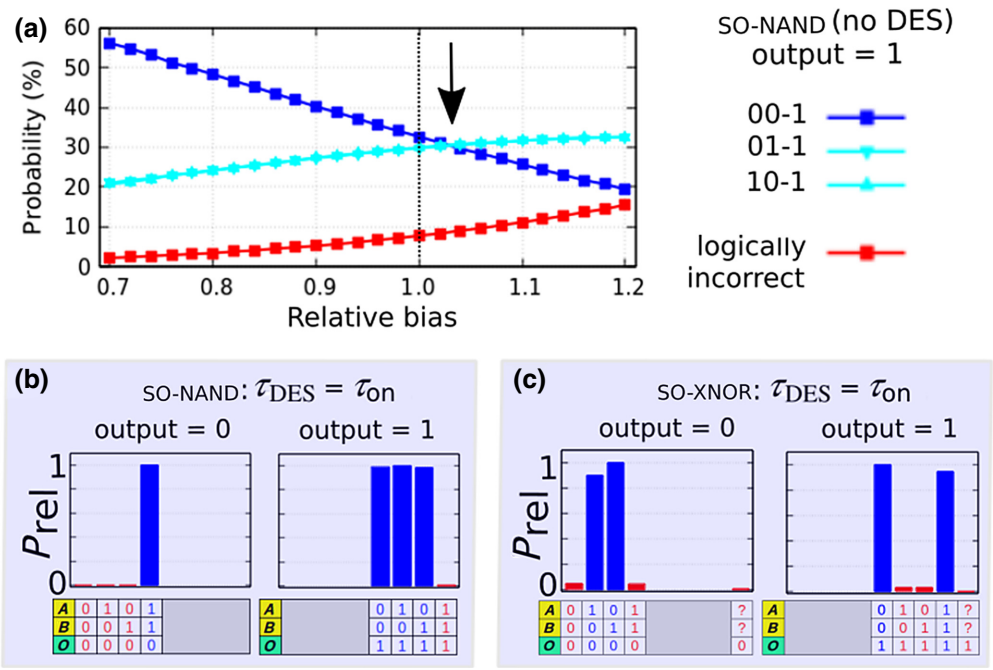

FIG. 6. SO gates with a fixed output. (a) The balancedness of a SO-NAND gate with output 1 is recovered at a relative bias of 1.04, corresponding to the point where the probabilities of all logically correct states are equal, as indicated by the arrow. The two-state model corresponds to a relative bias of 1. (b) The state probability distributions of a SO-NAND gate with fixed output. The relative probability P_{rel} is obtained by dividing the probabilities of all of the possible states by the probability of the most likely logical state. (c) The state probability distributions of a SO-XNOR gate with a fixed output.

The state probability distributions of a SO-NAND gate and a SO-XNOR gate with a fixed output are shown in Figs. 6(b) and 6(c), respectively.

Given the fixed magnetization of output islands a to d, the SO 2BM is allowed to explore its state space. The magnetization of the input islands, labeled from A to D, corresponds to the solution of our computation. For example, $m_z^A < 0$ and $m_z^B > 0$ means that $N = A + 2B = 2$, while $m_z^C > 0$ and $m_z^D > 0$ means that $M = C + 2D = 3$. Figure 7 demonstrates that our SO 2BM is capable of decomposing *any* output number into its (prime) factors. Each possible factorization is found without clearly favoring or penalizing any solution, which indicates that the balancedness remains largely conserved throughout the whole system.

V. CONCLUSION

In conclusion, we show that the use of balanced logic gates at nonzero temperature, supplemented with *local* dynamic error suppression, can be leveraged to build *nanomagnetic self-organizing logic gates*. These are

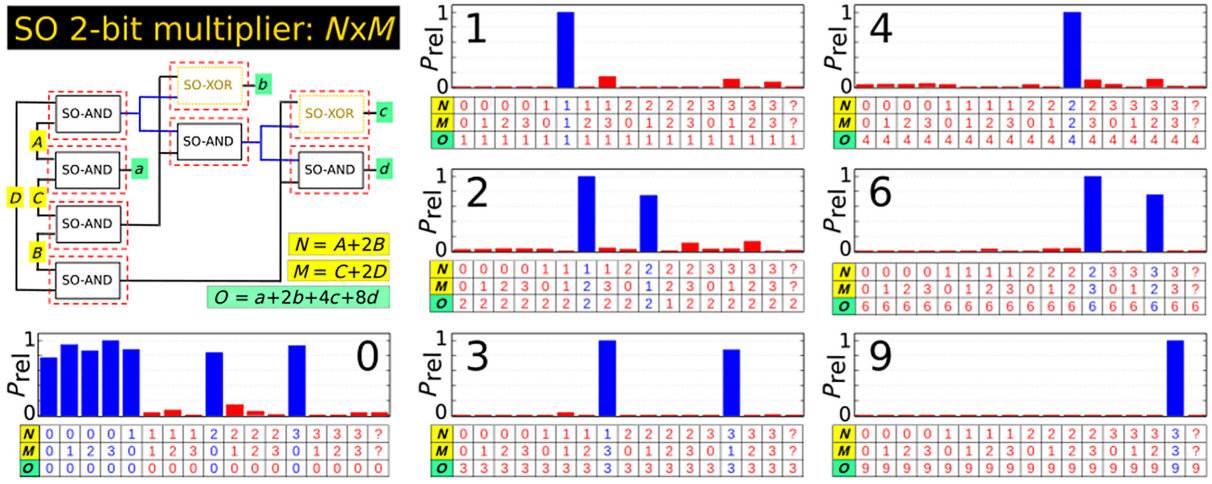

FIG. 7. The operation of a self-organizing two-bit multiplier. A schematic representation of a self-organizing two-bit multiplier and the state probability distributions for a fixed output, showing that for any fixed output, we retrieve the correct factorization(s) with a high probability. The relative probability P_{rel} is obtained by dividing the probabilities of all of the possible states by the probability of the most likely logical state. All states for which one of the inputs is logically inconsistent are aggregated into the "?, ?" state. The rate at which the DES scheme is applied, τ_{DES}, is set to $4\tau_{on}$.

terminal-agnostic gates that can dynamically satisfy their logical proposition regardless of whether information is committed to the inputs or outputs of the gate. They are the nanomagnetic equivalent of the building blocks required by digital memcomputing machines, which have already shown great promise in the solution of a variety of combinatorial optimization problems [27].

In particular, we propose a SO-NAND gate design that employs stray-field-coupled perpendicularly magnetized nanomagnetic islands. Because this gate is functionally complete, it allows us to construct circuits in a bottom-up approach.

As an exemplary application, we demonstrate number factorization by reversing the Boolean logic of a two-bit multiplier.

It is worth emphasizing that this approach is fundamentally different from the one suggested in Refs. [29,41,42], where the magnetic states of Boltzmann machines have been designed to be constrained by spin-current biasing of isolated SMTJs. Although this approach has notably been demonstrated on a small, yet emblematic, prime-factorization operation [40], it suffers a significant digital overhead because the individual current biases of all SMTJ elements in the circuit depend on the *global* magnetic state, i.e., the magnetic state of all elements. This means that the current biases need to be recalculated and adapted on the time scale between two consecutive switches anywhere in the circuit [40], since such switches affect the global magnetic state. However, the time between two consecutive switches decreases with increasing system size, making p-bit logic inversion hard to scale, since there is a critical system size for which the time to update the current biases reaches the practical limits. In contrast, our *local* DES scheme can be applied on time scales that only depend on the number of islands of individual gates used in the circuit, which remain *constant* regardless of the total circuit size, thus potentially allowing the inversion of circuits of any size. In addition, a local DES scheme only requires *a priori* knowledge about the logically correct states of a single (NAND) gate, which implies that it can be used to tackle every Boolean problem, hence omitting the need to redesign the DES scheme, as is the case for global DES schemes.

The disadvantage of a bottom-up approach is the overhead in the number of nanomagnetic islands needed to build a circuit. For example, our two-bit multiplier consists of 46 islands, which exceeds the number of SMTJ elements that are used in the p-bit logic of Borders *et al.* [40]. However, there, the small number of SMTJ elements is achieved by considering a circuit that is specifically designed to factorize a fixed number into two primes. This contrasts our more general approach, which allows us to build circuits that are able to reverse any multiplication, without any additional design conditions, although the overhead in the number of nanomagnetic islands could be significantly reduced, e.g., with an arrangement that directly mimics the functionality of a two-bit multiplier (or, at least, by using half-adder building blocks instead of individual NAND gates). However, the finding of novel gate designs capable of inherently emulating such complex functionalities while requiring a smaller overall number of islands is not a trivial task. Future work will attempt to use generative machine-learning models to aid in the search for such design improvements.

Regardless of these developments, the nanomagnetic self-organizing gates presented here represent a first important step toward the realization of unconventional computing architectures for the solution of a wide variety of problems of interest in academia and industry. Of particular interest are those related to cryptographically important functions such as Rivest-Shamir-Adleman (RSA) [43] and the Elliptic Curve Digital Signature Algorithm (ECDSA) [44], as well as many-to-one hashing functions [45], which are central to digital security [46] and block-chain protocols [47].

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M.D.V. is the co-founder of MemComputing, Inc. [48], which is attempting to commercialize the memcomputing technology. All other authors declare no competing interests.

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