Editors' Suggestion

Voltage-Gate-Assisted Spin-Orbit-Torque Magnetic Random-Access Memory for High-Density and Low-Power Embedded Applications

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The voltage-gate-assisted spin-orbit-torque (VGSOT) writing scheme combines the advantages from voltage control of magnetic anisotropy (VCMA) and spin-orbit-torque (SOT) effects, enabling multiple benefits for magnetic random-access-memory (MRAM) applications. In this work, we give a complete description of the VGSOT writing properties on perpendicular magnetic tunnel junction (PMTJ) devices, and we propose a detailed methodology for their electrical characterization. The impact of gate assistance on the SOT switching characteristics is investigated using electrical pulses down to 400 ps. The VCMA coefficient (ξ) extracted from the current-switching scheme is found to be the same as that from the magnetic-field-switch method, which is in the order of 15 fJ/Vm for 80–150-nm devices. Moreover, as expected from the pure electronic VCMA effect, ξ is revealed to be independent of the writing speed and gate length. We observe that SOT switching current characteristics are modified linearly with gate voltage (V_g), similar to that for the magnetic properties. We interpret this linear behavior as the direct modification of perpendicular magnetic anisotropy induced by VCMA. At $V_g = 1$ V, the SOT write current is decreased by 25%, corresponding to a 45% reduction in total energy down to 30 fJ/bit at 400 ps speed for the 80-nm devices used in this study. To test the operation reliability, we investigate the gate-SOT pulse configurations and overlays, and we find that an extended gate duration is able to preserve maximized gate benefit and selectivity. Furthermore, the device-scaling criteria are proposed, and we reveal that the VGSOT scheme is of great interest, as it can mitigate the complex material requirements of achieving high SOT and VCMA parameters for scaled MTJs. Finally, we perform design-to-technology co-optimization analysis to show that VGSOT MRAM can enable high-density arrays close to two-terminal geometries, with high-speed performance and low-power operation, showing great potential for embedded memories as well as in memory computing applications at advanced technology nodes.

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I. INTRODUCTION

Nonvolatile memory is believed to address the large standby-power issues in advanced technology nodes. Among the proposed candidates, magnetic random-access memory (MRAM) is attracting great attention due to its CMOS process compatibility, high density, low power, and relatively fast speed [1]. Recent progress has optimized spin-transfer-torque (STT) MRAM for embedded last-level cache, microcontrol unit, and embedded Flash applications [2–5], with commercial products beginning to appear on the market. Despite its excellent performance, present STT MRAM technology is not suited for implementation in the higher memory hierarchy, such as L1 or L2 cache memory, due to the significant incubation delay of the STT orientation and the voltage breakdown-writing speed trade-off. These constraints inhibit reliable programming of perpendicular magnetic tunnel junction (PMTJ) devices at below 5 ns [6].

To mitigate the STT limitations, the spin-orbit torque (SOT) [7] and the voltage control of magnetic anisotropy (VCMA) [8] effects are proposed as alternative writing mechanisms for the next MRAM generations. SOT is the transfer of orbital angular momentum from the lattice to the spin system. When injecting in-plane charge current in a heavy-metal layer, the spin Hall effect generates a spin current that would impose a dampinglike torque on the neighboring magnetization to induce switching. Simultaneously, a fieldlike torque induced by the Rashba interaction contributes to magnetization-reversal acceleration. These lead to the concept of SOT MRAM, a three-terminal device allowing for separate read and

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write channels, which significantly improve the device's endurance. Recent developments enable SOT PMTJ devices with energy-efficient and reliable subnanosecond writing capabilities [9,10].

VCMA, on the other hand, promises significant advances towards ultralow-power MRAM. The electronic based VCMA effect occurs by doping and redistributing electrons at the ferromagnet (FM)/MgO interface [11], which instantly modifies the interfacial magnetic anisotropy of the FM. In a PMTJ, the VCMA-induced free-layer (FL) switching is accomplished by applying a voltage across the MgO tunnel barrier to remove the energy barrier between the parallel (P) and antiparallel (AP) states; meanwhile, an external applied in-plane magnetic field (B_x) is required to induce FL precession around its axis [12]. Such a switching mechanism is unipolar and mostly voltage driven, allowing for ultralow energy consumption (fJ) at subnanosecond writing speeds [13].

However, SOT and VCMA PMTJs also present technological challenges. Both require the presence of an in-plane magnetic field to ensure deterministic switching. For SOT, various credible solutions have been proposed and demonstrated, such as integrating an embedded magnet as a field generator [14,15], making use of exchange bias by direct coupling with an antiferromagnet [16,17], or assisting reversal with STT [18]. Therefore, the present challenges for SOT are mostly related to the array density and write efficiency. Indeed, two transistors must be incorporated into a unit cell to operate a three-terminal SOT device. Meanwhile, the SOT write current remains larger than that for STT MRAM at the same technology node, which imposes a large selector transistor to accommodate its current, calling for the introduction of materials with larger spin Hall angles (θ_{SH}) [19,20]. For VCMA MRAM, the challenges mainly fall on the write margin and efficiency. The VCMA write duration is small, and it is subject to technology variations, such as VCMA coefficient (ξ), field amplitude, and MTJ diameter distribution, making uniform writing difficult in dense arrays. Furthermore, a large $\xi > 800$ fJ/Vm is mandatory to avoid compromising the retention of sub-30-nm PMTJs, which remains a major challenge, as typical values in PMTJs are in the range of 30–70 fJ/Vm at the device level [21].

To overcome the above-cited issues, a hybrid device combining advantageously SOT and VCMA effects is proposed [22], namely, voltage-gate-assisted spin-orbit-torque (VGSOT) MRAM; the cell structure is shown in Fig. 1(a). In the VGSOT concept, SOT is responsible for FL switching, while the VCMA top gate assists it. Several advantages emerge by having the VCMA gate assistance. First, it allows for SOT switching at a lower current, as it should be reduced proportionally to the decrease in FL perpendicular magnetic anisotropy (PMA). Second, the VCMA top gate can serve as the MTJ selector, which enables a multipillar

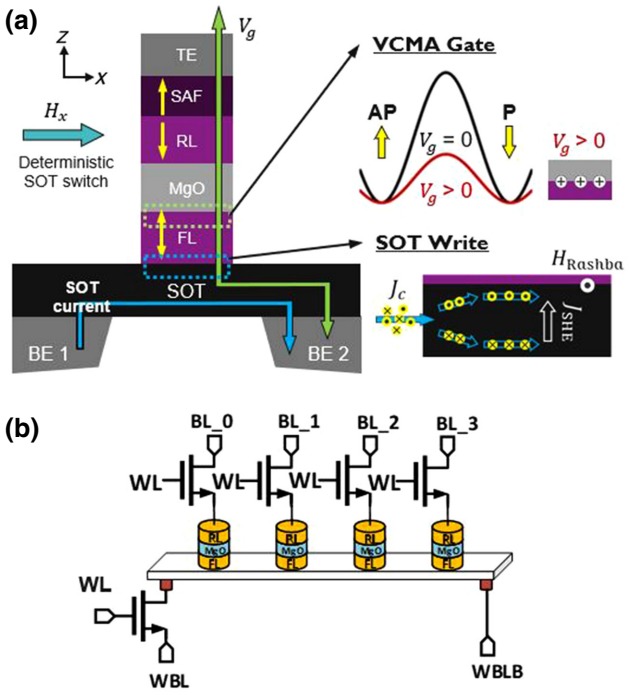

FIG. 1. (a) Illustration of the VGSOT writing scheme. Positive VCMA top gate induces electron accumulation at the FL/MgO interface, which lowers the PMA of the FL to allow for SOT switching with reduced current. (b) Multipillar VGSOT cell structure with target four MTJs on a SOT track. Gate voltage serves as the MTJ selector to enable a selective switch. WL, word line; BL, bit line; WBL, write bit line; WBLB, write bit line bar.

(MP) cell structure, as shown in Fig. 1(b). Such a design, with appropriate technology engineering, can also effectively reduce the VGSOT MRAM cell size to address the density limitation of SOT technologies. Third, by applying a read voltage opposite to write assistance, PMA is increased, which further limits the read disturbance [23]. Four, the VGSOT design can mitigate the need for achieving challenging high SOT and VCMA efficiencies, while maintaining the advantages of low power, high speed, and inherent nonvolatility.

Here, we study the VGSOT device properties using CMOS process-compatible PMTJ devices. Section II describes the experimental details, including the materials used for the MTJ stack, device fabrication process, and electrical measurements system. In Sec. III, the VGSOT switching properties are detailed: the VCMA coefficient is quantified by both magnetic field and current methods, and its dependences on size and pulse duration are investigated. Furthermore, the impact of SOT-gate pulse configurations and delays are tested to evaluate the writing scheme for practical operation, and we demonstrate the reliability and resilience of the VGSOT concept. Finally, in Sec. IV, we discuss the design perspectives for scaled VGSOT

devices. Based on the proposed MTJ property requirements, a design-to-technology co-optimization analysis is performed to evaluate VGSOT MRAM against other embedded memory technologies at the 5-nm technology node.

II. EXPERIMENTS

The PMTJ stack is deposited and integrated using our 300-mm SOT MRAM platform [10]. Typical structures consist of a prepatterned substrate with smoothed bottom electrodes, allowing electrical contact with a 3.5-nm tungsten (W) SOT track. The top-pinned PMTJ stack deposited on top of the SOT layer is composed of a 0.9-nm $Co_{20}Fe_{60}B_{20}$ FL, a 1.7-nm MgO barrier, and a $Co_{17.5}Fe_{52.5}B_{30}$/spacer/Co reference layer (RL). Through a Ru spacer, the RL is antiferromagnetically coupled to a $(Co/Pt)_x$ multilayer-based hard layer, forming the synthetic antiferromagnet (SAF) structure. The designed MgO thickness targets a resistance-area (RA) product of 5 kΩ μm^2 to suppress the STT current in the gate channel. All layers are sputter deposited in a Canon Anelva EC7800 cluster tool. After deposition, the stack is annealed at 300 °C for 30 min in vacuum in a TEL-MSL MRT5000 batch-annealing system, with a 1 T out-of-plane magnetic field applied. To pattern the device, we use 193-nm immersion lithography, and ion-beam etching forms 80–150-nm circular MTJ pillars, while optimized etch-stop conditions ensure the SOT layer remains intact. Next, the SOT layer is etched into 190–300-nm-wide tracks, depending on the MTJ size. Finally, the Cu top electrode is fabricated to complete the integration process, forming the three-terminal devices. The saturation magnetization of the FL ($M_{S,FL}$) measured by the Microsense vibrating sample magnetometer (VSM) before patterning is 900 kA/m.

For device characterizations, we use an Hprobe MRAM prober solution. The electrical scheme is shown in Fig. 2(a), where both SOT and gate channels are individually connected to a source measure unit and a pulse generator. It allows for dc and pulsed measurements with controllable dc voltages (V_{SOT}^{dc}/V_g^{dc}), pulse voltages (V_{SOT}/V_g), pulse durations ($t_{p,SOT}/t_{p,g}$), and time delays between the two channels. Unless specified, the pulses are synchronized and of the same duration (t_p). Additionally, the system is provided with individual controls over the out-of-plane and in-plane magnetic fields (H_z/H_x). To estimate the current distribution in the SOT channel, we use the parallel resistance model shown in Fig. 2(b). The total SOT current (I_{SOT}) splits into the SOT edge current (I_{edge}), SOT active-switching current (I_{sw}), and FL current (I_{FL}). Hence, $I_{eff} = I_{sw} + I_{FL}$ accounts for current shunting in the FL and defines the effective current required for switching. The resistivities of the FL and SOT layers are estimated to be 120 and 160 μΩ cm, respectively.

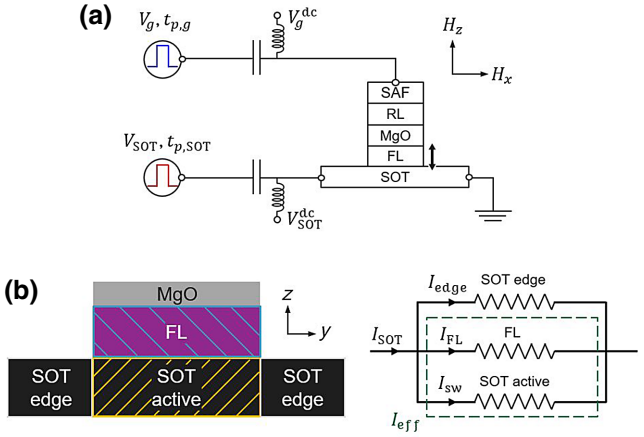

FIG. 2. (a) Schematic of the electrical setup for VGSOT measurements. (b) Parallel resistance model used to estimate the distribution of applied SOT current.

III. VGSOT MTJ DEVICE PROPERTIES

A. Fundamental MTJ properties

In Fig. 3, the fundamental properties of MTJs are presented as a function of electrical critical dimension (eCD). Statistics are obtained from 60 devices per size. We measure a median TMR of 120%, and a coercive field (H_C) of 40 mT, which decreases to 25 mT in the smallest devices. Compared with our reference devices [15], we notice that a thicker MgO barrier induces lower H_C. We attribute such degradation to the MgO deposition conditions, which we believe can be resolved by stack engineering. Next, we estimate the PMA field ($H_{k,eff}$) and the thermal stability factor (Δ) using the magnetic-field-switching probability [$P_{sw}(H_z)$] method [24]:

$$P_{sw}(H_z) = 1 - \exp\left\{\frac{-H_{k,eff} f_0 \sqrt{\pi}}{2R\sqrt{\Delta}} \operatorname{erfc}\left[\sqrt{\Delta}\left(1 - \frac{H_z - H_S}{H_{k,eff}}\right)\right]\right\}, \quad (1)$$

where f_0 is the attempt frequency, R is the magnetic field sweep rate, and H_S is the effective stray field from the RL-SAF layers. We measure a median $\mu_0 H_{k,eff}$ of 70 mT, independent of eCD, and a thermal stability factor (Δ) increasing with eCD from 35 to 50 $k_B T$.

To estimate the VCMA coefficient, we first quantify the dependence of $H_{k,eff}$ on dc bias voltage, i.e., the VCMA slope ($\partial H_{k,eff}/\partial V_g^{dc}$). The magnetic-field-switching probability curves are measured under different V_g^{dc} values, as shown in Fig. 4(a). A clear shrinkage (expansion) in the switching fields is observed under positive (negative) V_g^{dc}. By fitting the probability curves with Eq. (1), we summarize in Fig. 4(b) the dependences of $\mu_0 H_C$ and $\mu_0 H_{k,eff}$ on V_g^{dc}. As expected from the regular VCMA effect, both

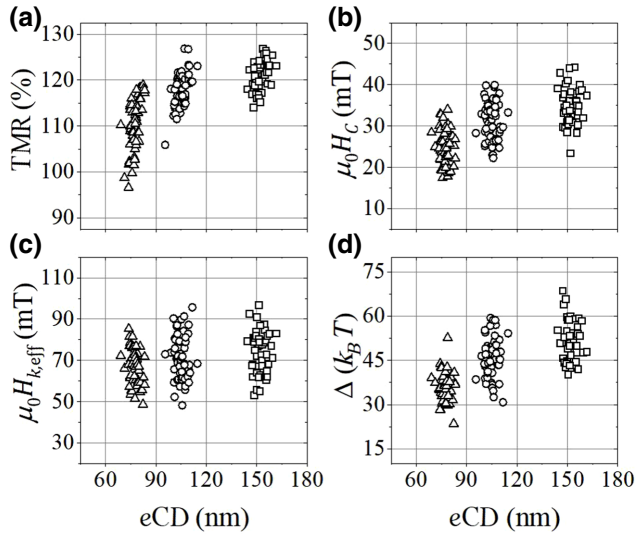

FIG. 3. PMTJ devices properties as a function of eCD for (a) tunneling magnetoresistance (TMR), (b) coercive field ($\mu_0 H_C$), (c) effective perpendicular anisotropy field ($\mu_0 H_{k,\mathrm{eff}}$), and (d) thermal stability factor (Δ).

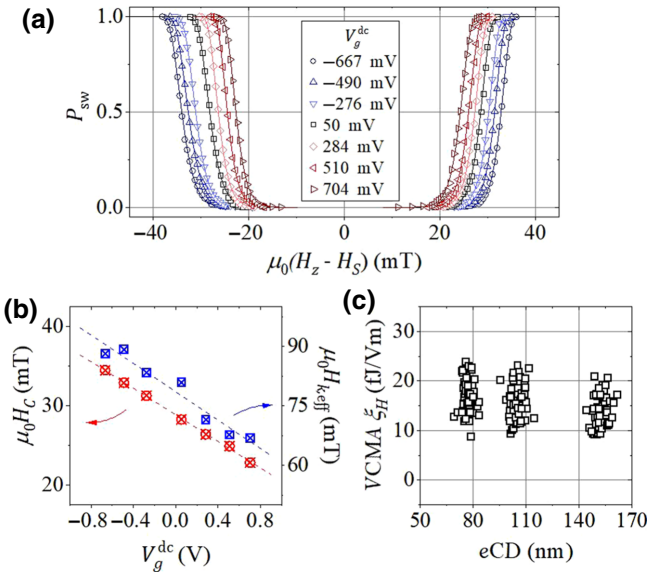

FIG. 4. Representative magnetic-field-switching probability curves as a function of out-of-plane field for various dc gate voltages (V_g^{dc}). (b) $\mu_0 H_C$ and $\mu_0 H_{k,\mathrm{eff}}$ as a function of V_g^{dc}. $\mu_0 H_{k,\mathrm{eff}}$ is obtained by fitting the distributions in (a). (c) VCMA coefficient (ξ_H) estimated by field-sweep method, which is shown to be independent of eCD.

quantities are reduced (enhanced) for $V_g^{\mathrm{dc}} > 0\,(<0)$ due to electron accumulation (depletion) at the FL/MgO interface. Such VCMA polarity is consistent with similar stacks in previous studies [25]. Here, we quantify the VCMA slope as 20 mT/V. Then, the field-estimated VCMA coefficient, denoted as ξ_H, is calculated as [26]

$$\xi_H = \frac{\mu_0 M_{S,\mathrm{FL}} t_{\mathrm{FL}} t_{\mathrm{MgO}}}{2} \frac{\partial H_{k,\mathrm{eff}}}{\partial V_g^{\mathrm{dc}}}, \tag{2}$$

where t_{FL} is the FL thickness and t_{MgO} is the MgO thickness. We obtain a median $\xi_H = 15$ fJ/Vm that is independent of eCD [Fig. 4(c)]. This lower than typical ξ_H can also be attributed to the MgO deposition conditions, which also seem to impact H_C.

B. Voltage-gate-assisted SOT switching

In the following, we discuss the switching results obtained from devices with eCD approximately 80 nm sitting on top of a 190-nm-wide SOT track. The SOT channel resistance (R_{SOT}) is 320 Ω. All measurements are performed at $\mu_0 H_x = 10$ mT, and $\mu_0 H_S$ is compensated by a $\mu_0 H_z$ of −15 mT. Figure 5(a) shows exemplary SOT switching-probability (P_{sw}) curves at $t_p = 0.4$ ns as a function of V_{SOT} under different gate values, as obtained from 100 switching events. We observe that VCMA induces a clear decrease (increase) in switching voltage under V_g of 1 V (−1 V) for both AP-P and P-AP transitions. The critical switching voltage, defined at $P_{\mathrm{sw}} = 50\%$, is converted into a critical switching current (I_c) and critical current density (J_c). Based on Fig. 2(b), a correction factor of 0.49 is applied to I_c for estimating the current contributing to switching I_{eff}, i.e., $I_{\mathrm{eff}} = 0.49 I_c$, and this will be used in Sec. IV to project the switching current for optimized processed devices. Figure 5(b) summarizes I_c as a function of $1/t_p$. It shows a typical linear scaling in the subnanosecond regime for both transitions at all gate values, implying that magnetization reversal remains mediated by domain-wall nucleation and propagation, and that the VCMA gate does not alter the mechanism. Such linear scaling is expressed as [27]

$$I_c(V_g) = I_{c0}(V_g) + \frac{q(V_g)}{t_p}, \tag{3}$$

where I_{c0} is the intrinsic critical current, and q is an effective charge parameter representing the number of electrons needed to be injected into the system before reversing magnetization, which also indicates the efficiency of angular momentum being transferred from the spin current to the system [27]. We plot the average intrinsic critical current (I_{c0}^{avg}) and q parameter (q^{avg}), averaging from the two switching directions, as a function of V_g in Figs. 5(c) and 5(d), respectively. Both quantities are linearly reduced (increased) for $V_g > 0$ (<0). We obtain $I_{c0}^{\mathrm{avg}}(0) = 0.32$ mA and $q^{\mathrm{avg}}(0) = 1.35 \times 10^{-13}$ C, and their dependences on V_g are −49.6 μA/V and -5.43×10^{-14} C/V, respectively. We interpret the $I_{c0}^{\mathrm{avg}}(V_g)$ linear scaling as a reflection of direct modification of the FLPMA upon gate-voltage applications. Since q is understood to describe the conservation of angular momentum

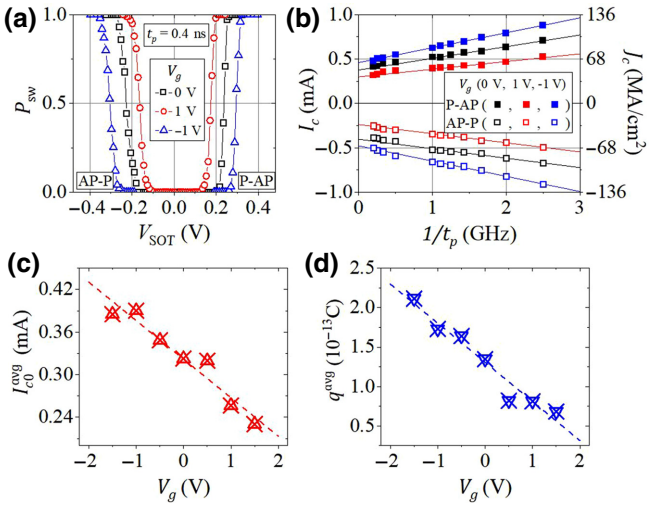

FIG. 5. Classical SOT switching-probability distribution (P_{sw}) as a function of SOT pulsed voltage (V_{SOT}) for different gate values (V_g) at $t_p = 0.4$ ns. (b) Critical SOT switching current (I_c) at $P_{sw} = 50\%$ as a function of $1/t_p$. (c) Average intrinsic critical current (I_{c0}^{avg}) and (d) average q parameter (q^{avg}) as a function of V_g.

[27,28], one can expect that $q^{avg}(V_g)$ should follow the linear trend of $I_{c0}^{avg}(V_g)$, as we report in Fig. 5(d). With 1-V gate assistance, we quantify a 25% reduction in I_{c0}^{avg}.

We also estimate the VCMA coefficient at various t_p based on the VGSOT switching results, denoted as ξ_I. The equation to calculate ξ_I is derived from the macrospin SOT switching current equation [29]:

$$I_c \sim \frac{2e\mu_0 M_{S,FL} t_{FL}}{\hbar\theta_{SH}} \left(\frac{H_{k,eff}}{2} - \frac{H_x}{\sqrt{2}} \right) w_{SOT} t_{SOT}, \quad (4)$$

where θ_{SH} is the spin Hall angle, w_{SOT} is the SOT track width, and t_{SOT} is the SOT layer thickness. Since we observe a linear variation of I_c on V_g, the slope is expressed as

$$\frac{\partial I_c}{\partial V_g} = \frac{e\mu_0 M_{S,FL} t_{FL}}{\hbar\theta_{SH}} \frac{\partial H_{k,eff}}{\partial V_g} w_{SOT} t_{SOT}. \quad (5)$$

By substituting Eqs. (4) and (5) into Eq. (2), ξ_I is derived as

$$\xi_I \sim \frac{\mu_0 M_{S,FL} t_{FL} t_{MgO}}{2} \frac{\partial I_c}{\partial V_g} \frac{H_{k,eff}(V_g = 0)}{I_c(V_g = 0)}, \quad (6)$$

which is an equivalent expression to that reported in Ref. [9]. Equation (6) is typically valid for estimating ξ_I from I_{c0}. However, since the slope of $\partial I_c/\partial V_g$ is normalized by the SOT current and $H_{k,eff}$ at $V_g = 0$ V, one can anticipate finding that Eq. (6) is also applicable to I_c, which we confirm in Fig. 6(a), with $\xi_I \sim 15$ fJ/Vm being independent of t_p. This further indicates that VCMA in our MTJ is,

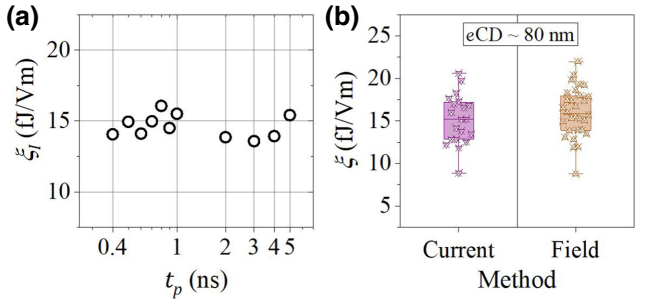

FIG. 6. (a) VCMA coefficient estimated from VGSOT switching current (ξ_I) as a function of t_p. (e) Comparison of VCMA coefficients estimated with current-switch and field-switch methods from 80-nm devices.

as expected, an instantaneous and electronic based effect. Importantly, we find that the ξ_I estimation method gives the same median value as the field-sweep method ξ_H, as shown in Fig. 6(b).

A reduction in switching current and, thereby, energy is one of the major benefits of VGSOT switching. To estimate the switching energy, we use an equivalent circuit, as shown in Fig. 7(a). We consider here the total energy (E_{total}) spent in the present device as the sum of energy dissipations in the SOT channel (E_{SOT}) and the gate channel (E_{gate}):

$$E_{total} = E_{SOT} + E_{gate}, \quad (7)$$

with

$$E_{SOT} = I_c^2 R_{SOT} t_p, \quad (8)$$

$$E_{gate} = \frac{V_g^2}{R_{MTJ} + 0.5R_{SOT}} t_p, \quad (9)$$

where R_{MTJ} is the resistance of the MTJ, taken as the P-state resistance. Figure 7(b) presents the energy values at $t_p = 0.4$ and 1 ns. Since E_{gate} is negligible due to high R_{MTJ}, the main energy dissipation comes from E_{SOT}. This demonstrates the benefit of gate assistance to SOT switching, with E_{total} reduced by 45% at $V_g = 1$ V to 30 and 41 fJ for $t_p = 0.4$ and 1 ns, respectively.

C. Reliability

In this section, we investigate the reliability of VGSOT switching. First, we study how the gate duration and timing modify the average critical switching current (I_c^{avg}) at $t_{p,SOT} = 5$ ns by looking at the gate overlay for $V_g = 1$ V. SOT and gate pulses are synchronized, and $t_{p,g}$ is varied from 0 to 9 ns, as shown in Fig. 8(a). We observe that I_c^{avg} decreases progressively with increasing $t_{p,g}$, and it reaches a maximum reduction of 25% when the SOT pulse is completely overlaid by the gate, i.e., $t_{p,g} = t_{p,SOT}$. We interpret this behavior as the decrease of nucleation energy, which

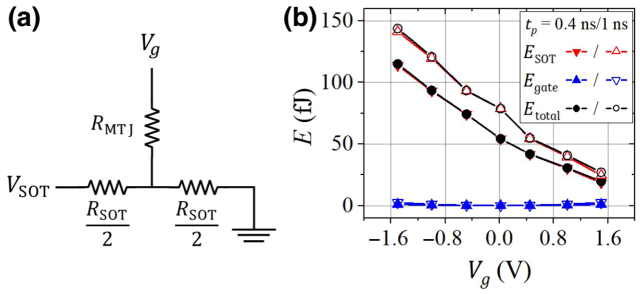

FIG. 7. (a) Schematic of equivalent circuit used for estimating switching energies. (b) Switching energies as a function of V_g at $t_p = 0.4$ and 1 ns.

can also result in a reduction of the nucleation delay time reported in Refs. [9,28]. Furthermore, we extend the gate duration prior to the SOT pulse, in addition to the primitive 5 ns, as shown in Fig. 8(b). It demonstrates that the pre-SOT gate does not influence I_c^{avg}. Similar results are also obtained for $t_{p,SOT} = 1$ ns (not shown). From the perspective of practical operation, these results suggest that one can moderately increase the gate duration to provide a sufficient gate margin to compensate for potential offsets in the SOT current arrival time, while maintaining the full advantage of current reduction and bit selectivity.

Second, we characterize the write error rate (WER) of 10^5 switching events. Figure 9(a) shows the WER of the AP-P transition at $t_{p,SOT} = 0.4$ ns as a function of I_{SOT} for $V_g = -1$, 0, and 1 V. It reveals that, even though $V_g = 1$ V reduces I_c by 25%, a wider separation for the WER curves is required to achieve full selectivity. To define gate selectivity, we introduce the S_g parameter, which is the ratio of the WER of the selected cell to the read error rate

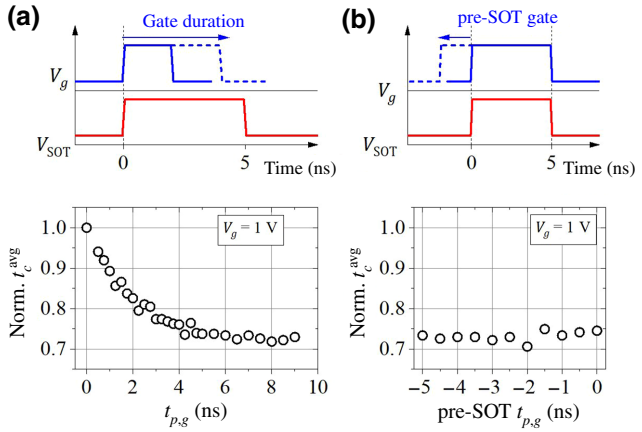

FIG. 8. (a) Normalized I_c^{avg} as a function of $t_{p,g}$ with $V_g = 1$ V. SOT and gate pulses are synchronized, and $t_{p,SOT} = 5$ ns. $t_{p,g}$ is progressively increased from 0 to 9 ns. (b) Normalized I_c^{avg} as a function of additional $t_{p,g}$ prior to primitive 5-ns overlay of the SOT pulse.

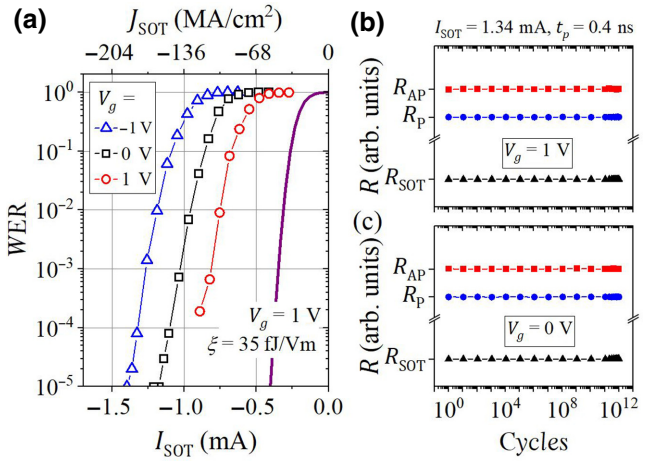

FIG. 9. (a) WER of 10^5 events for the AP-P transition at $t_p = 0.4$ ns. Purple curve predicts the WER for $\xi = 35$ fJ/Vm at $V_g = 1$ V, which is required to achieve full selectivity. (b) Endurance tests of 10^{12} cycles at applied SOT current $I_{SOT} = 1.34$ mA and $t_p = 0.4$ ns with 50 MHz repetition rate for (b) selected cell $V_g = 1$ V and (c) unselected cell $V_g = 0$ V.

(RER = 1 − WER) of the unselected cell:

$$S_g = \frac{\mathrm{WER}(V_g)}{\mathrm{RER}(V_g = 0)} = \frac{\mathrm{WER}(V_g)}{1 - \mathrm{WER}(V_g = 0)} > 1. \quad (10)$$

A full gate selectivity requires $S_g > 1$, meaning, for example, that, at $\mathrm{WER}(V_g) = 10^{-5}$, the RER ($V_g = 0$) of unselected devices must be below 10^{-5}. However, we emphasize that the S_g value will mostly depend on application requirements. To predict the required ξ to reach the target S_g, we include the VCMA effect in the WER switching-current distribution model for the SOT scheme [30]:

$$\mathrm{WER}(V_g) = \exp\Big(-f_0 t_p \exp\Big\{-\Delta(V_g) \times \Big[1 - 2h_s(V_g)\Big(\frac{\pi}{2} - h_s(V_g)\Big)\Big]\Big\}\Big), \quad (11)$$

$$\Delta(V_g) = \Delta(V_g = 0) - \frac{\xi \pi D^2 V_g}{4 k_B T t_{MgO}} = \Delta(V_g = 0) - \beta \xi V_g, \quad (12)$$

$$h_s(V_g) = \frac{I_{SOT}}{I_{c0}(V_g)}, \quad (13)$$

where $h_s(V_g)$ is the ratio of applied SOT current to the intrinsic switching current, and $\Delta(V_g)$ is the retention at the applied gate. We note that Eq. (11) typically applies for long t_p and cannot properly quantify actual device parameters. However, it fits qualitatively well with our experimental data using $f_0 = 10$ GHz. We obtain $\Delta(V_g = 0) = 14$

and $\beta = 0.17$ m/fJ by fitting the experimental data, and Eq. (11) allows us to estimate that the device presented in this study would require $\xi > 35$ fJ/Vm at $V_g = 1$ V to realize $S_g > 1$. This is largely achievable in standard VCMA MTJ devices [14,25].

Lastly, we test the endurance for 10^{12} cycles at a repetition rate of 50 MHz using the following conditions: $I_{SOT} = 1.34$ mA and $t_p = 0.4$ ns. Such an I_{SOT} is much larger than the required current for WER $< 10^{-5}$. Figures 9(b) and 9(c) show that both the selected ($V_g = 1$ V) and unselected ($V_g = 0$ V) cells sustain this intensive writing stress and that both MTJs and SOT tracks remain intact without any degradation in resistances, proving that the VGSOT writing scheme is robust and resilient for high-performance memory applications.

IV. VGSOT DEVICE-SCALING PERSPECTIVES

A. Device-scaling criteria

From the above studies, we project the required θ_{SH} and ξ for the scaled VGSOT PMTJ based on two scaling criteria: SOT critical current and gate selectivity. We consider a 30-nm MTJ with $\Delta = 60$ and RA $= 20\ \Omega\,\mu m^2$ ($t_{MgO} \sim 1$ nm); these conditions are defined to achieve the required retention for embedded memory applications and to minimize the reading latency. Notably, the STT effect at such a RA range would have a negligible impact on magnetization when writing at subnanosecond speeds [31,32]. By combining Eqs. (2) and (4), I_c under gate assistance is derived as

$$I_c(V_g) \sim \frac{2e\mu_0 M_{S,FL} t_{FL}}{\hbar\theta_{SH}} \left(\frac{H_{k,eff}}{2} - \frac{\xi V_g}{\mu_0 M_{S,FL} t_{FL} t_{MgO}} - \frac{H_x}{\sqrt{2}}\right) \times w_{SOT} t_{SOT}. \quad (14)$$

Then, we implement Δ into Eq. (14) and obtain

$$\Delta = \frac{\mu_0 M_{S,FL} H_{k,eff} \pi D^2 t_{FL}}{8 k_B T}, \quad (15)$$

$$I_c(V_g) \sim \frac{w_{SOT} t_{SOT}}{\hbar\theta_{SH}} \left(\frac{8 e k_B T \Delta}{\pi D^2} - \frac{2e\xi V_g}{t_{MgO}} - \frac{e\mu_0 M_{S,FL} t_{FL} H_x}{\sqrt{2}}\right), \quad (16)$$

where D is the MTJ diameter, k_B is the Boltzmann constant, and T is the ambient temperature. Using Eq. (16) and the parallel resistance model, we project in Fig. 10 the required I_{eff} for 1-ns writing speed based on our experimental results, with V_g being fixed at -0.7 V, to adapt the maximum supply voltage of the core transistor at beyond the 10-nm technology node [33]. Moreover, to achieve a fully functional VGSOT MRAM, we consider $S_g > 1$ at WER$(V_g) = 10^{-5}$, which corresponds to $\xi > 130$ fJ/Vm in the scaled MTJ.

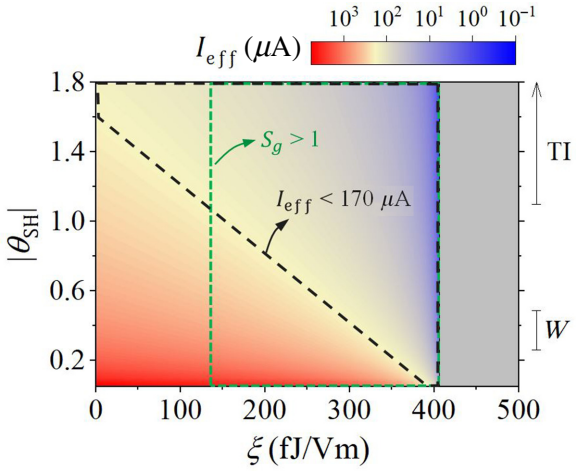

FIG. 10. Effective SOT switching current as a function of θ_{SH} and ξ. Following parameters are applied: $D = 30$ nm, $\Delta = 60$, $t_{MgO} = 1$ nm, and $V_g = -0.7$ V. Black outlined area indicates $I_{eff} < 170\ \mu$A and green outlined area indicates $S_g > 1$. Star symbol exemplifies required θ_{SH} and ξ to fulfill these targets.

With these calculations, we find that the VGSOT scheme can mitigate the requirements of challenging SOT and VCMA parameters. For example, one can achieve $I_{eff} = 170\ \mu$A using the standard material in SOT MRAM technology, such as tungsten, with $\theta_{SH} = -0.45$ [34]. Correspondingly, $\xi = 300$ fJ/Vm is needed, which can be implemented by appropriate interface engineering [35]. For comparison, these values are much more relaxed than the requirements for SOT MRAM ($|\theta_{SH}| > 1.6$) and for VCMA MRAM ($\xi > 800$ fJ/Vm, considering $t_{MgO} = 1.5$ nm at $\mu_0 H_x = 0$ mT) of the same Δ. A further reduction in I_{eff} would require emerging SOT materials with larger values, such as topological insulators (TI) [19,20]. We note that $\xi > 400$ fJ/Vm is not desired, as it would enter into a pure VCMA operation regime.

B. Design-to-technology co-optimization analysis

Finally, we perform an extensive design-to-technology co-optimization (DTCO) analysis to benchmark the VGSOT performance at the 5-nm technology node against other embedded memory technologies, such as static RAM (SRAM), STT MRAM, and SOT MRAM. In Fig. 11, the performance values for high-density (HD) and high-performance (HP) SRAM are estimated based on the device sizing constraints of different foundries [36–39]. We consider a 45-nm gate pitch and a 30-nm metal pitch for our STT MRAM [40] and SOT MRAM [41] designs to optimize the performances. The power consumptions are estimated for 128-kbit macromemory with 64-bit data output. For VGSOT MRAM, the two and four MTJ variants in VGSOT represent the number of pillars on a single SOT track within a single-bit cell [Fig. 1(b)]. VGSOT performance estimation would include variables such as the

Specs	Bit-Cell Types						
	SRAM		STT	SOT	VGSOT		
	HD	HP			2MTJ	4MTJ	Projected
Area (μm^2)	0.021	0.028	0.0084	0.016	0.0122	0.009	0.009
RD Power/bit (nW)	7.28	18.7	6.20	25.5	3.16	2.96	5.8
WR Power/bit (nW)	9.85	25.7	24.4	31.4	47.5	46.5	4.6
RD Latency (ns)	~1.5	~0.8	~2.8	~1	~10	~10	~5
WR Latency (ns)	~1.5	~0.8	~20	~2	~1	~1	~1
V_{DD} (V)	~0.7	~0.7	~0.7	~0.7	~0.7	~0.7	~0.7
Retention	-	-	>10yrs	>10yrs	>10yrs	>10yrs	>10yrs
Endurance	$>10^{16}$	$>10^{16}$	$>10^{9}$	$>10^{14}$	$>10^{14}$	$>10^{14}$	$>10^{14}$

FIG. 11. DTCO analysis of performance for different embedded memory technologies at 5-nm technology node, including SRAM, STT MRAM, SOT MRAM, and VGSOT MRAM. Projected values for VGSOT are estimated with improved MTJ properties.

number of MTJ pillars, the SOT line length or resistance, the spin Hall angle, and the VCMA coefficient. We estimate that the four-MTJ VGSOT design can significantly reduce the effective area compared with that of conventional SOT MRAM, making it comparable to STT MRAM and less than 50% of the HD SRAM with minimal performance degradation. As emphasized earlier, due to the large MTJ resistance in our present devices, the read performance is limited. This can be resolved by optimizing the RA product to RA = 20 $\Omega\,\mu m^2$ without compromising the benefits of VCMA gate effects. The write power of the two-MTJ and four-MTJ designs under the present VCMA coefficient remains larger than the typical SOT cell, which is due to the increase in SOT channel length and resistance. The minor difference between the write power of two-MTJ and four-MTJ designs stems from the change in the WL capacitance when increasing the number of pillars. Eventually, the write performance can also be enhanced with improved SOT and VCMA parameters. We project the VGSOT performance based on the following conditions: $\Delta = 60$, RA = 20 $\Omega\,\mu m^2$, SOT resistivity $\rho_{SOT} = 160\ \mu\Omega\,cm$, $\theta_{SH} = -0.45$, and $\xi = 300$ fJ/Vm. It shows 2 and 10 times improvements, respectively, in read latency and write power, opening design perspectives for high-performance, low-power, and high-density embedded memories as well as in memory computing applications.

V. CONCLUSION

We present a complete voltage-gate-assisted spin-orbit-torque switching study on PMTJ devices. Such a writing approach is of great interest, on one hand, to minimize the SOT write energy, and, on the other hand, to gain architecture density by combining multiple MTJs on the same SOT track with a VCMA gate acting as the bit selector. From the dependences of the SOT critical switching current on gate voltage (with a gate duration equal to the SOT pulse), we find that both the intrinsic current and the charge-conservation parameter, q, scale linearly with the gate voltage, which corresponds to the expected direct modification of PMA and nucleation energy by VCMA. We also propose a generalized method to evaluate the VCMA coefficient from time-dependent switching experiments. As expected from a purely electronic VCMA effect, ξ_I is independent of the writing speed, and its value is similar to that obtained from the traditional magnetic field method, ξ_H. In addition, we show that a fully gate-overlaid SOT pulse is required to maximize the gate effects, and both pre-SOT and post-SOT gates have no impact on the SOT switching efficiency or selectivity. To highlight the VGSOT switching reliability, we investigate the write error rate down to 10^{-5} with no error, and both selected and unselected cell endure intensive write stress for more than 10^{12} cycles without signs of degradation. Interestingly, we show through a simple device metric analysis that the VGSOT scheme can ease the requirements of challenging high SOT and VCMA parameters. This would relieve the need for complex SOT materials with $\theta_{SH} > 1$, which currently raise the complexities for optimizing MTJ properties and integration processes. Finally, we benchmark the VGSOT device performance against other embedded memories (SRAM, STT MRAM, SOT MRAM) using design-to-technology co-optimization analysis, and we determine that the VGSOT four-MTJ design is energy efficient with a fast read-write speed and density close to that of a two-terminal device. This makes VGSOT an appealing candidate for memory applications requiring high density, high performance, nonvolatility, and low power.

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