Bilateral Photoresponse of a Graphene-Oxide-Semiconductor Heterostructure Diode

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(Received 14 September 2020; revised 5 February 2021; accepted 22 April 2021; published 28 May 2021)

We report on the photodetection properties of a graphene-oxide-semiconductor (GOS) diode by measuring its current-voltage characteristics under illumination with light-emitting diodes (LEDs). We demonstrate that a GOS structure, with graphene used as a transparent gate electrode to form an inversion layer at the oxide-semiconductor interface, can function as a GOS field-effect transistor operable at low temperatures down to 1.5 K. By investigating the gate tunneling current in a GOS diode with a transistor structure, we find that the dark current is below approximately 0.1 nA at $T = 150$ K, which is almost two orders of magnitude lower than that in a graphene-semiconductor (GS) Schottky-diode photodetector. Notably, the GOS diode shows a bilateral photoresponse in both forward- and reverse-bias regimes under LED illumination. The photocurrent responsivity R reaches approximately 100 mA/W at $T = 150$ K with a low bias voltage of approximately -0.6 V, which is one order of magnitude lower than that applied in a GS Schottky-diode photodetector. We propose that a GOS heterostructure can be made to behave as a *p-i-n* or an *n-i-p* diode by manipulating the polarity of the bias voltage applied to the graphene gate. In addition, we quantitatively simulate the key features of the dark current by taking into account the associated bipolar current in graphene along with band-to-trap tunneling and trap-assisted tunneling processes. Our theoretical model sheds light on the mechanism of the bilateral photoresponse of the GOS photodetector. Our work paves the way to engineering hybrid devices made of two-dimensional materials and conventional semiconductors with CMOS integrability.

DOI: 10.1103/PhysRevApplied.15.054067

I. INTRODUCTION

The metal-insulator-semiconductor (MIS) structure is a fundamental building block of semiconductor devices. For example, metal-oxide-semiconductor field-effect transistors (MOSFETs) are by far the most widely used components in electronic devices. The charge-coupled devices commonly used in digital cameras consist of MIS diodes packed into an array [1]. The MIS structure can also function as a photodetector and has been utilized in solar-cell-related devices with a detectivity ranging from visible to near-infrared light (0.4–2 μm) [2]. On the other hand, recent advances in vertically stacking two-dimensional (2D) materials have opened up a route to designing van der Waals heterostructure devices [3,4]. Graphene, a 2D sheet of carbon atoms arranged in a honeycomb lattice, is the premier 2D material that has been discovered, and exhibits various unique properties, which are appealing for postsilicon electronics, optoelectronics, and photonics [5–7]. Because of the high electron mobility and high electric-current-carrying capacity of graphene, graphene field-effect transistors have shown great promise in radio-frequency applications [8,9]. Furthermore, graphene possesses broadband optical transparency, which is a property highly in demand for optoelectronic devices such as displays, light-emitting diodes, solar cells, and touch panels [7,10]. Nowadays, it is generally believed that a variety of emerging composite materials, consisting of graphene and other 2D crystals, can be employed to realize versatile hybrid devices with unprecedented multifunctionality.

In parallel with the efforts on heterogeneous stacks of 2D materials, another approach is to engineer van der Waals interfaces between 2D crystals and conventional semiconductors. It has been demonstrated that graphene-semiconductor (GS) heterojunctions can behave like Schottky diodes and, therefore, can serve as photodetectors and solar cells [11–17], similarly to regular metal-semiconductor (MS) diodes. The current-voltage

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characteristics of GS heterojunctions exhibit rectifying behavior with a semiconductor-substrate-dependent barrier energy. Compared with their MS counterparts, GS Schottky-diode photodetectors have several advantageous features: voltage-tunable responsivity, a large dynamic range of six decades [15], high internal quantum efficiency (approximately 10% for a graphene-Si junction), and more sensitive infrared detection ability [12].

In the work presented here, we integrate graphene with a SiO_2/Si substrate to form a graphene-oxide-semiconductor (GOS) planar junction. Despite extensive studies of GS Schottky diodes, the electric and optical properties of GOS structures have been much less explored to date. Distinctly differently from the conventional metal-oxide interface in the MOS structure, graphene can provide two types of carriers in an electrode, electrons or holes, depending on whether the gate-tunable Fermi level lies above or below the Dirac point (DP). Correspondingly, the nature of the charges residing at the SiO_2/Si interface, whether they are accumulation, depletion, or inversion charges, is intimately related to the polarity of the gate voltage. Therefore, the GOS structure possesses more versatile transport pathways than the MOS structure does. In addition, the surface barrier associated with the extra oxide layer in the GOS structure significantly reduces the dark current compared with a GS photodetector. We present a systematic study of a GOS structure, including a GOS field-effect transistor (GOSFET) and a GOS photodetector. Our work shows that GOS heterostructure devices provide potential integrability with the photonic and electronic components utilized in MOS devices and open up a route to developing graphene-silicon hybrid devices.

II. DEVICE FABRICATION AND CHARACTERIZATION

The devices investigated are fabricated by transferring a large-area chemical-vapor-deposition (CVD)-grown graphene sheet onto a SiO_2/Si substrate. Figure 1(a) shows a cross-section schematic view of the silicon-based GOS structure. The oxide-silicon structure shown in Fig. 1(a) is fabricated by the Taiwan Semiconductor Research Institute. We adopt the fabrication parameters for cryo-MOSFETs reported earlier [18], and outline the key procedures below. The fabrication of the GOS device begins with a p-type (6×10^{15} boron atoms/cm^3) (100) silicon wafer of thickness 0.675 mm and then channel-stop doping with approximately 10^{14} boron atoms/cm^3 around the gate area. The source and drain, two n^+ regions, are formed by implanting 5×10^{15} arsenic atoms/cm^3. The device is patterned into a Hall-bar geometry for transport measurements. The subsequent step is to thermally grow an 80-nm-thick gate oxide. The interconnect contacts are made from 60-nm-thick aluminum layers, as shown by blue-colored pads in Fig. 1(b). After the deposition of the

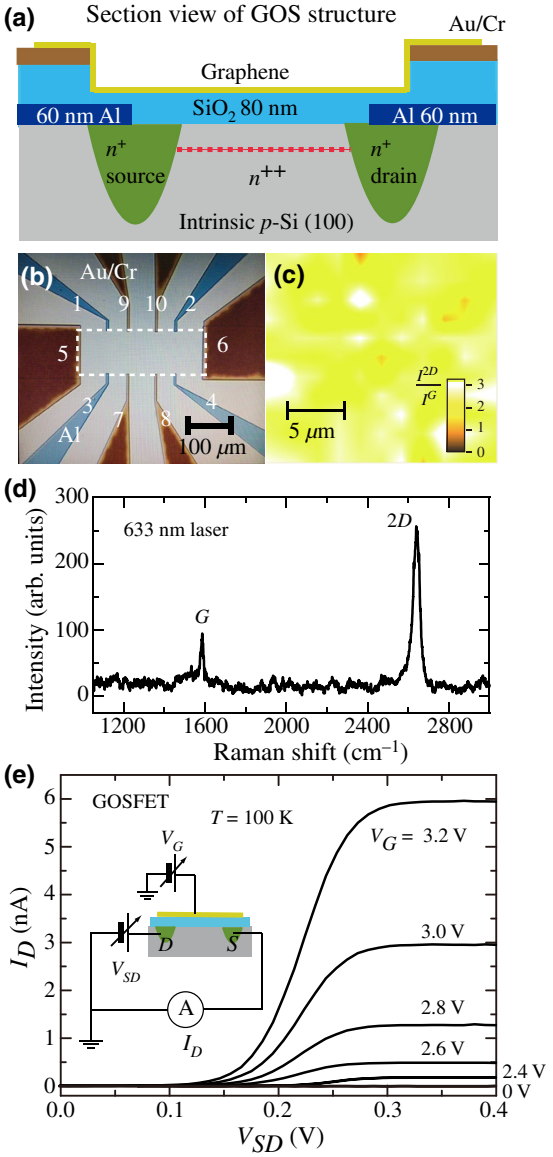

FIG. 1. (a) Schematic diagram of the device layout. (b) Top-view optical image of the device, which shows the interconnect voltage leads and the graphene contact leads. The blue-colored areas, marked by numbers from 1 to 4, are the voltage leads, and the brown-colored areas, marked by numbers from 5 to 10, are the graphene contacts, made with a Au(70 nm)/Cr(8 nm) bilayer. The dashed box denotes the channel region. (c) Mapping image using the Raman intensity ratio of the $2D$ and G peaks of the CVD-grown graphene transferred to the channel area, taken with 633-nm excitation at $T = 300$ K. (d) Raman spectrum of the CVD-grown graphene, taken from one spot of the graphene on the channel area. The intensity ratio of the $2D$ and G peaks is 2.6. (e) Drain current I_D versus drain-to-source voltage V_{SD} for a GOSFET operated at 100 K. The inset shows the measurement circuitry.

Al contacts, an additional SiO_2 layer with a thickness of 80 nm is employed in the shape of a square washer with a 400 μm $\times$ 400 μm hole. The goal of this layer is to

TABLE I. Device parameters of GOSFET at $T = 100$ K.

	Symbol (units)	Value
Channel length	L (μm)	300
Channel width	W (μm)	100
Threshold voltage	$V_{\rm th}$ (V)	0.1
Transconductance	g_m (MΩ)	15
Mobility	μ (cm^2/V s)	4.3
Zero-gate-voltage drain-source current at $V_G = 0$ V, $V_{SD} = 0.3$ V	I_{DSS} (nA)	6
Gate-source leakage current at $V_G = 0.3$ V, $V_{SD} = 0.0$ V	I_{GSS} (pA)	< 0.5

achieve electric isolation between the Al contact leads and the graphene contact leads. Next, the graphene contacts are made with a Au(70 nm)/Cr(8 nm) bilayer, as indicated by brown-colored areas in Fig. 1(b). Finally, CVD graphene is gently placed on the channel area, and the GOS structure is formed. For details of the preparation and characterization of the graphene, we refer readers to our previous publications [19–21]. To examine the quality of the graphene, we carry out micro-Raman mapping at room temperature as shown in Fig. 1(c), and take the Raman spectrum of one spot of the graphene on the channel area as displayed in Fig. 1(d). In general, approximately 95% of the channel area is found to have an intensity ratio of the 2D and G peaks (I^{2D}/I^{G}) larger than two, indicative of highly uniform monolayer graphene [21].

We first demonstrate that our GOS structure can function as a FET. For FET operations, all measurements are done in a light-tight enclosure. Figure 1(e) shows the drain current (I_D) versus the source-drain voltage (V_{SD}) for the GOSFET as a function of the graphene-gate voltage (V_G) at 100 K. It appears that the device acts like a gate-voltage-dependent resistor in the low-V_{SD} regime, whereas it operates more like a gate-voltage-controlled current source in the high-V_{SD} regime, which resembles the key features of a FET. We measure 10 sets of devices, and all of them reveal consistent results. The device parameters extracted from the measured I_D-V_{SD} curves of a representative device are summarized in Table I. The measured channel mobility μ (approximately 4–5 cm^2/V s) is relatively low, which is attributed to an increase in contact resistance at low temperatures. It should be noted that the performance of the GOSFET may be improved in the future after further optimization of the fabrication parameters, e.g., by increasing the doping concentration in the channel-stop layer and minimizing the issue of incomplete ionization [22–25], to facilitate specific applications.

We shall now make some brief remarks on the advantages of a graphene gate. For a comparative experiment, we implement a conventional MOSFET device with the same geometry as the GOSFET by depositing aluminum as the metal gate in the last fabrication step. The gate leakage

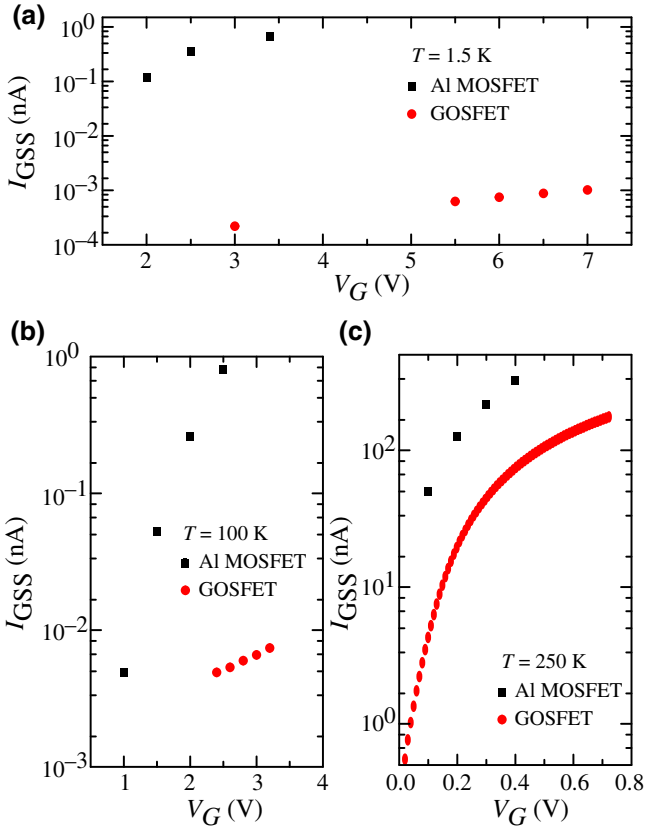

FIG. 2. Leakage current I_{GSS} versus gate voltage V_G for a GOSFET and an Al MOSFET operated at different temperatures. (a) I_{GSS} versus V_G at 1.5 K. I_{GSS} for the GOSFET is 4 orders of magnitude lower than that for the Al MOSFET at $V_G = 3$ V. (b) At 100 K and $V_G = 2.5$ V, the difference in the magnitude of I_{GSS} is on the order of 2. (c) At 250 K and $V_G = 0.4$ V, I_{GSS} for both devices is of the same order of magnitude.

current (I_{GSS}) of the GOSFET is found to be 4 orders of magnitude lower than that of the Al MOSFET. Figure 2 shows the leakage current I_{GSS} versus the gate voltage V_G for a GOSFET and an Al MOSFET operated at different temperatures. The differences of the leakage current at 1.5, 100, and 250 K are shown in Figs. 2(a), 2(b), and 2(c), respectively. This suggests that the graphene-SiO_2 van der Waals interface could possibly form a strain-free reliable structure that could significantly suppresses the leakage paths that could be induced by employing an Al metal gate [26].

III. PHOTORESPONSE OF THE DEVICE

We proceed to report on the photoresponse of the GOS device. Figure 3 shows typical curves of gate current versus bias voltage for the GOS device under visible-light illumination. Here, the gate current (I_G) is defined as the current flowing through the GOS device. The inset of

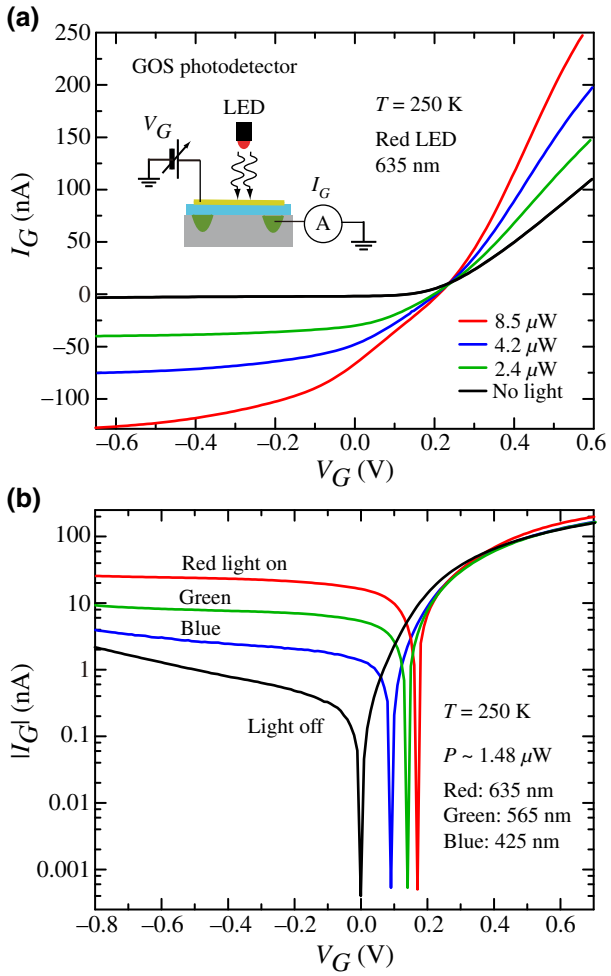

FIG. 3. (a) Gate current (I_G) versus gate voltage (V_G) for a GOS photodetector under illumination with a red LED with power $P = 0$ (no light), 2.4, 4.2, and 8.5 μW. The black solid line represents the trace of the dark current as a function of V_G, which exhibits a conventional photodiodelike behavior. The inset illustrates the measurement circuitry. (b) Semilog plot of $|I_G|$-V_G curves for the GOS photodetector exposed to different-colored lights with a fixed power of 1.48 μW at $T = 250$ K.

Fig. 3(a) displays the setup for photodetection measurements. Light-emitting diodes (LEDs) of three different colors, with peak emissions at wavelengths $\lambda = 635$ (red), 565 (green), and 425 (blue) nm, are used as the light sources. They are mounted, enclosed in a shielded holder, in front of the GOS device. The emission power (P) is controlled by the forward-bias current through the diode and is carefully calibrated by a power meter. The LEDs used here fail to illuminate when the temperature T is below approximately 100 K. Therefore, all measurements are carried out at temperatures above 100 K, even though our GOS device, operated in the FET mode, still functions properly at temperatures down to 1.5 K. The measured I_D-V_{SD} curves of the GOSFET at a temperature of 1.5 K are shown in Fig. 4.

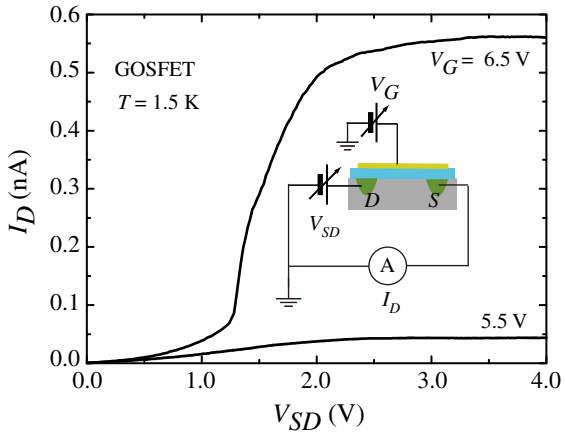

FIG. 4. Drain current I_D versus drain-to-source voltage V_{SD} for a GOSFET operated at 1.5 K. The inset shows the measurement circuitry.

Figure 3(a) shows the I_G-V_G characteristics of the GOS device for V_G from −0.6 to 0.6 V. The red LED is used as a light source, and the measurements are taken at $T = 250$ K with and without illumination. The dark current (I_{dark}, I_G at $P = 0$) shown in Fig. 3(a) (the black line) exhibits rectifying behavior, which is similar to that observed in a GS or conventional photodiode. However, the dark current of the GOS device, on the order of 0.1–100 nA within the range of V_G applied, is two orders of magnitude lower than that found in a GS diode [12,15,17]. More interestingly, a photoresponse is evidently observed in both the reverse- and the forward-bias regimes, which is distinctly different from the situation for GS and MOS photodetectors. For a MOS photodiode, the dark current in the reverse-bias regime is essentially unchanged upon light exposure [2,27]. In contrast, a photoresponse can be observed only in the reverse-bias regime for a GS diode [12,15,17]. In light of the above-mentioned information, the experimental findings suggest a photogeneration mechanism in the GOS device. The photocurrent responsivity (R) of the detector is defined as $R = \Delta I_G/P$, where ΔI_G ($= I_G - I_{\text{dark}}$) denotes the photocurrent. We find that R is around 17 mA/W at $V_G = -0.6$ V and around 20 mA/W at $V_G = 0.6$ V, at $T = 250$ K. Figure 3(b) shows a semilog plot of $|I_G|$-V_G curves taken under illumination with the three different colors of LEDs with the irradiation power P controlled at approximately 1.48 μW. It appears that the photocurrent exhibits a more noticeable λ dependence in the reverse-bias regime. R is approximately 13.83, 4.46, and 1.04 mA/W at $V_G = -0.2$ V for red, green, and blue light, respectively, which is consistent with the lower quantum efficiency for shorter-wavelength visible light in Si-based photodetectors [1]. Moreover, the values of I_G for different P or λ merge at $V_G \sim 0.27$ V, in the vicinity of the threshold voltage V_{th} [see Figs. 3(a) and 3(b)]. The anomalous features of the photocurrent, with an asymmetric

gate-voltage dependence, indicate that the photoresponses in the forward- and reverse-bias regimes are associated with different mechanisms.

Our GOS device is designed to operate in cryogenic environments. To have a better understanding of the bilateral photoresponse, we investigate the temperature dependence of the current–bias-voltage characteristics of the GOS diode, as shown in Fig. 5(a). The I_G-V_G curves are taken under weak red-light illumination with $P = 1.26$ μW at $T = 250$, 200, 175, and 150 K. Note that the I_G-V_G curves evolve from a diodelike behavior at $T = 250$ K [see also Fig. 3(a)] to a more symmetrical form with a bilateral photoresponse when T is lower than 175 K. At $T = 150$ K, the magnitude of I_G decreases and the distinct features of the bilateral photoresponse are preserved with decreasing P, as shown in Fig. 5(b). Furthermore, I_G is relatively small and insensitive to changes in the gate voltage for $V_G \leq V_{\text{th}}$ at lower temperatures. The inset of Fig. 5(a) shows the dark current versus V_G at various temperatures, and reveals a diodelike behavior at $T = 250$ K.

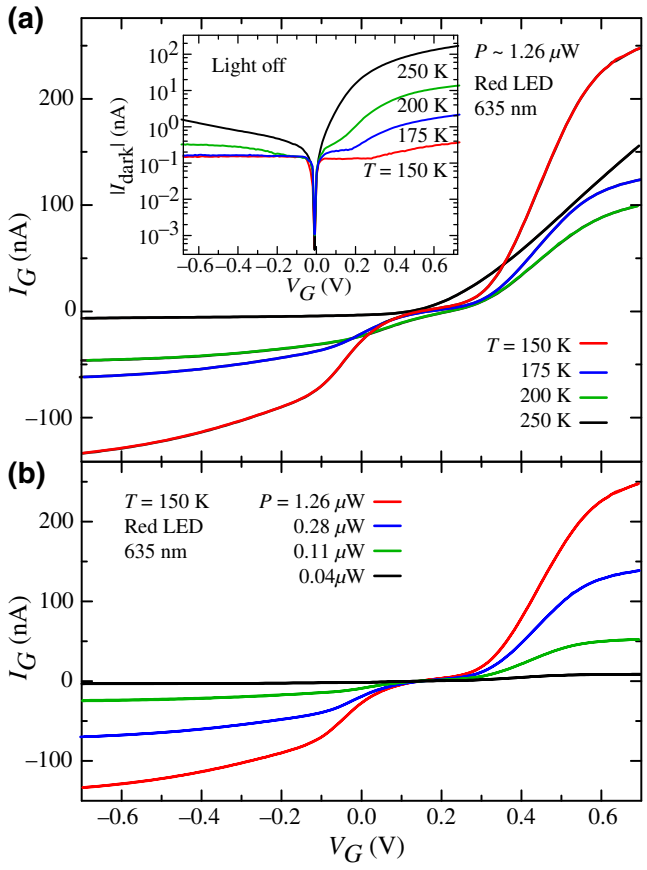

FIG. 5. (a) Current (I_G) versus gate voltage (V_G) measured at $T = 250$, 200, 175, and 150 K under illumination with a red LED with $P = 1.26$ μW. The inset plots the dark current (I_{dark}) in units of nanoamperes on a log scale as a function of V_G at various temperatures. (b) I_G versus V_G measured at $T = 150$ K with different powers of red light of 0.04, 0.11, 0.28, and 1.26 μW.

TABLE II. Responsivity R at various temperatures with an illumination power of 1.26 μW.

T (K)	R (mA/W) ($V_G = 0.6$ V)	R (mA/W) ($V_G = -0.6$ V)
250	1.40	4.28
200	60.1	35.4
175	88.2	48.0
150	178	102

However, the magnitude of the dark current is strongly suppressed with decreasing temperature and reaches the noise floor, on the order of 0.1 nA, in the reverse-bias regime when T is lower than 175 K. Table II summarizes the temperature dependence of R at $V_G = \pm 0.6$ V under illumination with the red LED at $P = 1.26$ μW. Despite the reduction of thermally excited carriers at lower temperatures, R increases to 102 and 178 mA/W at $T = 150$ K for $V_G = -0.6$ and $+0.6$ V, respectively. It should be noted that the values of R are comparable to those found in GS Schottky photodetectors [12,15,17], and the bias voltage is one order of magnitude lower than that applied in GS Schottky-diode photodetectors.

IV. FORMATION MECHANISM OF PHOTODETECTOR

In order to explore the underlying mechanism of the photoresponse, we make an attempt to simulate the gate tunneling current through the vertical GOS structure as a function of the gate bias. Because the optical absorption of single-layer graphene is approximately 2.3% [5], we attribute the photodetection of the GOS diode mainly to a photoresponse taking place in the silicon layer. Theoretical models for the gate tunneling current in MOS diodes, in both the inversion and the accumulation regimes, are well studied [2,28,29]. However, comprehensive modeling and numerical simulation of the whole tunneling process in a GOS diode rely not only on a knowledge of realistic distribution functions for the charge carriers, but also on various material parameters associated with the device layout and fabrication. For a proof of concept, instead, we employ a simplified model to account only for the key tunneling pathways with the minimum number of adjustable parameters to capture the essential features observed in the experiments. We consider two main carrier-generation mechanisms: band-to-trap tunneling and the Shockley-Read-Hall (SRH) model. The latter is also referred as the trap-assisted generation and recombination model [30]. Note that the photoresponse is observed at a relatively low gate voltage ($V_G \leq \pm 0.6$ V); therefore, we ignore the band-to-band tunneling current in our GOS device. On the other hand, in most conventional MOS diodes with a thin oxide thickness (typically less than or equal to 3 nm),

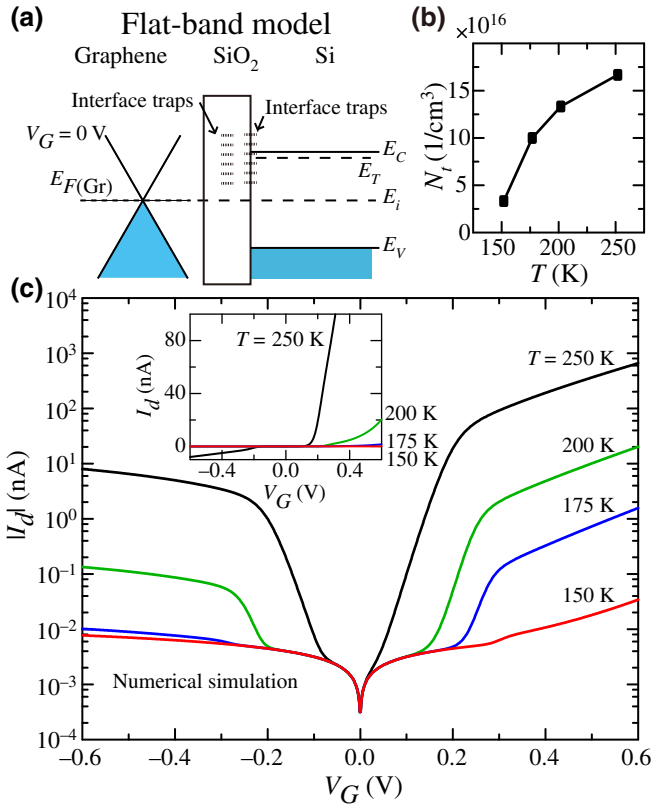

FIG. 6. Modeling and simulation of tunneling current in a GOS device. (a) Schematic energy-band diagram of a flat-band model for the GOS device, which reproduces the key features of the measured gate current (I_G) versus the applied gate voltage (V_G). The parameters of the energy levels for the simulation are illustrated in the diagram (see the text and Table III for details). (b) Temperature dependence of the trap density in the oxide layer estimated from the observed I_G. (c) Semilog plot of numerically simulated absolute dark current $|I_d|$ versus applied gate voltage (V_G) at temperatures $T = 150$, 175, 200, and 250 K. The inset shows the simulated I_d-V_G curves on a linear scale.

the current is dominated by the minority-carrier generation rate via traps at the Si/SiO_2 interface due to the effective tunneling rate at a large gate bias through the oxide, whereas the tunneling rate in our GOS device is governed by the capability of graphene to supply carriers, which varies with the gate bias, the trap-assisted tunneling in the oxide, and junction effects in the source-drain contacts. We elaborate on these factors and incorporate their contributions to the dark current in our model below.

A schematic energy-band diagram of the GOS device is illustrated in Fig. 6(a). We begin by representing the charge-carrier density per unit area Q_{gr} on the graphene electrode as $Q_{gr} = qn_{induced} = Q_s$, where $Q_s = C_{ox}V_{ox}$ is the total charge per unit area, $C_{ox} = \epsilon_{ox}/d$ is the capacitance of the oxide per unit area, d is the oxide thickness, and $n_{induced}$ is the induced carrier density on graphene with a Fermi energy $E_F^{gr} = \hbar v_F\sqrt{\pi\,|n_{induced}|}$, where v_F ($= 1.1 \times 10^8$ cm/s) is the Fermi velocity of graphene [13]. To minimize the number of model parameters without losing the most essential features, we assume that the graphene remains at its charge-neutrality point and assume the absence of any work-function differences, i.e., the flat-band condition at $V_G = 0$. The applied gate voltage V_G appears partly across the insulator, V_{ox}, and partly across the silicon, V_s. Thus, we have $V_G = V_{ox} + V_s$, where V_s is referred to as the surface potential and its magnitude is restricted to be close to the potential difference between the Fermi level of silicon and the intrinsic Fermi level (E_i) due to the small V_G ($\leq \pm 0.6$ V) applied to the GOS device. We therefore reasonably assume that the space-charge width (W_{SC}) in both the depletion or weak inversion regime and the accumulation regime is related to V_s as $V_s = qN_AW_{SC}^2/2\epsilon_s$, where ϵ_s is the dielectric constant of silicon and N_A is the acceptor concentration [1,30].

Within the framework of the conventional SRH model, the generation rate of electron-hole pairs U can be described as follows [30]:

$$U = \frac{pn - n_i^2}{\tau_p\left[n + n_i\exp\left(-\frac{E_T-E_i}{k_BT}\right)\exp\left(-\frac{eV_s}{k_BT}\right)\right] + \tau_n\left[p + n_i\exp\left(\frac{E_T-E_i}{k_BT}\right)\exp\left(-\frac{eV_s}{k_BT}\right)\right]}, \tag{1}$$

where n and p are the electron and hole densities, respectively, n_i is the intrinsic carrier density, E_T is the trap energy level, and τ_p and τ_n are the lifetimes of holes and electrons, respectively. To account for both electron and hole tunneling in heavily doped gated diodes, we adopt Hurkx *et al.*'s approach [31,32], which includes a modified generation rate of carriers via traps $G(x)$ of the form

$$G(x) = [1 + \Gamma(x)]U(x), \tag{2a}$$

$$\Gamma = \frac{2\sqrt{3\pi}\,|F|}{F_\Gamma}\exp\left(\frac{F}{F_\Gamma}\right)^2, \tag{2b}$$

$$F_\Gamma = \frac{\sqrt{24m^*(kT)^3}}{q\hbar}, \tag{2c}$$

where F is the local electric field in silicon and m^* is the effective mass of the carriers, with a value of $0.19m_e$ for electrons and $0.55m_e$ for holes. The thermal generation rate of carriers via the interface states is calculated via G_{Dit},

TABLE III. Parameters for simulation of I_d-V_G characteristics.

	Symbol (units)	Value
Hole carrier density	p $(1/\mathrm{m}^3)$	$5 \times 10^{15} \times \exp(E_c/300k_B) \times \exp(\xi eV_s - E_c/k_BT)$ $\xi = \begin{cases} 0 & \text{if } V_G \geq 0 \\ 0.01 & \text{if } V_G < 0 \end{cases}$
Electron carrier density	n $(1/\mathrm{m}^3)$	$n_i^2/p \times \exp(-\xi eV_s/k_BT)$ $\xi = \begin{cases} 0.1 & \text{if } V_G \geq 0 \\ 0 & \text{if } V_G < 0 \end{cases}$
Intrinsic carrier concentration	n_i $(1/\mathrm{m}^3)$	$5.29 \times 10^{23} \times T/300^{2.54} \times \exp(-6726/T)$ [38]
Trap energy level	E_T (eV)	0.5
Intrinsic Fermi energy of Si	E_i (eV)	0
Conduction-band energy of Si	E_c (eV)	0.57
Valence-band energy of Si	E_v (eV)	−0.57
Trap density	N_t $(1/\mathrm{cm}^3)$	10^{16}–10^{17}
Generation rate via interface states	G_{Dit} $(1/\mathrm{cm}^2\ \mathrm{eV})$	$\sim 10^{11}$ [29]
Channel area	A $(\mu\mathrm{m}^2)$	300 μm × 100 μm
Space-charge width	W_{SC}	$\sqrt{2\epsilon_{\mathrm{ox}}V_s/qn}$
Local electric field of silicon	F	V_s/W
Junction parameter	η	0.01

where Dit is interface trap density [29]. Here we assume that the density of trapped electrons and holes is uniformly distributed within the band gap.

The dark gate current density J_d can be expressed as

$$J_d = (qN_t)\left\{\int_0^W G(x)\,dx + \int_{E_v}^{E_c} G_{\mathrm{Dit}}\,dE\right\}\exp\left(\frac{\eta qV_{\mathrm{Si}}}{k_BT}\right), \tag{3}$$

where N_t is the trap density residing in the oxide layer; the value of N_t that we obtain is consistent with previous reports [33–35]. The term in the curly brackets includes two integration components, the first one of which expresses the band-to-trap tunneling and the second of which represents the band-to-interface tunneling, and the final exponential term describes the junction effects in the source-drain contacts.

The parameters of our model for device simulation are summarized in Table III. Before presenting the simulation results, we would like to justify three free parameters, N_t, η, and ξ, which are adjusted to fit the features of the measured dark current shown in the inset of Fig. 5(a). The oxide layer in our device is sufficiently thick (approximately 80 nm), in principle, to make the direct tunneling and Fowler-Nordheim tunneling currents through the oxide negligibly small at a small $|V_G|$. Nevertheless, the injection current density through the SiO_2 is observed to be up to approximately 10^{-2} A/cm^2 at $T \sim 250$ K, and decreases drastically to approximately 10^{-5} A/cm^2 at $T \sim 150$ K when V_G is less than ±0.6 V. This suggests that the gate tunneling current is predominantly carried by thermally excited electrons and holes hopping from one trapped state to the next in a low-electrical-quality oxide [1]. The oxide traps may be due to mobile ionic charges and defects in the SiO_2, which are known to be electrically neutral and can be charged by introducing electrons or holes. These defects are likely the source of the trap-assisted tunneling processes. We define the parameter N_t as the density of trap centers per unit area. Note that N_t is a temperature-dependent parameter associated with a decrease in the activation energy, the capture cross section, and the number of phonons with lowering of the temperature. Furthermore, the gate tunneling current is measured via a transistor configuration. In the accumulation region, the contact leads on the silicon side form a p-n diode, which blocks the tunneling currents. We introduce an adjustable parameter η to describe the junction regularity. Finally, the inversion tunneling current in an NMOS diode is distinctly different from the accumulation current because of the lack of carrier supply [1]. This is the reason that conventional MOS diodes are operated under reverse bias as photodetectors. For a GOS diode, in contrast, not only the space-charge density in a p-type Si substrate but also the tunneling density of states in graphene [36] varies with the polarity of V_G. We introduce a parameter ξ for determining the carrier densities n and p to account for these effects. As shown in the inset of Fig. 5(a), I_{dark} at $V_G = 0$ V is about 0.5 pA, indicating that I_{dark} is limited by current noise in our system. We estimate the shot noise, expressed as $I_n = \sqrt{2Iq\,\Delta f}$, where Δf is the bandwidth of the measurement amplifier (approximately 6 kHz), to be on the order of picoamperes [37]. We therefore identify that the current noise is mainly dominated by shot noise in our GOS device. After integrating J_d obtained from Eq. (3) over the channel area, we add I_n up and denote the result as I_d, and plot the simulated I_d-versus-V_G characteristics, as displayed in Fig. 6(c).

Figure 6(c) shows the simulated gate-tunneling current, referred to as the dark current I_d, as a function of V_G at different temperatures. At any given temperature, the increase in the simulated I_d with $|V_G|$ is in qualitative agreement with the measured curves displayed in the inset of Fig. 5(a). As the temperature is lowered, I_d drops in general, due to a decrease in the thermal generation rate of electron-hole pairs, described by the temperature dependence of the band-to-trap transport equation in the SRH model. Within the range of the gate voltage V_G applied, most of the voltage drop is in the silicon, with the formation of depletion and accumulation regions. For $|V_G| \leq 0.6$ V, the correction term Γ is small, so that the SRH generation and recombination rates have similar behaviors in both regions. In the inversion region, I_d is dominated by the band-to-trap (oxide traps, bulk traps, and interface states) tunneling. However, in the accumulation region, where a p-n junction forms in the contacts, I_d is suppressed by the junction exponential term. This reconciles the asymmetric $|I_{\text{dark}}|$-V_G characteristics of the GOS device, as shown in the inset of Fig. 5(a).

V. DISCUSSION

We now proceed to provide a qualitative picture to elaborate on the photoresponse mechanism of the GOS diode based on the theoretical model proposed in the previous section. Figure 7(a) illustrates conditions under which the bias voltage V_G is positive and greater than the threshold voltage; it attracts electrons to form an inversion layer at the oxide/p-silicon interface. Accordingly, the quasi-Fermi level of the graphene, $E_{F(\text{Gr})}$, is tuned to be located below the DP, which causes the graphene to be in the p-doped regime. On the other hand, Fig. 7(b) displays the situation where V_G is negative, under which condition the negative charges on the gate attract holes from the substrate to yield an accumulation layer at the oxide-semiconductor interface. Correspondingly, the graphene is tuned to be in the n-doped regime. In this sense, the GOS device can be viewed as either a p-i-n ($V_G > 0$) or an n-i-p ($V_G < 0$) diode when the polarity of the gate voltage is manipulated.

In the following, we start by identifying the charge conduction in the GOS diode without photon excitation (the dark current). In terms of device structure and practical operation, our GOS diode can be classified as an n-channel GOSFET structure. In the reverse-bias regime, where $V_G < 0$, the conduction is primarily dominated by carrier transport processes from the graphene through the oxide layer [see Fig. 7(b)] and by transport of holes in the accumulation layer to n-type Si ohmic contacts [see Fig. 1(a)]. For the former process, minority holes in the n-doped graphene are generated via thermal excitation and subsequently injected into the hole-rich accumulation layer with the help of trap-assisted tunneling, shown as path 1

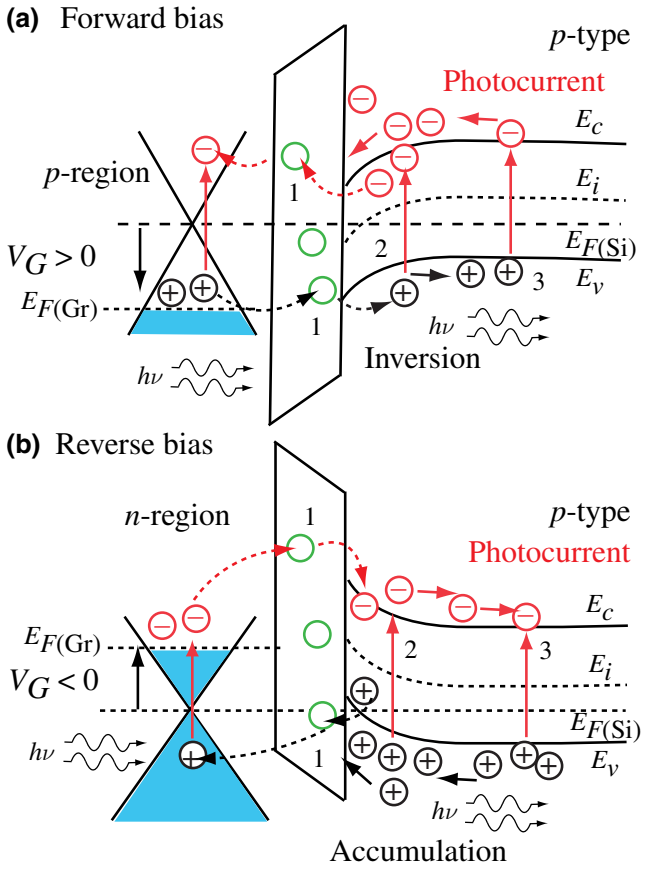

FIG. 7. Schematic energy-band diagram to illustrate photocurrent generation in a GOS photodetector under illumination in (a) the forward-bias regime and (b) the reverse-bias regime. The green open circles represent the trap centers inside the oxide. (Not to scale.)

in Fig. 7. However, the transport process is blocked by the depletion region formed at the interface between the accumulation layer and the n^+ contacts. The (dark) saturation current of the reverse-biased p-n junction at $V_G < 0$ depends on the density of p- and n^+-type carriers. Consequently, it has a temperature-dependent character. When the thermal excitation process is quenched at lower temperatures, the reverse dark current drastically diminishes and becomes insensitive to the gate voltage, as demonstrated in the inset of Fig. 5(a). Alternatively, in the forward-bias regime, where $V_G > 0$, an n inversion layer is formed at $V_G > V_{\text{th}}$, and electrical connection to the contacts is established. In this case, the forward dark current is mainly governed by the generation rate of thermally excited minority electrons in the p-doped graphene. As a whole, the gate-voltage dependence of the dark current resembles a diodelike I-V curve. When the thermal generation rate is quenched at lower temperatures, the dark current drastically diminishes, as demonstrated in the inset of Fig. 5(a).

Under irradiation, optical absorption takes place both in the graphene and in the p-Si substrate. Meanwhile, the graphene also acts as a charge-carrier collector or emitter, depending on the polarity of V_G. Owing to the unique properties of graphene, such as a gapless band structure and a flat absorption spectrum from 300 to 2500 nm, graphene exhibits efficient broadband photon-electron conversion [7]. The photoexcited electrons and holes in the graphene tunnel over the oxide barrier into the semiconductor, yielding photocurrents (path 1 in Fig. 7). On the silicon side, absorption of short-wavelength light occurs in the depletion region (path 2 in Fig. 7), and long-wavelength light can be absorbed in the neutral region, generating electron-hole pairs (path 3 in Fig. 7). Subsequently, the electrons and holes diffuse to the depletion and accumulation edges separately and are collected by electrodes. In the forward-bias condition, the photoresponse mechanism of the GOS diode is similar to that of a MIS photodetector. In the reverse-bias condition, the photon-generated excess carriers in the space-charge region of the accumulation layer are swept out of the depletion region quickly by the built-in electric field. The mechanism of photocurrent generation resembles that responsible for the photocurrent in a p-n junction photodiode. The aforementioned effects on the photocurrent are more pronounced when the number of thermally excited carriers is reduced at low temperatures. This accounts for the fact that our GOS photodetector shows different features in the bilateral photoresponse with decreasing temperature.

Before closing, we wish to make few comments on the future development of GOS-based devices. First, the GOS structure studied in this work is compatible with CMOS integrability. Our GOSFET thereby opens up a route for engineering types of FET devices based on GOS, MOS, or hybrid structures. Second, it has been demonstrated that MOS diodes can function both as light-emitting devices in the accumulation region and as photodetectors in the inversion region [27]. For the Schottky barriers and MIS structures used in photodetectors and solar cells, the thickness of the metal layer must be thin enough to allow a sufficient amount of light to reach the semiconductor. Remarkably, our GOS diode with graphene as a transparent gate overcomes this material obstacle and provides a means for harvesting photon energy. In conventional MOS diodes, the light is blocked by the thick metal gate electrode. As a result, the emission can be observed only at the diode edge, which limits the value of MOS diodes for lighting applications. From this perspective, the GOS diode is a promising candidate for electroluminescence investigations, a direction that has not been explored yet. Furthermore, our work addresses the tunneling behavior and energy-band properties of the GOS structure that are being studied ever more, and are of great importance to applications in photodetection. Finally, transparent electronic circuits are believed to be an essential component for next-generation optoelectronics [39]. Our GOS device could potentially pave the way toward the realization of transparent field-effect transistors or diodes.

VI. CONCLUSION

In summary, we develop a GOS photodetector with semiconductor processing technology by employing monolayer graphene to replace the metal layer used in the conventional MIS photodetector. To explore the functionality of the GOS heterostructure device, we first demonstrate that a GOSFET is operable at low temperatures down to 100 K. Note that its performance could be further improved after optimizing the fabrication parameters. Notably, we find that the GOS diode exhibits a bilateral photoresponse in both the forward- and the reverse-bias regimes under LED illumination. We propose that the photoresponse mechanism of the GOS diode in the forward-bias regime is similar to that of a MIS photodetector, whereas the mechanism of photocurrent generation in the reverse-bias regime resembles that of a p-n junction photodiode. As a result of the weak broadband absorption in graphene, we expect that the detectivity of our GOS photodetector can be easily extended over the range from the ultraviolet to the infrared for practical applications. Our results will stimulate cutting-edge research on tailoring stacked van der Waals materials for developing future hybrid optoelectronic devices.

ACKNOWLEDGMENTS

This work was supported by the Ministry of Science and Technology, Taiwan under Grants No. MOST 107-2112-M-007-003-MY3, MOST 109-2811-M-007-535-, MOST 109-2634-F-007-022, MOST 109-2627-M-002-003- and MOST 107-2112-M-032-010-, and also supported by the Center for Quantum Technology from the Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the Ministry of Education (MOE) in Taiwan under Grant No. 107-3017-F-007-001-.

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